Programmable Dual Output LCD Bias Power

Features

- Input voltage range (2.7V to 5.5V)
- Dual output regulator with single inductor
- High efficiency above 85%
- Charge pump with PFM mode at light load
- Programmable output voltages
- Positive output voltage range
  - ► +4.0V to +6.3V (100mV/step)
- Negative output voltage range
  - ► -4.0V to -6.3V (100mV/step)
- Programmable regulator offset voltage
- 1.0% output voltage accuracy
- Regulated output current up to 80mA
- Programmable active discharge
- I²C compatible interface
- 1 µA shutdown supply current
- Pb-free WLCSP-15 and TDFN-14 packages
- RoHS and Green Compliant
- -40°C to +85°C Temperature Range

Applications

- Smartphone TFT-LCD
- Tablet TFT-LCD
- General Dual Power Supply Applications

Brief Description

The KTD2151 is a TFT-LCD power supply IC for small and medium size displays for smartphones and tablets. The positive and negative output rails provide bias supplies for TFT LCD panels via the Source Driver IC. The device only requires a single inductor, to reduce the total PCB area.

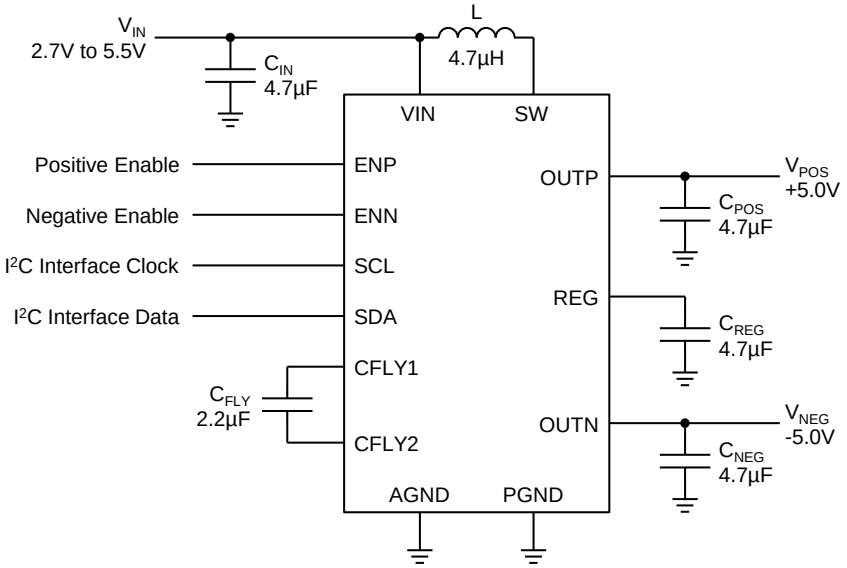
It features an integrated step-up DC-DC converter with input voltage range from 2.7V to 5.5V. An LDO and charge pump generate dual regulated outputs, whose voltages can be programmed via an I²C compatible interface. Optimized step-up, LDO and charge pump converters maximize conversion efficiency, exceeding 85%.

KTD2151 integrates all compensation and soft-start circuitry, which results in a simpler and smaller solution with much fewer external components. High switching frequency (1.8MHz) allows the use of a smaller inductor and capacitor to further reduce the solution size.

The I²C compatible interface allows control of the positive and negative outputs from +4.0V to +6.3V and from -4.0V to -6.3V, respectively, as well as programming additional registers on the device.

KTD2151 is available in a RoHS and Green compliant 15-bump 2.2mm x 1.45mm x 0.62mm WLCSP and 14-lead TDFN 2.5 x 3.0 x 0.75mm.

Typical Application

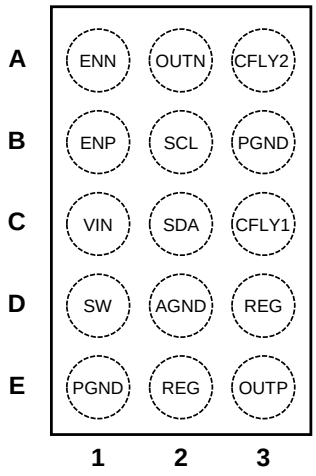


Pin Descriptions

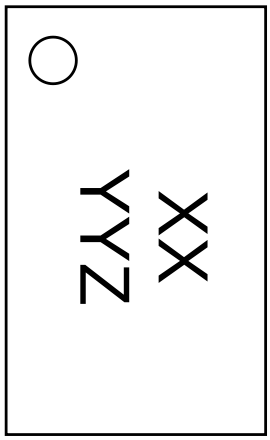
Pin # (WLCSP-15)	Pin # (TDFN-14)	Name	Function
A1	14	ENN	Enable input pin for negative output (OUTN)
A2	1	OUTN	Charge pump output pin of the negative power
A3	2	CFLY2	Negative charge pump flying capacitor pin
B1	12	ENP	Enable input pin for positive power (OUTP)
B2	13	SCL	SCL Clock input pin of the I²C interface
B3, E1	3, 8	PGND	Power GND connection
C1	10	VIN	Input supply pin for the IC
C2	11	SDA	SDA bi-direction data pin of the I²C interface
C3	4	CFLY1	Negative charge pump flying capacitor pin
D1	9	SW	Switch node pin of step-up converter
D2	5	AGND	Analog ground
D3, E2	6	REG	Step-up converter output pin
E3	7	OUTP	Positive LDO output pin

WLCSP-15

TOP VIEW

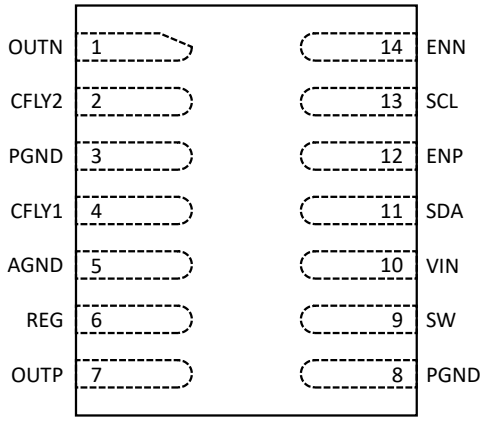


TOP VIEW



TDFN-14

Top View



15-Bump 2.2mm x 1.45mm x 0.62mm
WLCSP Package

Top Mark
XX = Device Code
YY = Date Code, Z = Assembly Code

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description		Value	Units
VIN	Input voltage		-0.3 to 6	V
SW	High voltage switching node	DC Voltage	-0.3 to 7	V
		Transient Voltage	-0.3 to 7.7 [2]	V
CFLY1	Charge pump pin		-0.3 to 7	V
OUTP, REG	Output voltage pin		-0.3 to 7	V
OUTN, CFLY2	Output voltage pin and charge pump voltage		-7 to 0.3	V
ENP, ENN, SCL, SDA	Control pins		-0.3 to VIN+0.3	V
T_J	Operating Temperature Range		-40 to 150	°C
T_s	Storage Temperature Range		-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at pins, 10 sec)		300	°C
ESD	HBM electrical static discharge		2.0	kV

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Transient voltage rating is with 300ns maximum duration and 50% maximum duty cycle.

Thermal Capabilities

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient[3]	77	°C/W
P_D	Maximum Power Dissipation at T_A = 25°C	1.3	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-13	mW/°C

3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Ordering Information

Part Number	Marking[4]	V_{POS} Default Setting	V_{NEG} Default Setting	I_{SD}[5]	Operating Temperature	MSL	Package
KTD2151EUO-TR	GRYYZ	+5.0V	-5.0V	6µA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151EUO-CC-TR	GZYYZ	+5.2V	-5.2V	6µA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-TR[6]	HMYYZ	+5.0V	-5.0V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-BB-TR[6]	HXYYZ	+5.1V	-5.1V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-CC-TR[6]	HOYYZ	+5.2V	-5.2V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-FF-TR[6]	HSYYZ	+5.5V	-5.5V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-GG-TR[6]	MJYYZ	+5.6V	-5.6V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151BEUO-JJ-TR[6]	MKYYZ	+5.8V	-5.8V	100nA	-40°C to +85°C	Level 1	WLCSP-15
KTD2151EXH-TR	GRYYZ	+5.0V	-5.0V	6µA	-40°C to +85°C	Level 1	TDFN-14

4. "YYZ" is the date code and assembly code.
5. Shutdown current with V_{IN} = 3.6V, ENP = ENN = 0 and SDA = SCL = 1.8V.
6. KTD2151B I^2C inputs are disabled when both ENP and ENN are logic low.

Electrical Characteristics[7]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.7V, ENN = ENP = V_{IN}, V_{POS} = +5V, V_{NEG} = -5V

Symbol	Description	Conditions	Min	Typ	Max	Units
IC Supply						
VIN	Input operating range		2.7		5.5	V
UVLO	Input under voltage lockout	Rising VIN			2.5	V
$UVLO_{HYST}$	UVLO hysteresis			0.2		V
I_Q	IC standby current	Not switching		620		µA
	IC operating current	Switching, no load		1.2		mA
I_{SHDN}	Shutdown current	ENP = ENN = 0V, SDA = SCL = V_{IN}		0.1		µA
Step-Up DC-DC Converter						
I_{LIM}	Peak NMOS current limit		0.9			A
F_{SW}	Oscillator frequency			1.8		MHz
D_{max}	Maximum duty cycle		80	86		%
T_S	Start-up time			0.7		ms
OUTP Positive Output VPOS						
V_{POS}	Positive output voltage range		4.0		6.3	V
V_{POS_ACC}	Positive output voltage accuracy	T_A = 25°C	-1.0		+1.0	%
I_{LIM_POS}	Positive output current limit		200			mA
V_{DROP}	Dropout voltage	I_{OUT} = 150mA		150		mV
V_{LINE}	Line regulation	V_{IN} = 3.2V to 4.2V, I_{OUT} = 30mA		0.06		%/V
V_{LOAD}	Load regulation	ΔI_{OUT} = 80mA		6		mV
$R_{DISCHARGE}$	Discharge resistance			70		Ω
OUTN Negative Output VNEG						
V_{NEG}	Negative output voltage range		-4.0		-6.3	V
V_{NEG_ACC}	Negative output voltage accuracy	T_A = 25°C	-1.0		+1.0	%
I_{LIM_NEG}	Negative output max regulated current		80			mA
F_{SW_CP}	Charge pump switching frequency			0.9		MHz
V_{LINE}	Line regulation	V_{IN} = 3.2V to 4.2V, I_{OUT} = 30mA		0.02		%/V
V_{LOAD}	Load regulation	ΔI_{OUT} = 80mA		14		mV
$R_{DISCHARGE}$	Discharge resistance			20		Ω
Logic Control: ENP, ENN						
V_{TH-L}	ENP, ENN pin logic low threshold	V_{IN} = 2.5V to 5.5V			0.4	V
V_{TH-H}	ENP, ENN pin logic high threshold		1.4			V
R_{ENP}	ENP pull down resistor			500		kΩ
R_{ENN}	ENN pull down resistor			500		kΩ

7. KTD2151 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics[8]

Symbol	Description	Conditions	Min	Typ	Max	Units
I²C-Compatible Voltage Specifications (SCL, SDA)						
V_{IL}	Input Logic Low Threshold	SDA, SCL			0.4	V
V_{IH}	Input Logic High Threshold	SDA, SCL	1.2			V
I²C-Compatible Timing Specifications (SCL, SDA)[8], see *Figure 1*						
t_1	SCL (Clock Period)		2.5			µs
t_2	Data In Setup Time to SCL High		100			ns
t_3	Data Out Stable After SCL Low		0			ns
t_4	SDA Low Setup Time to SCL Low (Start)		100			ns
t_5	SDA High Hold Time After SCL High (Stop)		100			ns
f_{SCLK}	SCL Clock Frequency				400	kHz
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			µs
t_{HD_STA}	Hold Time (Repeated) START Condition[8]		0.6			µs
t_{LOW}	LOW Period of SCL Clock		1.3			µs
t_{HIGH}	HIGH Period of SCL Clock		0.6			µs
t_{SU_STA}	Setup Time for a Repeated START Condition		0.6			µs
t_{HD_DAT}	Data Hold Time[9]		0		0.9	µs
t_{SU_DAT}	Data Setup Time[10]		100			ns
t_R	Rise Time of Both SDA and SCL Signals				300	ns
t_F	Fall Time of Both SDA and SCL Signals				300	ns
t_{SU_STO}	Setup Time for STOP Condition		0.6			µs
Thermal Shutdown						
T_{J-TH}	IC junction thermal shutdown threshold			140		°C
	IC junction thermal shutdown hysteresis			15		°C

8. KTD2151 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

9. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIHMIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.

10. A fast-mode device can be used in a standard-mode system, but the requirement t_{SU_DAT} = to 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + t_{SU_DAT} = 1000 + 250 = 1250nsec before the SCL line is released.

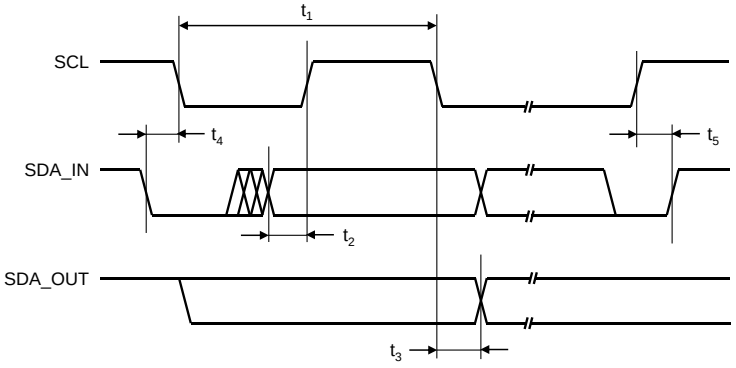
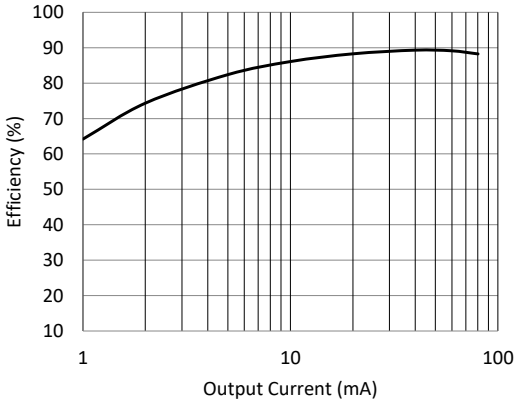


Figure 1. I²C Compatible Interface Timing

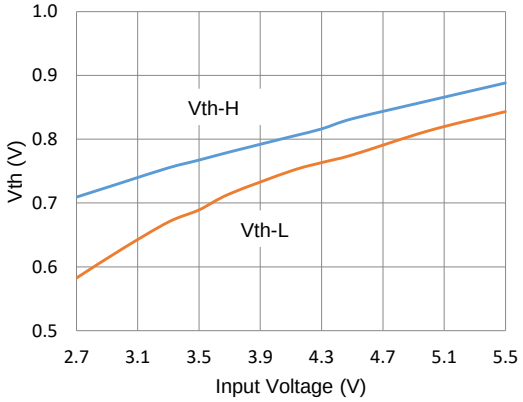
Typical Characteristics

V_{IN} = 3.7V, L = 4.7µH (Coilcraft LPS4018-472), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = 4.7µF, I_{POS} = -I_{NEG} = 40mA, Temp = 25°C unless otherwise specified. Default setting: V_{POS}/V_{NEG} = +/-5.0V, VREG Offset = 200mV.

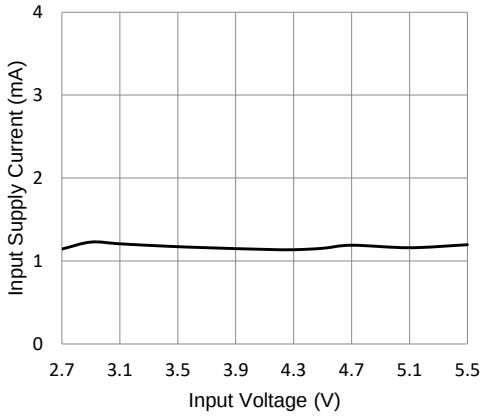
Efficiency vs. Output Current
(V_{POS}/V_{NEG} = +/-5.0V, VREG Offset = 200mV)



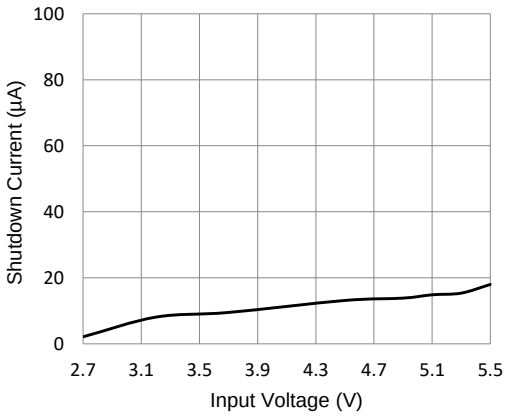
ENP / ENN Logic Threshold Voltage



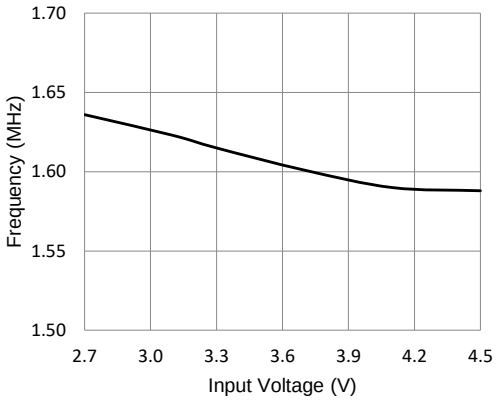
Quiescent Current
(no load)



Shutdown Current
(ENP = ENN = low)



Step-up Converter Switching Frequency



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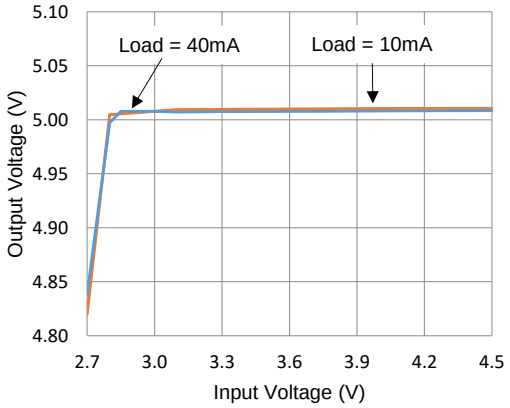
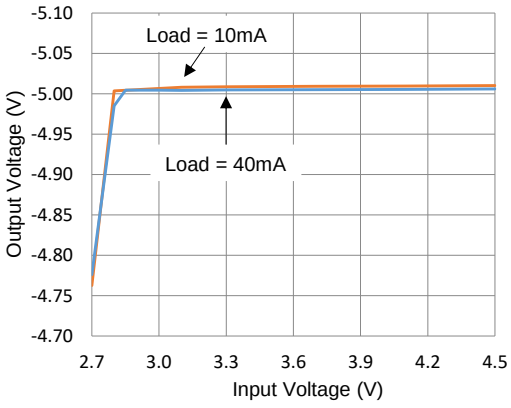
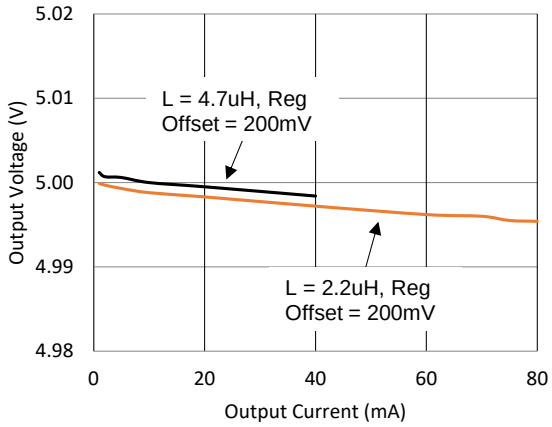
OUTP Line Regulation



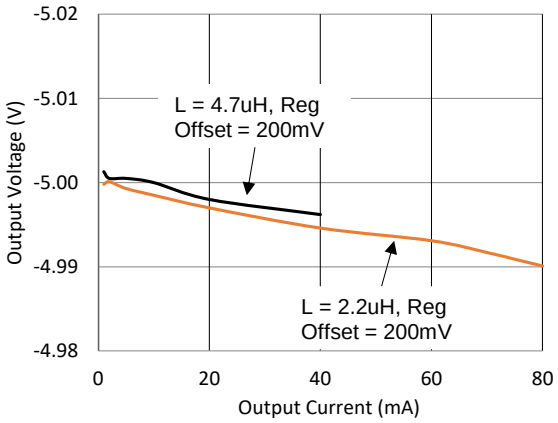
OUTN Line Regulation



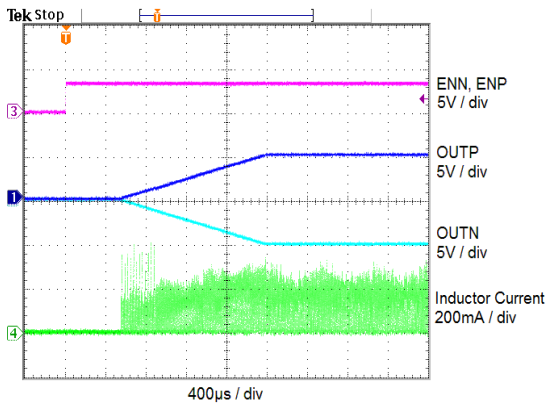
OUTP Load Regulation



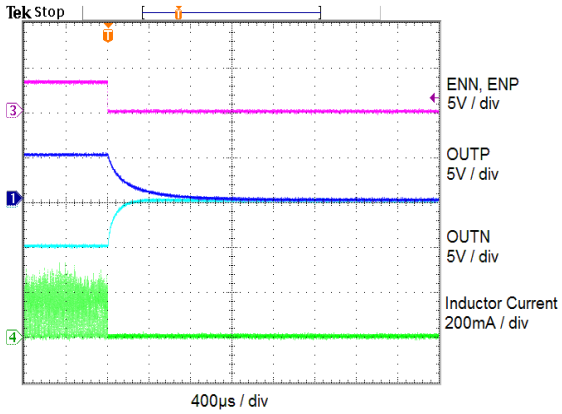
OUTN Load Regulation



Power-up
(40mA load)



Power-down
(40mA load)



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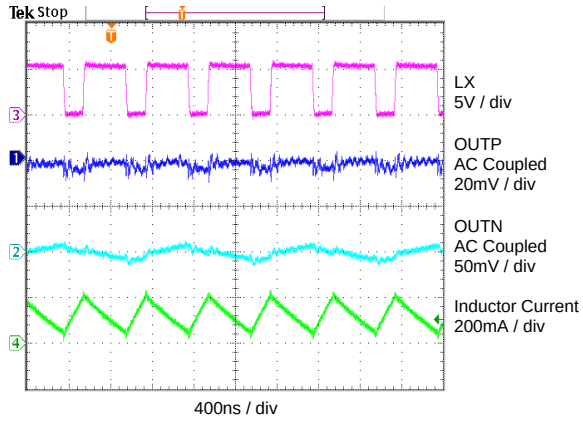
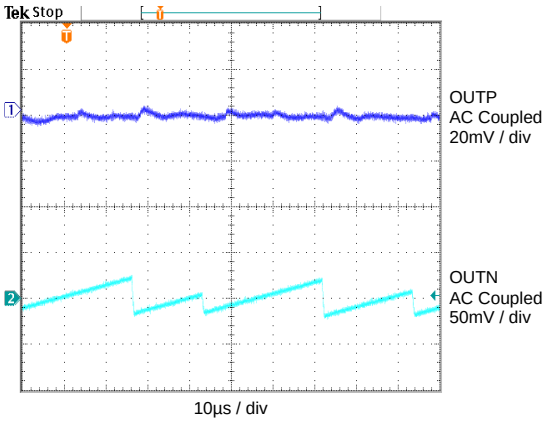
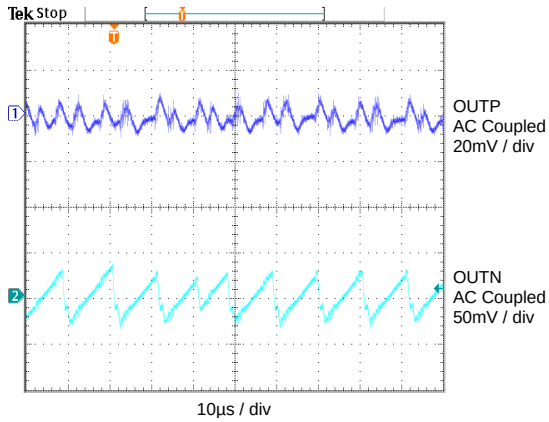
Switching Waveform
(I_{POS} = I_{NEG} = 40mA)



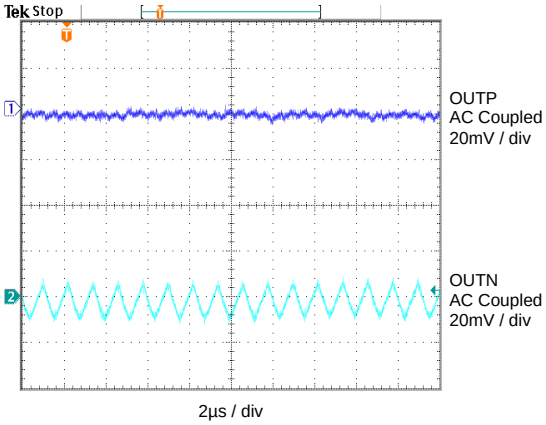
Steady-state Operation
(I_{POS} = -I_{NEG} = 2mA)



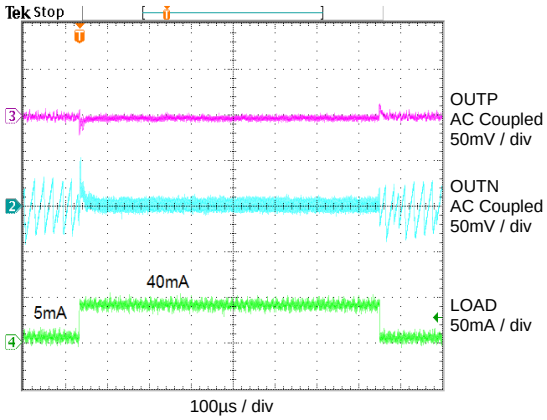
Steady-state Operation
(I_{POS} = -I_{NEG} = 10mA)



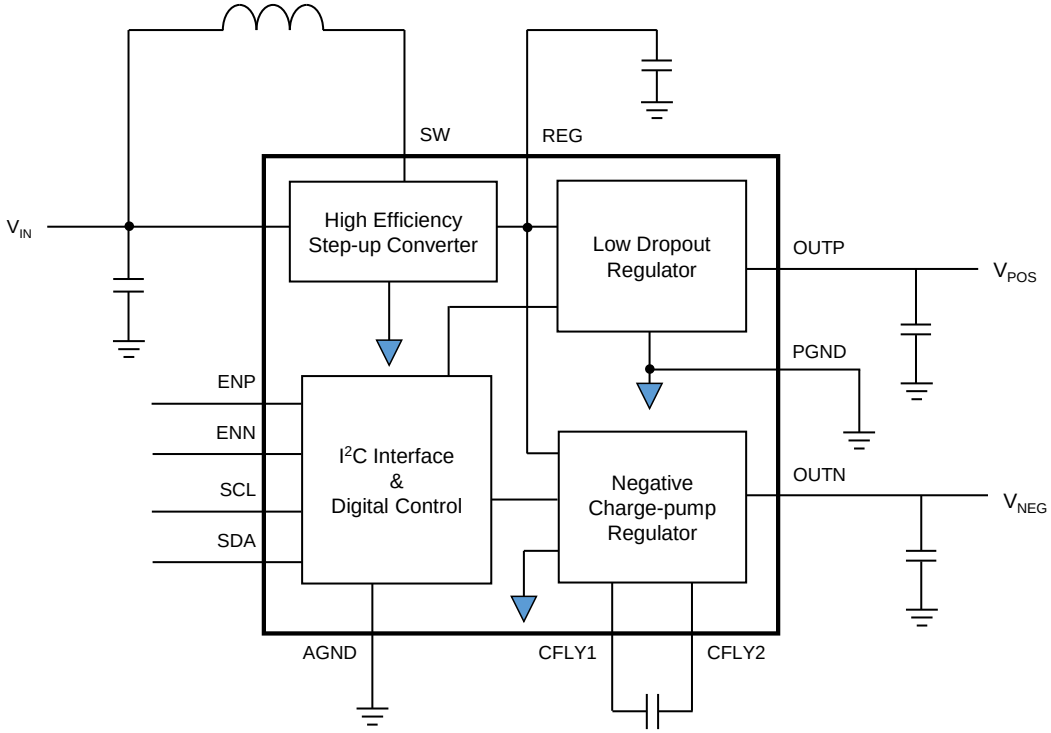
Steady-state Operation
(I_{POS} = -I_{NEG} = 40mA)



Load Transient
(5mA to 40mA step load)



Functional Block Diagram



Functional Description

The KTD2151, powered from single-cell Li-Ion/Polymer batteries from 2.7V to 5.5V, is a dual output converter only requiring a single inductor. The KTD2151 is a dual switching converter to generate both a positive and a negative power supplies that are required by TFT-LCD display panels. The KTD2151 integrates a boost regulator, LDO and charge pump, to generate two regulated output rails OUTP and OUTN, whose voltages can be adjusted by I^2C compatible interface. The step-up converter generates a positive voltage on the REG pin that is used by both the positive output and negative output converters. The internal LDO gets its power from the REG pin, drops down the voltage with optimized high efficiency linear control, delivering the positive supply (OUTP). The negative supply (OUTN) is generated by an integrated inverting voltage regulator charge pump driven from the step-up converter output.

The REG offset voltage, equal to the voltage between REG and the Max (OUTP, -OUTN), can be set to 200mV and 300mV depending on the maximum output currents on OUTP and OUTN. Higher output current requires higher offset voltage (headroom) in order to guarantee the best regulation. By adjusting the offset voltage to the lower level 200mV, the overall converter efficiency can be optimized for the application. The device can operate with independent current setting on each output, even with no load on one output and full load on the other.

The device integrates full compensation and soft-start circuitry, which results in a simpler and smaller solution with fewer external components. High switching frequency (1.8MHz) allows the use of a smaller inductor and capacitors to further reduce the solution size.

Under Voltage Lockout (UVLO)

The KTD2151 integrates an Under Voltage Lockout circuit to prevent the IC from operating until V_{IN} pin exceeds the UVLO threshold. Output voltages will not be activated until enable signals are applied. All of the internal converters will be disabled as soon as the V_{IN} voltage falls below the UVLO threshold minus the UVLO hysteresis ($UVLO_{HYST}$).

Active Discharge

The positive rail OUTP and/or the negative rail OUTN can be actively discharged by KTD2151. The output discharge settings can be programmed by the I²C interface; the default value is ON. When the supply output is powered down, KTD2151 will discharge the corresponding output(s) through the associated $R_{DISCHARGE}$ resistor connected to ground. The power-down happens when both enable signals (ENN, ENP) go low, or when one enable goes low while the other enable is already low. If one output is turned OFF while the other output stays ON, the discharge circuit is inactive for both outputs.

Step-Up DC-DC Converter Operation

The step-up converter uses a current mode design operating at 1.8 MHz in full load, allowing the use of small value 2.2µH or 4.7µH inductors. The converter dynamically adjusts the output to optimize the highest efficiency depending on OUTP and OUTN voltage requirements.

Power-Up and Soft-Start

The step-up converter operates when either enable signal, ENN or ENP, is pulled high or I²C bits are set, and VIN voltage is greater than UVLO. If the enable signal is already high when VIN reaches the UVLO threshold, the step-up converter will start switching immediately. An integrated soft-start circuit controls excessive inrush current from the battery during startup.

Power-Down

The step-up converter powers down when V_{IN} goes below UVLO minus $UVLO_{HYST}$ or after both OUTP and OUTN have been disabled, if VIN is still above UVLO.

LDO Regulator Operation (OUTP)

The internal LDO gets its power from the REG pin and drops down the voltage, generating the positive voltage rail OUTP. The LDO's ripple rejection characteristics help to filter the output of the boost converter in order to provide a well-controlled supply for the source driver IC of the TFT-LCD panel.

Power-Up and Soft-Start (OUTP)

The LDO is activated immediately when ENP signal is asserted, and VIN voltage is above the UVLO threshold and the step-up converter has reached its target voltage. OUTP has a soft-start circuit which slowly ramps-up its output.

Power-Down and Discharge (OUTP)

The LDO stops operating when VIN drops below the UVLO threshold minus the hysteresis, or when ENP is de-asserted. The positive supply output can be actively discharged to GND through the IC's $R_{DISCHARGE}$ internal resistor. The discharge selection bit by default is ON, and can be reset or set through register programming.

Setting the Output Voltage (OUTP)

The output voltage of the LDO is programmable via an I²C compatible interface with 5 bits, from 4.0V to 6.3V with 100mV steps.

Regulated Inverting Charge Pump Operation (OUTN)

The inverting charge pump generates the negative voltage rail OUTN from the output voltage of the boost converter (V_{REG}). The converter uses a four-switch topology with single external flying capacitor to generate the negative output voltage. The first switching phase turns on two of the switches to charge the flying capacitor equal to V_{REG}, and the second phase inverts the drive logic of all four switches, negatively connecting the flying capacitor to OUTN.

Power-Up and Soft-Start (OUTN)

The charge pump is activated immediately when ENN signal is asserted, and VIN voltage is above the UVLO threshold and the step-up converter has reached its target voltage. OUTN has a soft-start circuit which slowly ramps-up its output.

Power-Down and Discharge (OUTN)

The charge pump stops operating when VIN drops below the UVLO threshold minus UVLO hysteresis or when the ENN is de-asserted. The negative rail can be actively discharged to GND during power-down if required. A discharge selection bit is available to enable or disable this function.

Setting the Output Voltage (OUTN)

The output voltage of the charge pump is programmable via an I²C compatible interface with 5 bits, from -4.0V to -6.3V with 100mV steps.

Flying Capacitor Selection (OUTN)

The charge pump needs an external flying capacitor with a minimum value of 2.2µF. Ceramic X5R dielectric material or better is recommended for best performance. For higher current tablet application, a larger 4.7µF capacitor can be used. For proper operation, the flying capacitor value must be lower than the output capacitor of the boost converter on VREG pin.

Thermal Shutdown

A thermal shutdown feature is included in the KTD2151. When the IC's junction temperature (T_J) reaches 150°C, the IC will immediately enter shutdown mode. Once T_J drops 15°C to approximately 135°C, the IC will resume normal operation.

I²C interface or Enable Control

The KTD2151 can be turned on/off by pulling the ENP/ENN inputs high without using the I²C interface. If the I²C interface is not used, both SDA and SCL inputs should be tied high (for example to VIN directly) or through pull-up resistors. These two inputs should never be left floating (unconnected).

KTD2151 can be controlled via the I²C interface, even when both the ENP and ENN inputs are low. KTD2151B I²C inputs are disabled when both ENP and ENN are low. KTD2151B can be controlled via the I²C interface when ENN or ENP are logic high.

Application Information

I²C Serial Data Bus

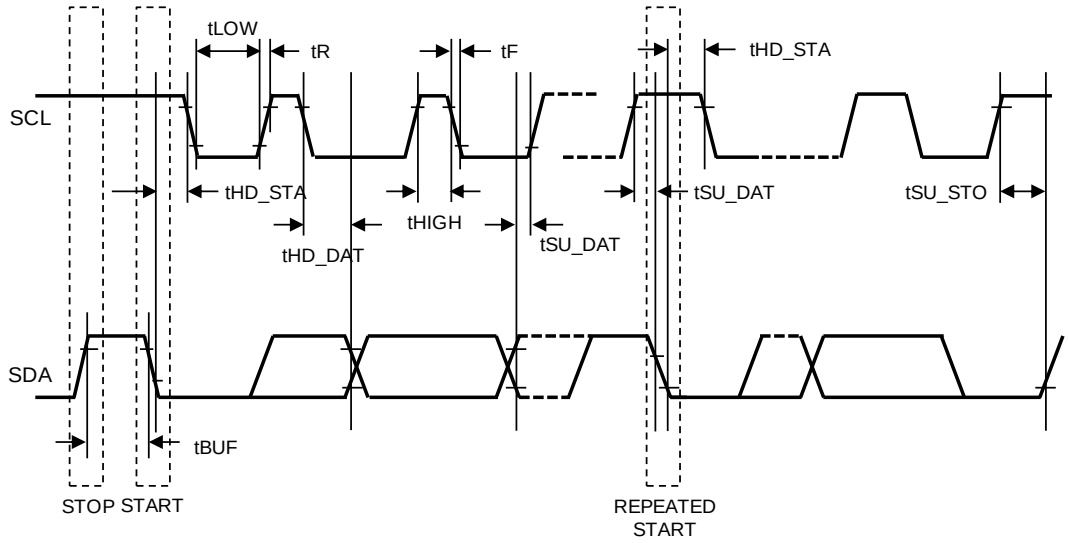


Figure 2. I²C Mode Timing Diagram

The KTD2151 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The KTD2151 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The KTD2151 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (Figure 2 and Figure 3):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy
Both data and clock lines remain HIGH.

Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

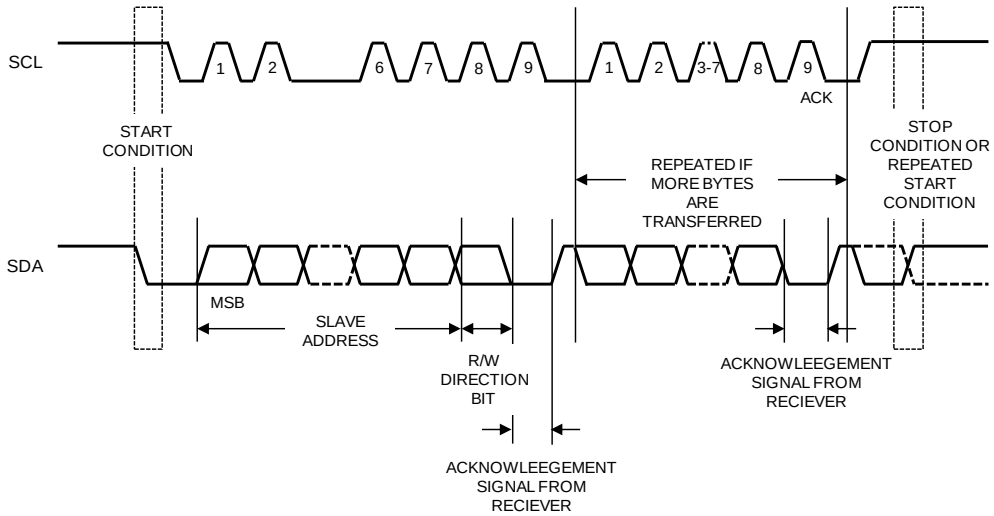


Figure 3. Data Transfer on I²C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The KTD2151 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 4 for Interface). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-KTD2151 address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the KTD2151 acknowledges the slave address + write bit, the master transmits a register address to the KTD2151. This sets the register pointer on the KTD2151. The master may then transmit zero or more bytes of data, with the KTD2151 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the KTD2151 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit KTD2151 address followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The KTD2151 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The KTD2151 must receive a “not acknowledge” to end a read.

The 7-bit slave device address is 0111110 binary (or 3Eh).

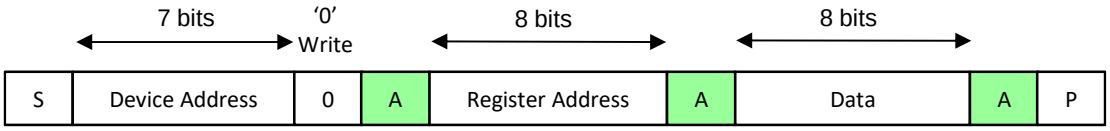


Figure 4. I²C Write – Slave Receiver Mode

where
S = START condition
P = STOP condition
Device Address = 0111110 (7 bits, MSB first)
Register Address = Reg0 - Reg3 address (8 bits)
Data = data to read or write (8 bits)
1 = Read command bit
0 = Write command bit
A = acknowledge (SDA low)
A* = not acknowledge (SDA high)

From master to slave

From slave to master

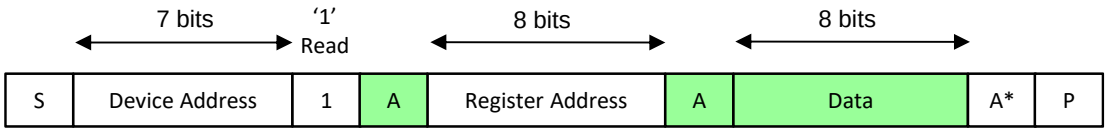


Figure 5. I²C Read – Slave Transmitter Mode

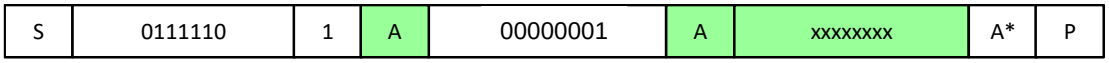


Figure 6. Example of Read Command

I²C Serial Bus Register Map

The device has three registers, Reg0, Reg1 and Reg3. Each register includes one data byte (8 bits) that can be written or read via the I²C interface.

VPOS: Reg 0	
0	VPOS OUTP Voltage Setting 4.0V to 6.3V in 100mV steps
1	
2	
3	
4	
5	Reserved*
6	
7	

VNEG: Reg 1	
0	VNEG OUTN Voltage Setting -4.0V to -6.3V in -100mV steps
1	
2	
3	
4	
5	Reserved*
6	
7	

Control 1: Reg 3	
0	Discharge OUTN
1	Discharge OUTP
2	Reserved*
3	
4	
5	
6	REG Offset Setting
7	Reserved*

* When writing to a register, always write a "0" in the reserved bits.

Reg#	Register Name	Address (Hex)	Default Value (Hex) (Reset Value)
Reg0	VPOS (positive voltage output) Register	00	0A
Reg1	VNEG (negative voltage output) Register	01	0A
Reg3	Control Register 1	03	03

VPOS Positive Voltage Output Setting Register (ADDR 00h, Default 0Ah or 0Ch)

V_{POS} Voltage Setting 4.0V to 6.3V in 100mV steps.
V_{POS} = 4.0V + (code * 100mV).

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Reserved			VPOS	VPOS	VPOS	VPOS	VPOS

OUTP Output Voltage			
Dec	Binary	Hex	Voltage (V)
0	0000 0000	00h	4.0
1	0000 0001	01h	4.1
2	0000 0010	02h	4.2
3	0000 0011	03h	4.3
4	0000 0100	04h	4.4
5	0000 0101	05h	4.5
6	0000 0110	06h	4.6
7	0000 0111	07h	4.7
8	0000 1000	08h	4.8
9	0000 1001	09h	4.9
10	0000 1010	0Ah	5.0
11	0000 1011	0Bh	5.1
12	0000 1100	0Ch	5.2
13	0000 1101	0Dh	5.3
14	0000 1110	0Eh	5.4
15	0000 1111	0Fh	5.5
16	0001 0000	10h	5.6
17	0001 0001	11h	5.7
18	0001 0010	12h	5.8
19	0001 0011	13h	5.9
20	0001 0100	14h	6.0
21	0001 0101	15h	6.1
22	0001 0110	16h	6.2
23	0001 0111	17h	6.3

VNEG Negative Voltage Output Setting Register (ADDR 01h, Default 0Ah or 0Ch)

V_{NEG} Voltage Setting -4.0V to -6.3V in 100mV steps.
V_{NEG} = -4.0V – (code * 100mV).

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Reserved			VNEG	VNEG	VNEG	VNEG	VNEG

OUTN Output Voltage			
Dec	Binary	Hex	Voltage (V)
0	0000 0000	00h	-4.0
1	0000 0001	01h	-4.1
2	0000 0010	02h	-4.2
3	0000 0011	03h	-4.3
4	0000 0100	04h	-4.4
5	0000 0101	05h	-4.5
6	0000 0110	06h	-4.6
7	0000 0111	07h	-4.7
8	0000 1000	08h	-4.8
9	0000 1001	09h	-4.9
10	0000 1010	0Ah	-5.0
11	0000 1011	0Bh	-5.1
12	0000 1100	0Ch	-5.2
13	0000 1101	0Dh	-5.3
14	0000 1110	0Eh	-5.4
15	0000 1111	0Fh	-5.5
16	0001 0000	10h	-5.6
17	0001 0001	11h	-5.7
18	0001 0010	12h	-5.8
19	0001 0011	13h	-5.9
20	0001 0100	14h	-6.0
21	0001 0101	15h	-6.1
22	0001 0110	16h	-6.2
23	0001 0111	17h	-6.3

Control Register 1 (ADDR 03h, Default 03h)

REG Offset Control

The REG output (output of the step-up controller) voltage is set to the following value:

$$V_{REG} = Max\ (V_{POS}, -V_{NEG}) + V_{OFFSET}$$

V_{REG} default value is the maximum of either (V_{POS} or $-V_{NEG}$) + 200mV.

For example, if V_{POS} = 5.1V and V_{NEG} = -5V, then the default V_{REG} = 5.1V + 0.2V = 5.3V

Fast Discharge

Allows quick discharge of the OUTP and OUTN nodes when the outputs are disabled. Default is ON (1).

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Reserved*	REG Offset Setting **0 = 200mV (Default)** 1 = 300mV	Reserved*				Discharge OUTP 0 = Disable **1 = Enable (Default)**	Discharge OUTN 0 = Disable **1 = Enable (Default)**

* When writing to the register, always write “0” in the reserved bits.
For example, to set the REG offset to 300mV and Discharge OUTP/OUTN enable, write 0x43 in the Control register.

Capacitor Selection

Small size X5R or X7R ceramic capacitors are recommended for the KTD2151 application. 4.7µF capacitors are suggested for the input VIN, and for the outputs REG, OUTP, OUTN. The input capacitor should be placed as close as possible to the input pin and the PGND pin of the KTD2151. For better input voltage filtering, this value can be increased. For the output capacitors, higher capacitor values can be used to improve the load transient response. For higher output current up to 80mA, the REG and OUTN output capacitors can be increased to 10µF.

The capacitor data sheet determines what value of capacitor is required to guarantee a minimum capacitance value for a given bias voltage and over operating temperature.

Capacitor	Comments
2.2µF/16V	C_{FLY}
4.7µF/16V	C_{IN}, C_{POS}, C_{NEG}, C_{REG}
10µF/16V	C_{NEG}, C_{REG}

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Inductor Selection

An inductor in the range of 2.2µH to 10µH with low DCR can be selected for the boost converter. To estimate the inductance required for applications, calculate the maximum input average current as the following

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

where η is the converter efficiency and can be approximated as 90% for the typical case. In order to have smaller current ripple (to improve efficiency and minimize output voltage ripple), larger inductance will be required. If inductor ripple current needs to be less than 40% of the average input current, then

$$\Delta I_L = \frac{V_{IN} \cdot D \cdot T_S}{L} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where duty cycle can be estimated as

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Then

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN}) \cdot T_S}{L \cdot V_{OUT}} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Therefore the inductance can be calculated as

$$L \ge \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{40\% \cdot V_{OUT}^2 \cdot I_{OUT(MAX)} \cdot f_S}$$

where f_S is the switching frequency of the boost converter.

For smartphone applications with load currents up to 40mA per outputs, a 4.7µH inductor is recommended. For tablet applications with higher load currents up to 80mA per outputs, a 2.2µH inductor is recommended.

Inductor Part Number	Value (µH)	DCR (Ω)	Saturation Current (A)	Dimensions (mm)	Manufacturer
LPS3015-472ML	4.7	0.20 max	1.3	3 × 3 × 1.5	Coilcraft
LPS3015-222ML	2.2	0.11 max	2.0	3 × 3 × 1.5	Coilcraft
MIPS2520D2R2	2.0	0.11 typ.	1.1	2.5 x 2 x 1	FDK

CSP PC Board Layout

PCB layout is very important for high frequency switching regulators in order to keep the loop stable and minimize noise. A small 4.7µF ceramic capacitor CIN is recommended to be placed close to the IC VIN pin (C1) to get the best decoupling. The boost output capacitor CREG should located close the REG pin (E2) and with a direct contact to PGND pin (E1). The two REG pins must be tied together. The output (OUTP, OUTN) capacitors should also be located close to their respective pins (A2, E3). To minimize switching loss and EMI noise, the inductor L1 must adjacent to the SW pin (D1), and the charge pump capacitor C_FLY should be next to the CFLY1/CFLY2 pins. The AGND pin (D2) is connected to the GND plane underneath using a micro via. The power GND plane should be uninterrupted, if possible. The I2C lines, SDA and SCL, are routed using micro vias. The KTD2151 CSP recommended layout is shown in Figure 7.

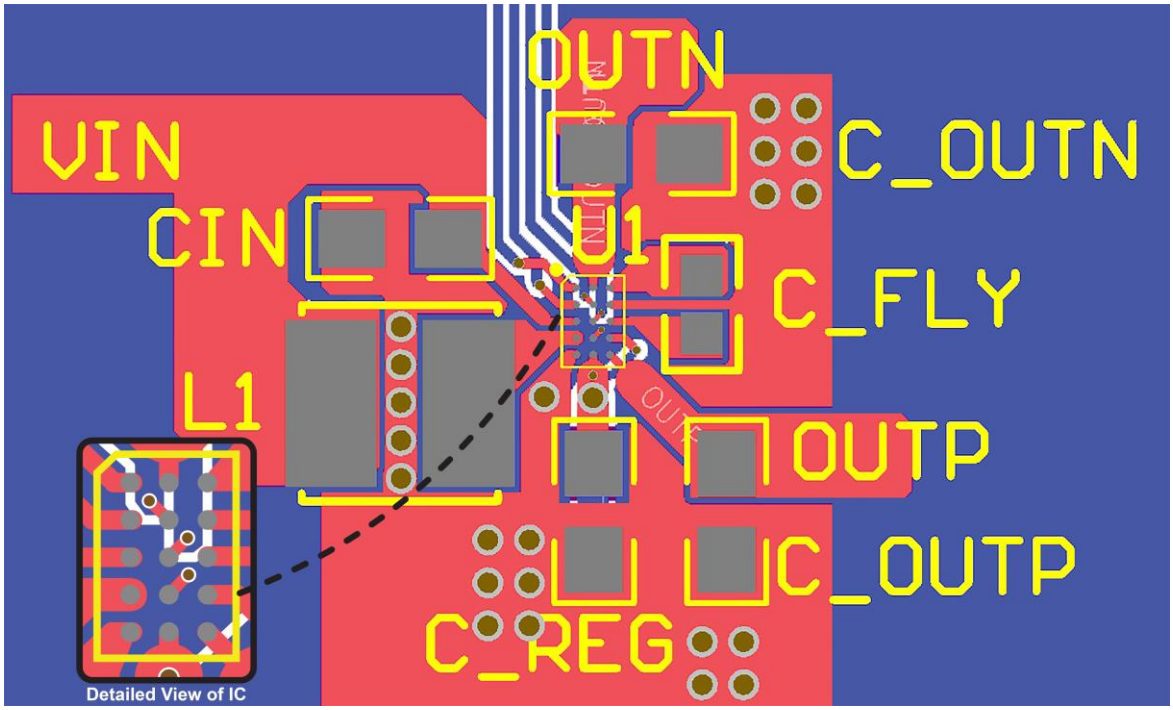
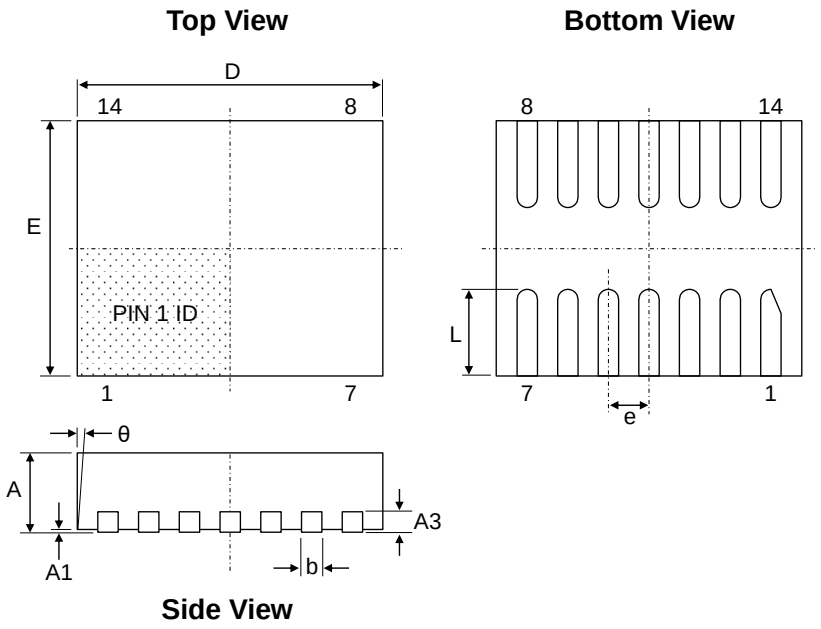


Figure 7. CSP Recommended PCB Layout

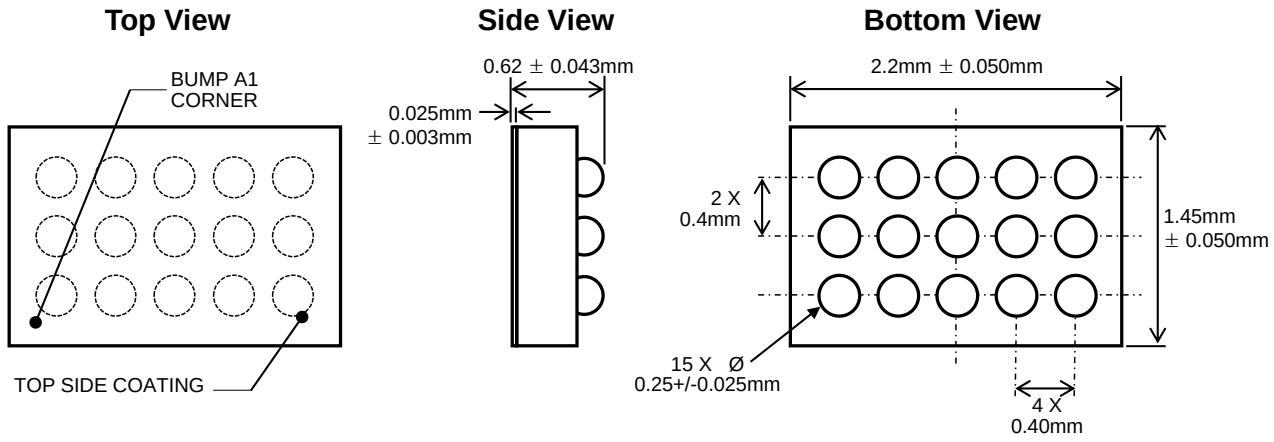
Packaging Information

TDFN2.5x3-14



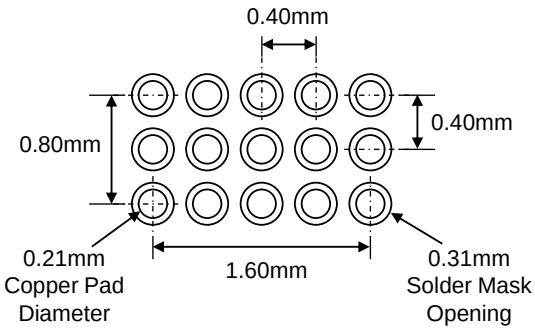
Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3	0.175	0.20	0.225
D	2.9	3.0	3.1
E	2.4	2.5	2.6
e	0.40 TYP		
b	0.15	0.20	0.25
L	0.7	0.75	0.8
θ	0°	2°	4°

WLCSP-15



Recommended Footprint

(NSMD Pad Type)



* Dimensions are in millimeters.

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Kinetic Technologies:

KTD2151EUO-TR