

XS3A4051

Single low-ohmic 8-channel analog switch

Rev. 2 — 31 July 2024

Product data sheet

1. General description

The XS3A4051 is a low-ohmic 8-channel analog switch, suitable for use as an analog or digital multiplexer/demultiplexer. The XS3A4051 has three digital select inputs (S1 to S3), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). All eight switches share an enable input (E). A HIGH on E causes all switches into the high impedance OFF-state, independent of Sn.

Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC} . This makes it possible for the XS3A4051 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The XS3A4051 allows signals with amplitude up to V_{CC} to be transmitted from Z to Yn or from Yn to Z. Its low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensures minimal attenuation and distortion of transmitted signals.

2. Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
 - 1.6 Ω (typical) at $V_{CC} = 1.4$ V
 - 1.0 Ω (typical) at $V_{CC} = 1.65$ V
 - 0.55 Ω (typical) at $V_{CC} = 2.3$ V
 - 0.50 Ω (typical) at $V_{CC} = 2.7$ V
 - 0.50 Ω (typical) at $V_{CC} = 4.3$ V
- Break-before-make switching
- High noise immunity
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD78 Class II Level A
- Low-switching threshold levels
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
 - CDM ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
 - IEC61000-4-2 contact discharge exceeds 8000 V for switch ports
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

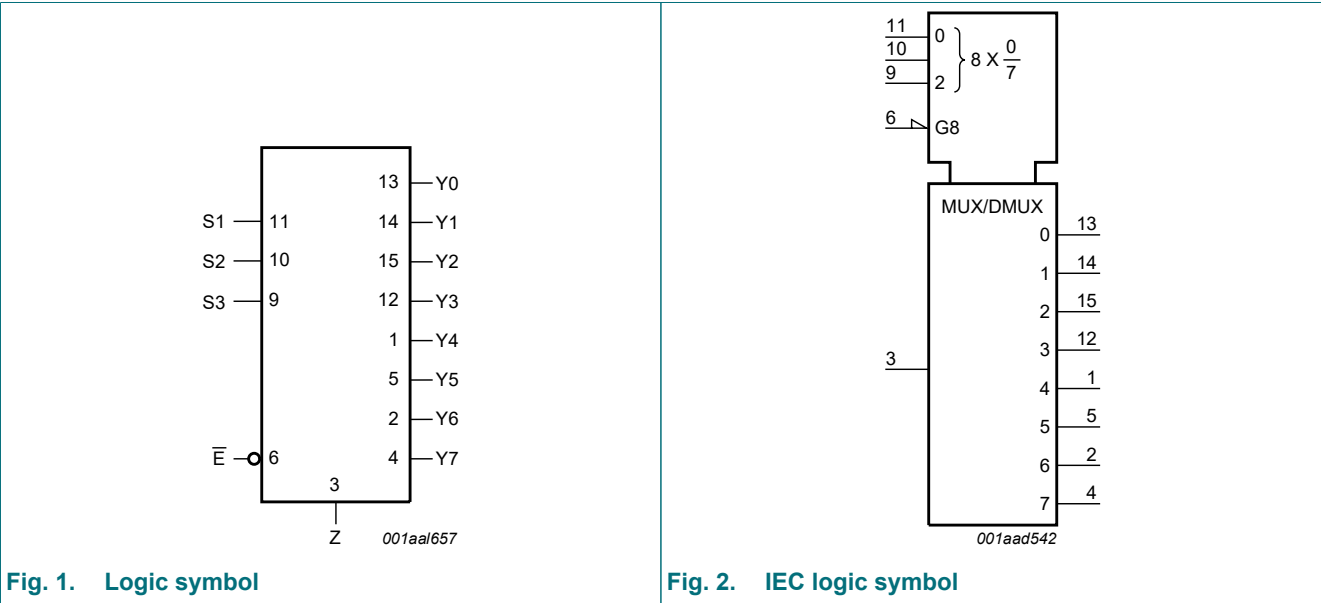
- Appliances
- Communication Systems
- Medical Equipment
- Analog Sensor Monitoring
- Audio Routing/Switching
- Test and Measurement

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
XS3A4051PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram



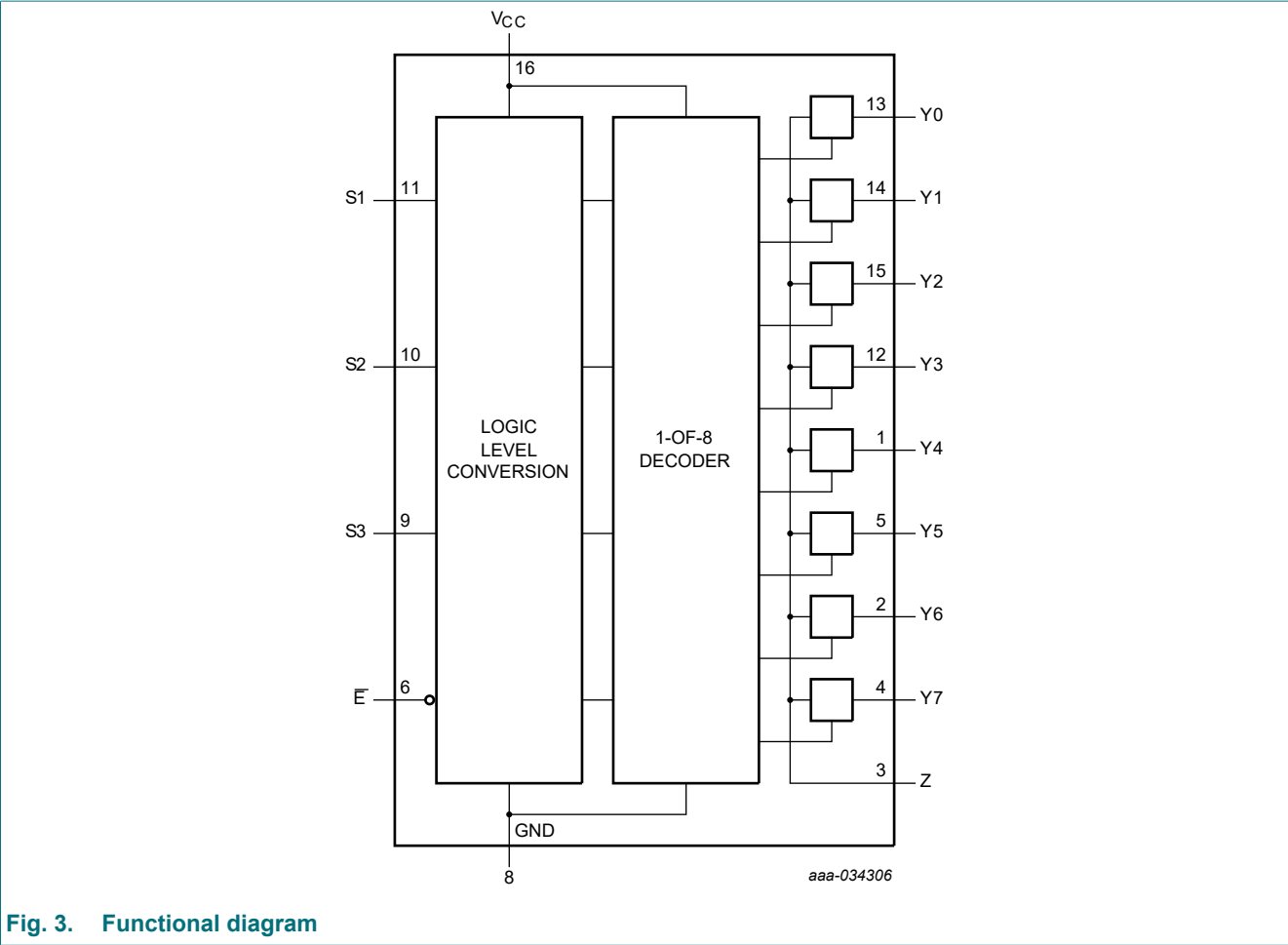
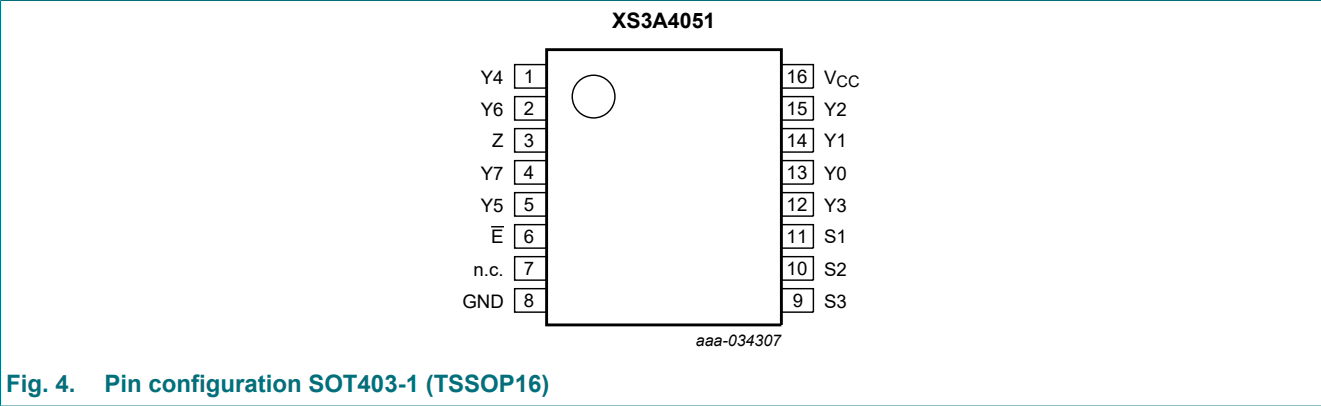


Fig. 3. Functional diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{E}$	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground supply voltage
S1, S2, S3	11, 10, 9	select input
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	13, 14, 15, 12, 1, 5, 2, 4	independent input or output
Z	3	common output or input
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table
H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Channel ON
E	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	S _n and $\overline{E}$ inputs [1]	-0.5	+4.6	V
V _{SW}	switch voltage	[2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±50	mA
I _{SW}	switch current	V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; source or sink current	-	±350	mA
		V _{SW} > -0.5 V or V _{SW} < V _{CC} + 0.5 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current	-	±500	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

- [1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.
[3] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.4	4.3	V
V _I	input voltage	Sn and $\bar{E}$ inputs	0	4.3	V
V _{SW}	switch voltage	[1]	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	Sn and $\bar{E}$ inputs; V _{CC} = 1.4 V to 4.3 V [2]	-	200	ns/V

- [1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.
- [2] Applies to control signal levels.

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	0.9	-	V
		V _{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	0.9	-	V
		V _{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	1.1	-	V
		V _{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	1.3	-	V
		V _{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	1.4	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	-	0.3	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	-	0.3	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.4	-	0.4	-	0.4	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	-	0.6	V
I _I	input leakage current	Sn and $\bar{E}$ input; V _I = GND to 4.3 V; V _{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	-	±1	μA
I _{S(OFF)}	OFF-state leakage current	Y1 and Y2 port; see Fig. 5								
		V _{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	-	±500	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	-	±500	nA
I _{S(ON)}	ON-state leakage current	Z port; see Fig. 6								
		V _{CC} = 1.4 V to 3.6 V	-	-	±15	-	±150	-	±1500	nA
		V _{CC} = 3.6 V to 4.3 V	-	-	±20	-	±150	-	±1500	nA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{SW} = GND or V _{CC}								
		V _{CC} = 3.6 V	-	-	100	-	690	-	6000	nA
		V _{CC} = 4.3 V	-	-	150	-	800	-	7000	nA

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	$V_{SW} = GND \text{ or } V_{CC}$								
		$V_I = 2.6 \text{ V}; V_{CC} = 4.3 \text{ V}$	-	2.0	4.0	-	7	-	7	μA
		$V_I = 2.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	0.35	0.7	-	1	-	1	μA
		$V_I = 1.8 \text{ V}; V_{CC} = 4.3 \text{ V}$	-	7.0	10.0	-	15	-	15	μA
		$V_I = 1.8 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	2.5	4.0	-	5	-	5	μA
		$V_I = 1.8 \text{ V}; V_{CC} = 2.5 \text{ V}$	-	50	200	-	300	-	500	nA
C_I	input capacitance	Sn and $\bar{E}$ input	-	1.0	-	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	35	-	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	350	-	-	-	-	-	pF

Table 7. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Fig. 8 to Fig. 14.

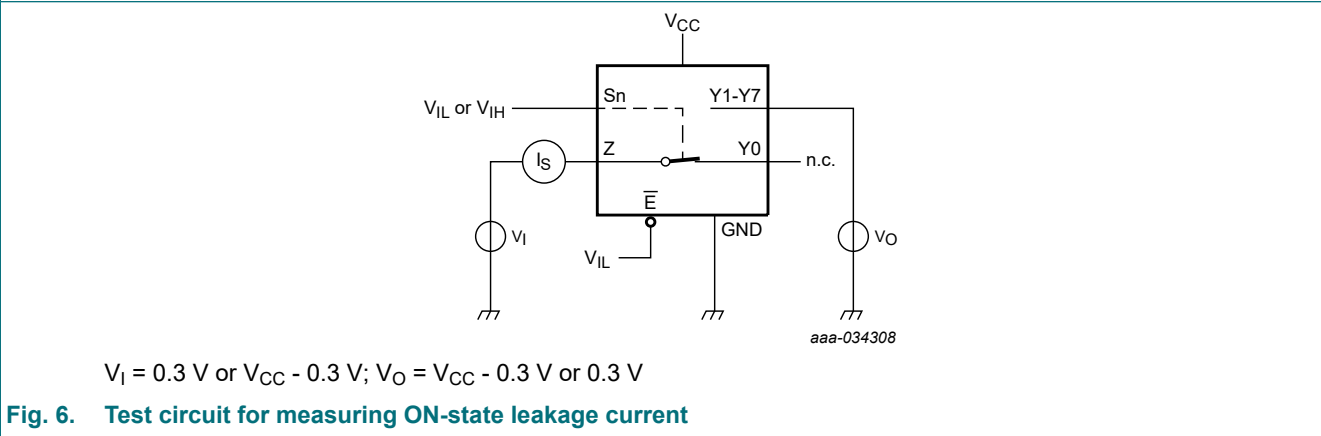
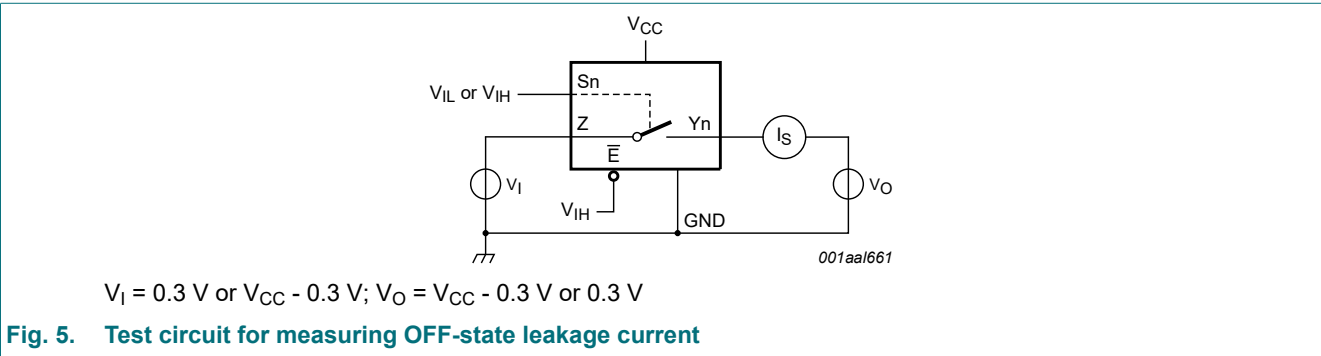
Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_I = GND \text{ to } V_{CC}; I_{SW} = 100 \text{ mA}$; see Fig. 7						
		$V_{CC} = 1.4 \text{ V}$	-	1.6	3.7	-	4.1	Ω
		$V_{CC} = 1.65 \text{ V}$	-	1.0	1.6	-	1.7	Ω
		$V_{CC} = 2.3 \text{ V}$	-	0.55	0.8	-	0.9	Ω
		$V_{CC} = 2.7 \text{ V}$	-	0.5	0.75	-	0.9	Ω
		$V_{CC} = 4.3 \text{ V}$	-	0.5	0.75	-	0.9	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_I = GND \text{ to } V_{CC}; I_{SW} = 100 \text{ mA}$ [2]						
		$V_{CC} = 1.4 \text{ V}; V_{SW} = 0.4 \text{ V}$	-	0.07	0.30	-	0.30	Ω
		$V_{CC} = 1.65 \text{ V}; V_{SW} = 0.5 \text{ V}$	-	0.07	0.20	-	0.30	Ω
		$V_{CC} = 2.3 \text{ V}; V_{SW} = 0.7 \text{ V}$	-	0.05	0.10	-	0.13	Ω
		$V_{CC} = 2.7 \text{ V}; V_{SW} = 0.8 \text{ V}$	-	0.05	0.10	-	0.13	Ω
		$V_{CC} = 4.3 \text{ V}; V_{SW} = 0.8 \text{ V}$	-	0.05	0.10	-	0.13	Ω
$R_{ON(flat)}$	ON resistance (flatness)	$V_I = GND \text{ to } V_{CC}; I_{SW} = 100 \text{ mA}$ [3]						
		$V_{CC} = 1.4 \text{ V}$	-	1.0	3.3	-	3.6	Ω
		$V_{CC} = 1.65 \text{ V}$	-	0.5	1.2	-	1.3	Ω
		$V_{CC} = 2.3 \text{ V}$	-	0.15	0.3	-	0.35	Ω
		$V_{CC} = 2.7 \text{ V}$	-	0.13	0.3	-	0.35	Ω
		$V_{CC} = 4.3 \text{ V}$	-	0.2	0.4	-	0.45	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

10.1. Test circuits and graphs



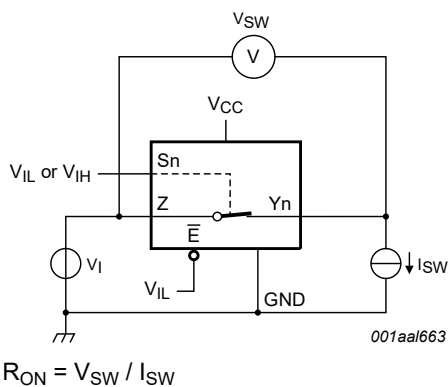


Fig. 7. Test circuit for measuring ON resistance

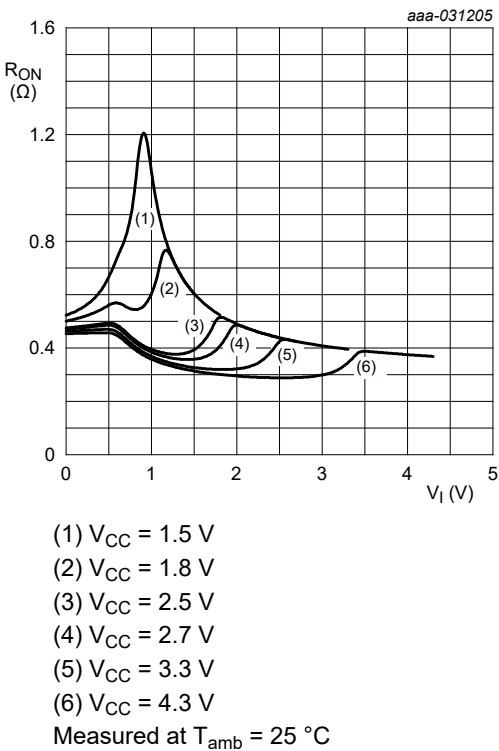


Fig. 8. Typical ON resistance as a function of input voltage

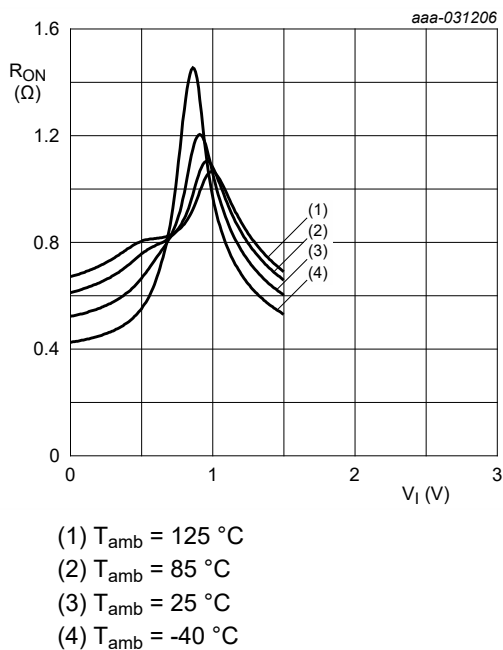


Fig. 9. ON resistance as a function of input voltage; $V_{CC} = 1.5\text{ V}$

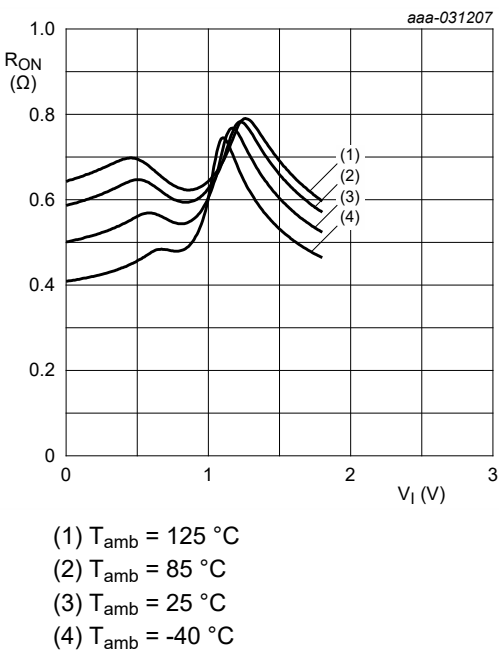


Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 1.8\text{ V}$

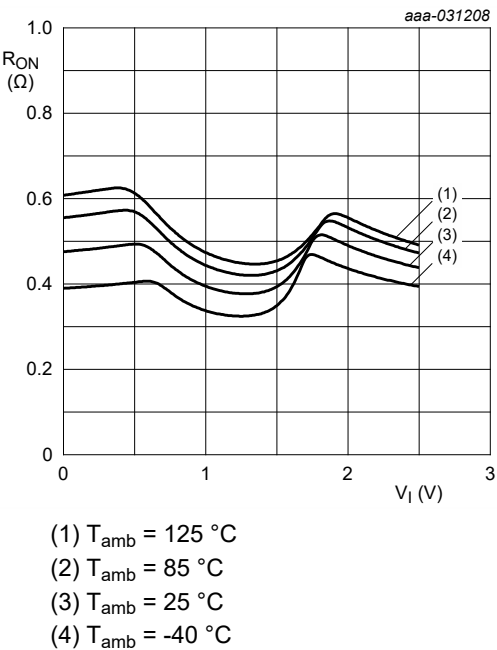


Fig. 11. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}$

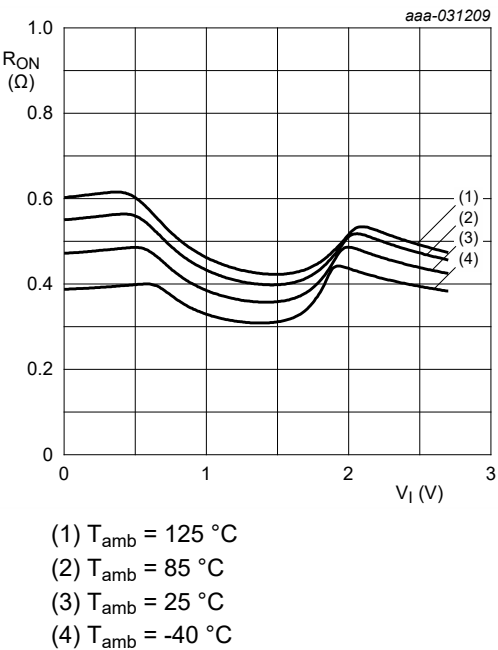


Fig. 12. ON resistance as a function of input voltage;
 $V_{CC} = 2.7\text{ V}$

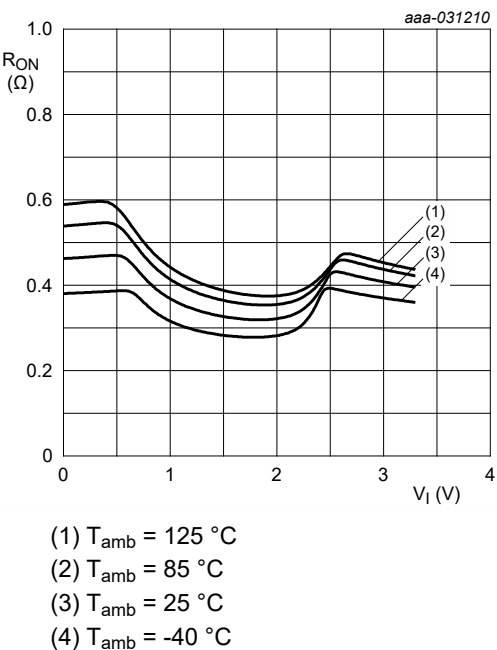


Fig. 13. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}$

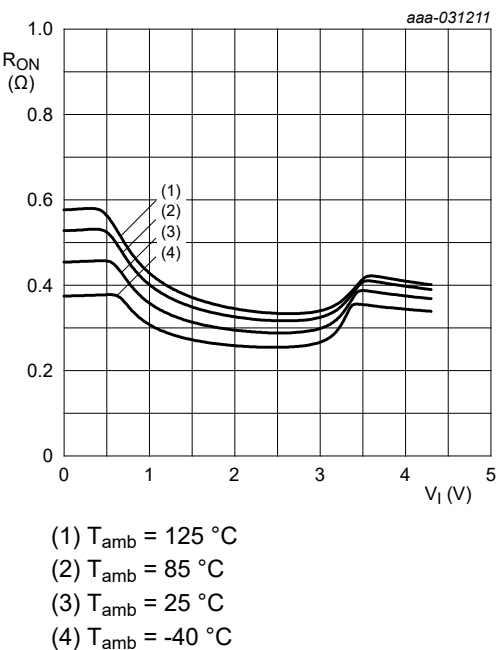


Fig. 14. ON resistance as a function of input voltage;
 $V_{CC} = 4.3\text{ V}$

11. Dynamic characteristics

Table 8. Dynamic characteristics
 At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 17.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = –40 °C to +85 °C		T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{en}	enable time	$\overline{E}$, Sn to Z or Yn; see Fig. 15								
		V _{CC} = 1.4 V to 1.6 V	-	50	110	-	120	-	120	ns
		V _{CC} = 1.65 V to 1.95 V	-	36	70	-	80	-	90	ns
		V _{CC} = 2.3 V to 2.7 V	-	24	45	-	50	-	55	ns
		V _{CC} = 2.7 V to 3.6 V	-	22	40	-	45	-	50	ns
		V _{CC} = 3.6 V to 4.3 V	-	22	40	-	45	-	50	ns
t _{dis}	disable time	$\overline{E}$, Sn or Yn; see Fig. 15								
		V _{CC} = 1.4 V to 1.6 V	-	32	90	-	90	-	90	ns
		V _{CC} = 1.65 V to 1.95 V	-	20	55	-	60	-	65	ns
		V _{CC} = 2.3 V to 2.7 V	-	12	25	-	30	-	35	ns
		V _{CC} = 2.7 V to 3.6 V	-	10	20	-	25	-	30	ns
		V _{CC} = 3.6 V to 4.3 V	-	10	20	-	25	-	30	ns
t _{b-m}	break-before-make time	see Fig. 16 [2]								
		V _{CC} = 1.4 V to 1.6 V	-	19	-	9	-	9	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	17	-	7	-	7	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	13	-	4	-	4	-	ns
		V _{CC} = 2.7 V to 3.6 V	-	10	-	3	-	3	-	ns
		V _{CC} = 3.6 V to 4.3 V	-	10	-	2	-	2	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.
 [2] Break-before-make guaranteed by design.

11.1. Waveforms and test circuit

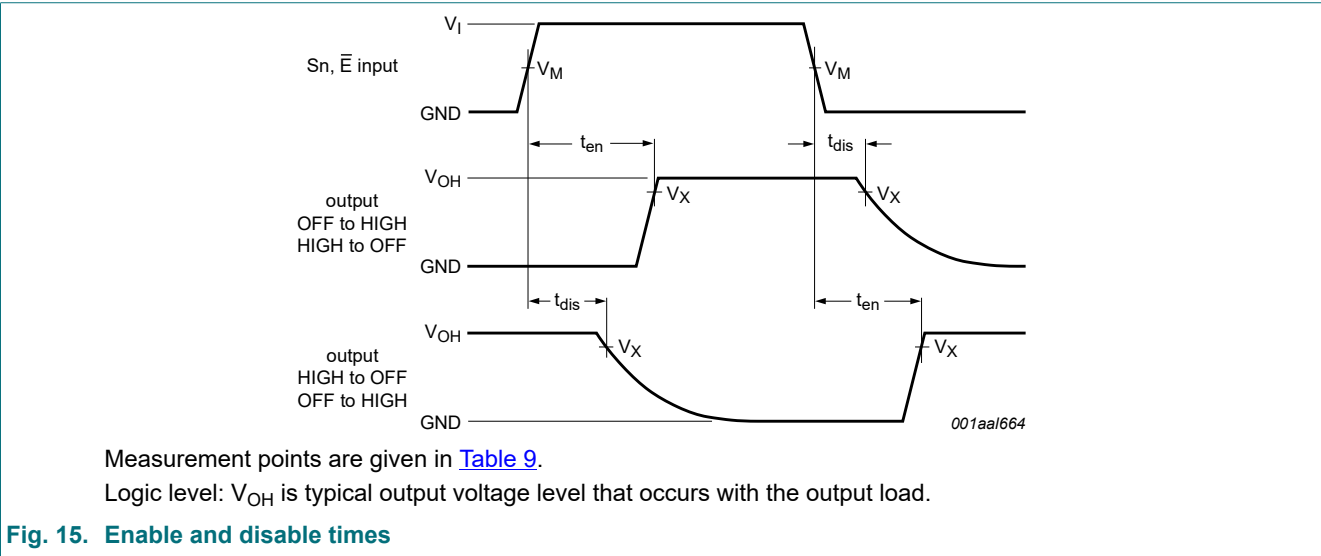


Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

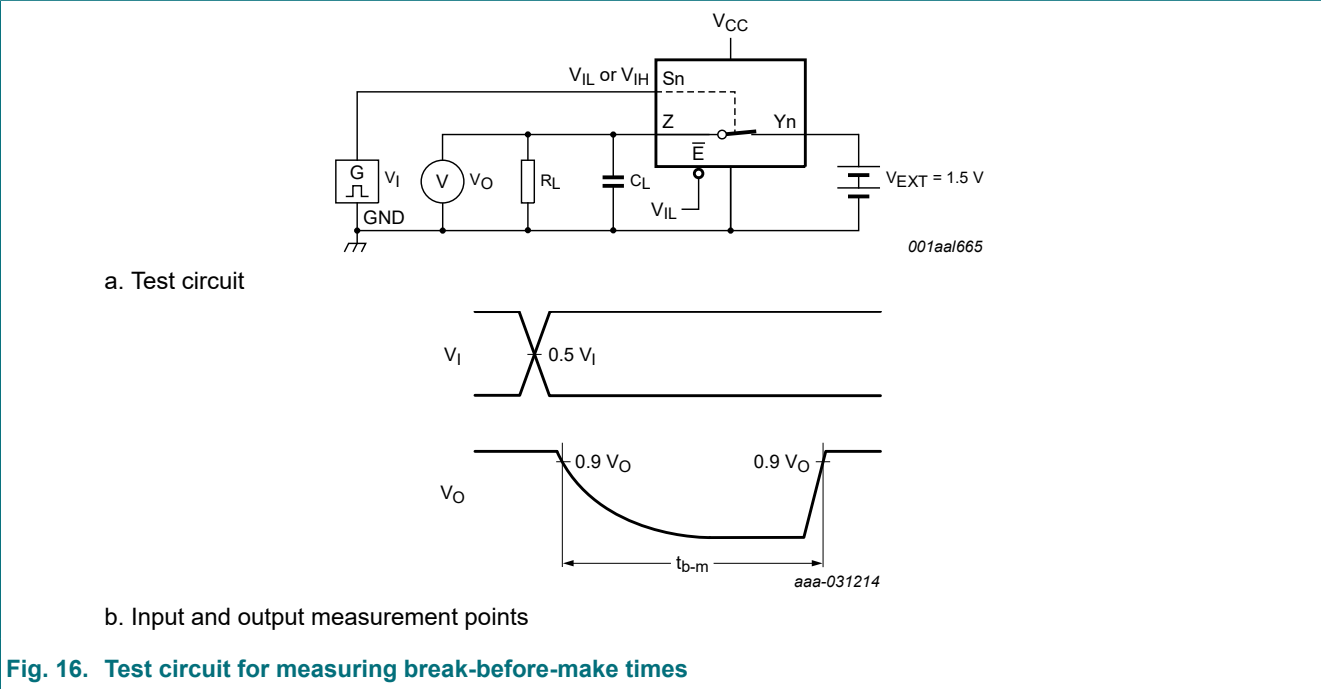


Fig. 16. Test circuit for measuring break-before-make times

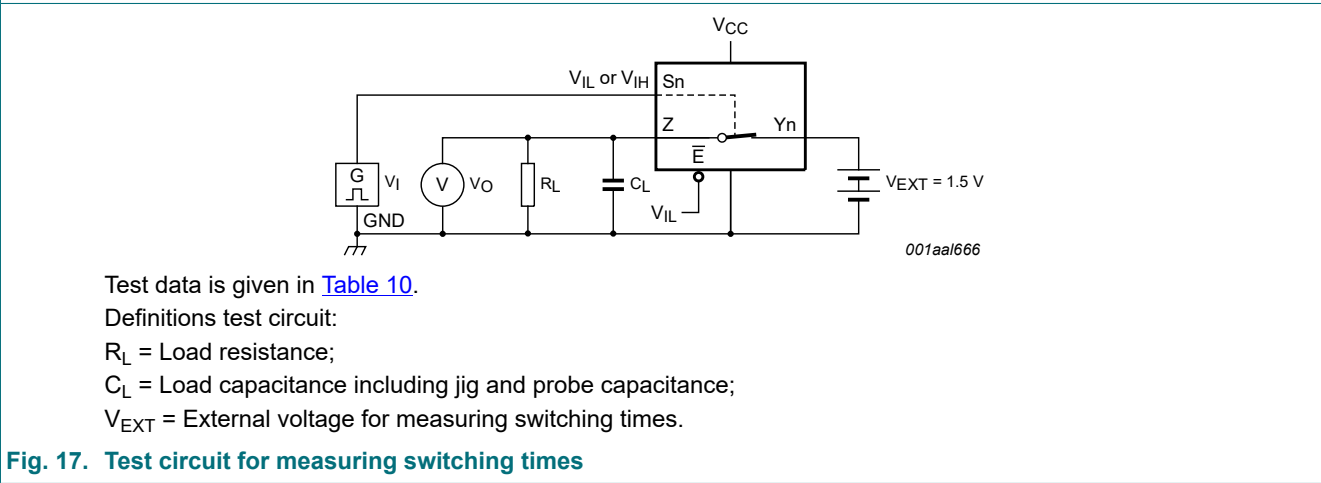


Fig. 17. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	$\leq 2.5 \text{ ns}$	35 pF	50 Ω

11.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
 V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
THD	total harmonic distortion	f_i = 20 Hz to 20 kHz; R_L = 32 Ω ; see Fig. 18 [1]				
		V_{CC} = 1.4 V; V_I = 1 V (p-p)	-	0.17	-	%
		V_{CC} = 1.65 V; V_I = 1.2 V (p-p)	-	0.10	-	%
		V_{CC} = 2.3 V; V_I = 1.5 V (p-p)	-	0.05	-	%
		V_{CC} = 2.7 V; V_I = 2 V (p-p)	-	0.04	-	%
		V_{CC} = 4.3 V; V_I = 2 V (p-p)	-	0.01	-	%
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω ; see Fig. 19 [1]				
		V_{CC} = 1.4 V to 4.3 V	-	15	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 100 kHz; R_L = 50 Ω ; see Fig. 20 [1]				
		V_{CC} = 1.4 V to 4.3 V	-	-90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 50 Ω ; see Fig. 21 [1]				
		V_{CC} = 1.4 V to 3.6 V	-	0.2	-	V
		V_{CC} = 3.6 V to 4.3 V	-	0.3	-	V
Xtalk	crosstalk	between switches; f_i = 100 kHz; R_L = 50 Ω ; see Fig. 22 [1]				
		V_{CC} = 1.4 V to 4.3 V	-	-90	-	dB
Q_{inj}	charge injection	f_i = 1 MHz; C_L = 0.1 nF; R_L = 1 M Ω ; V_{gen} = 0 V; R_{gen} = 0 Ω ; see Fig. 23 [1]				
		V_{CC} = 1.5 V	-	3	-	pC
		V_{CC} = 1.8 V	-	4	-	pC
		V_{CC} = 2.5 V	-	6	-	pC
		V_{CC} = 3.3 V	-	9	-	pC
		V_{CC} = 4.3 V	-	15	-	pC

[1] f_i is biased at 0.5V_{CC}.

11.3. Additional test circuits

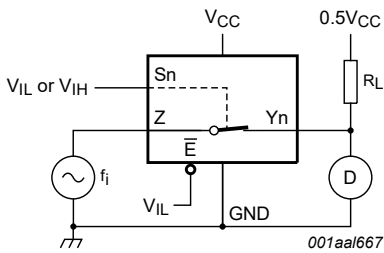
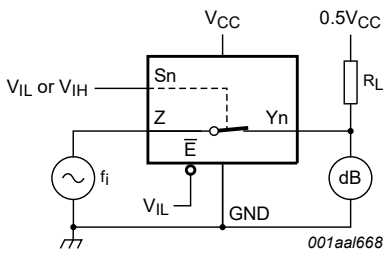
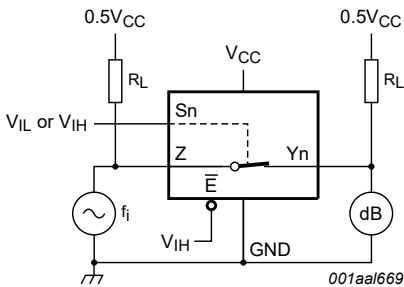


Fig. 18. Test circuit for measuring total harmonic distortion



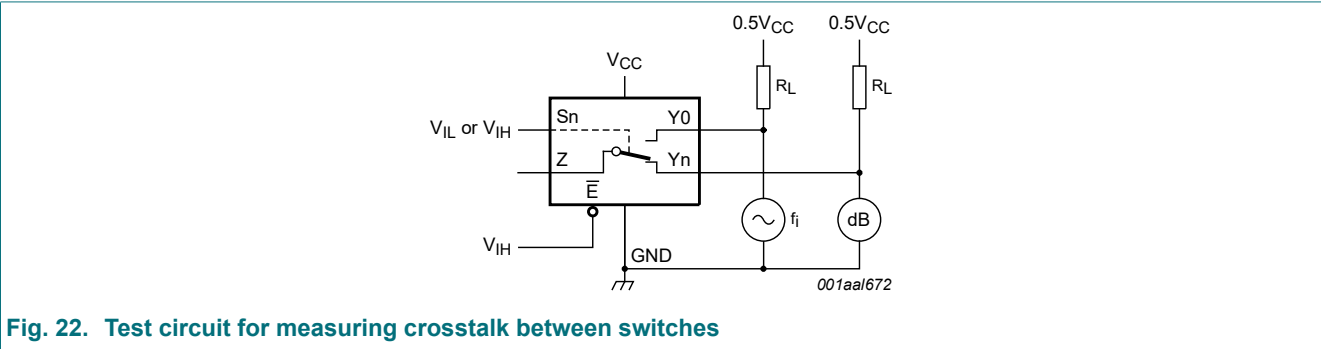
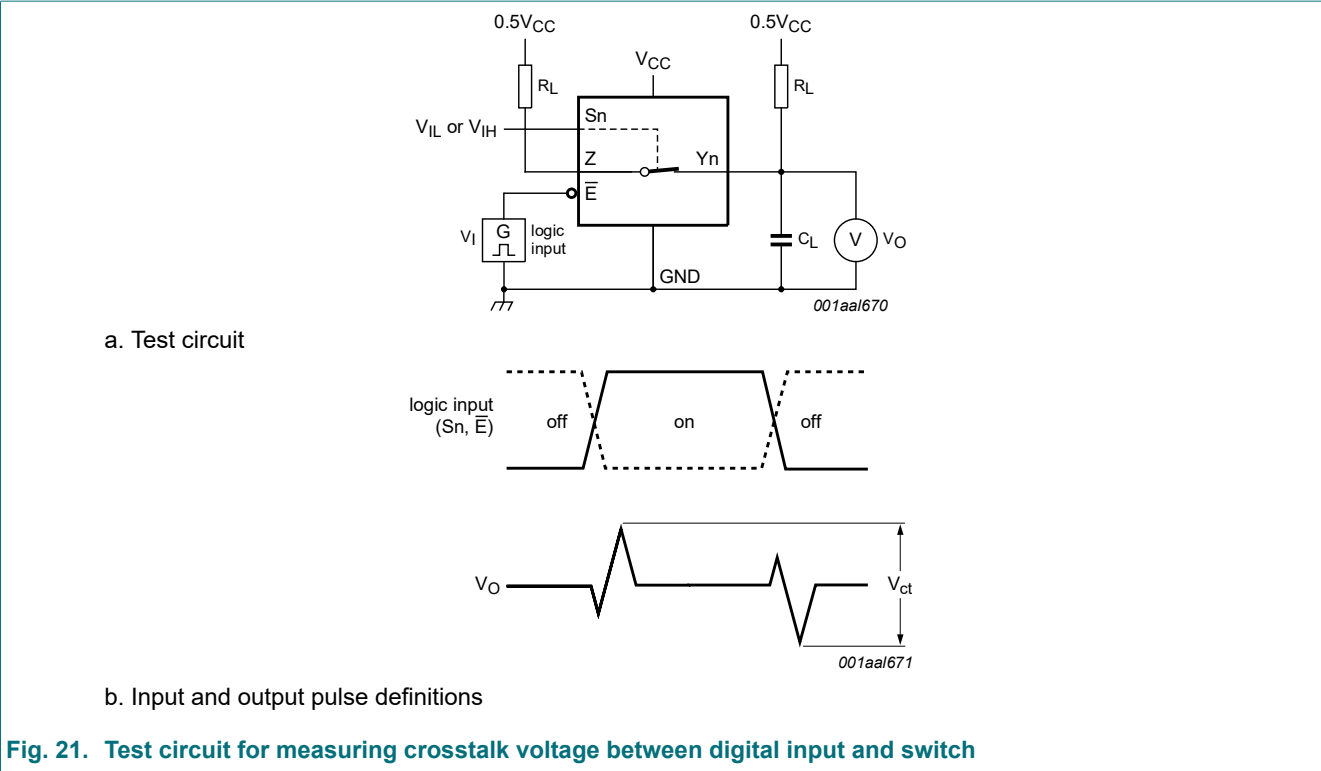
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.
 $R_S = R_L = 50 \, \Omega$ (standard 50 Ω system).

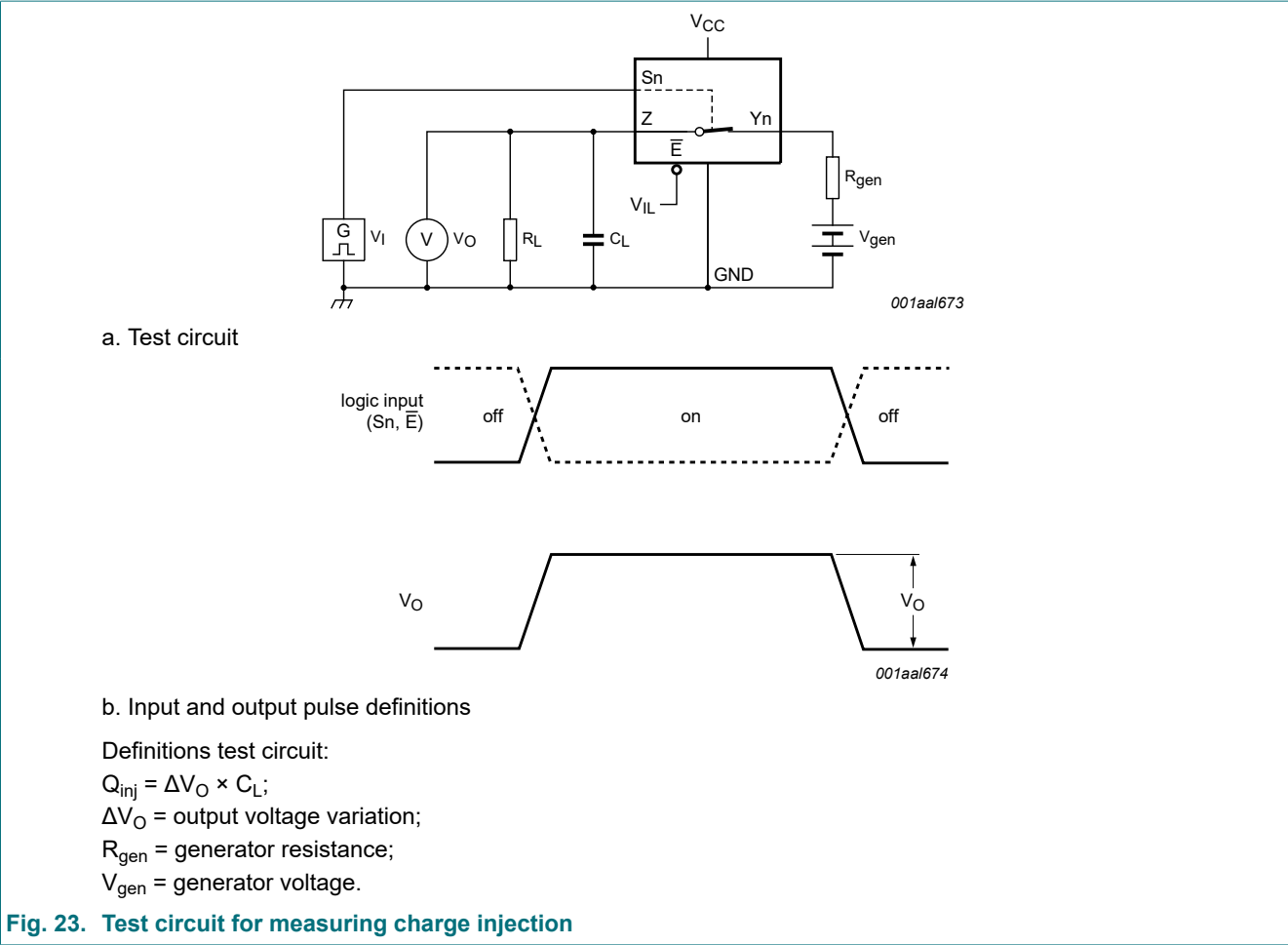
Fig. 19. Test circuit for measuring the frequency response when channel is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 20. Test circuit for measuring isolation (OFF-state)





12. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

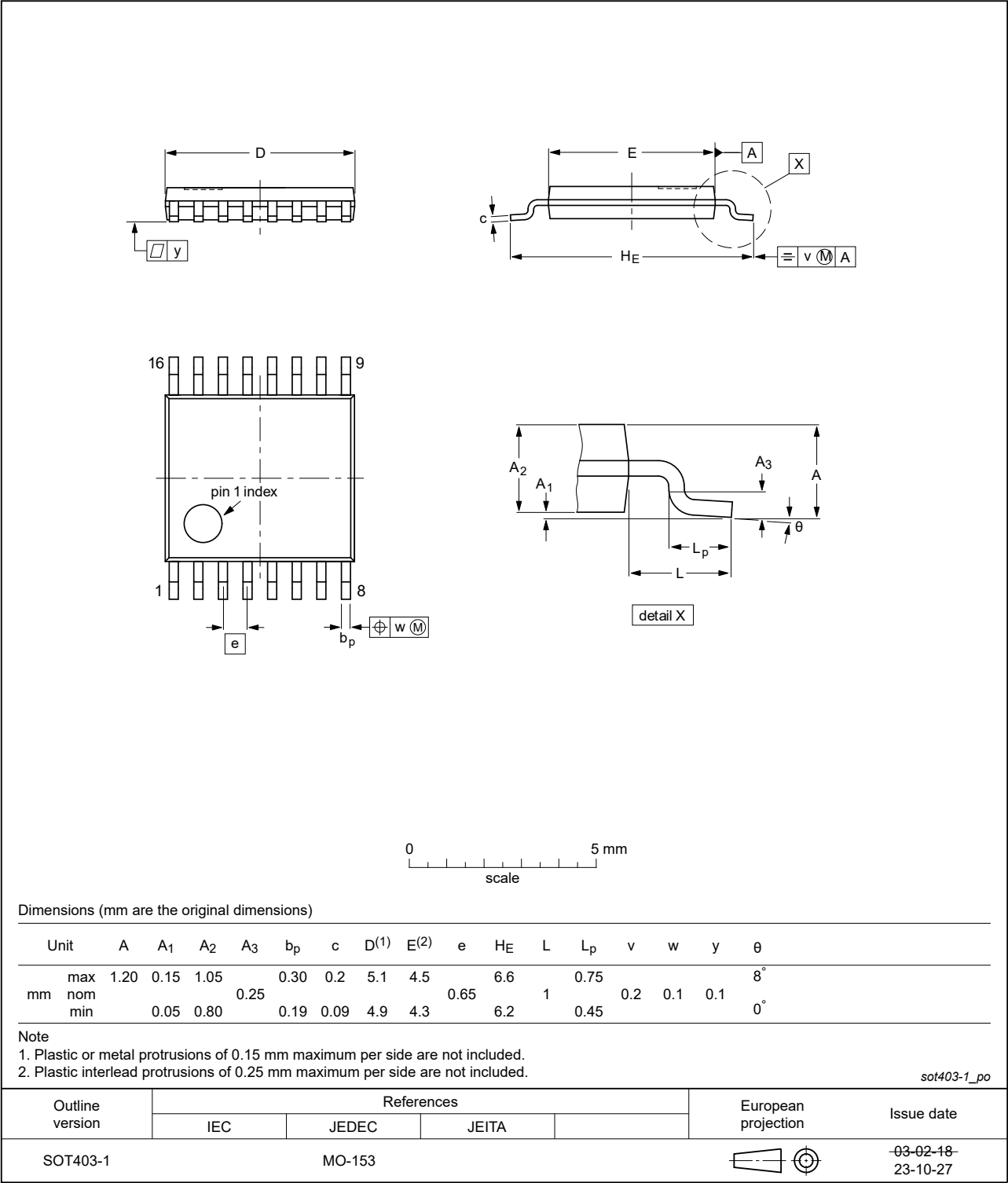


Fig. 24. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
XS3A4051 v.2	20240731	Product data sheet	-	XS3A4051 v.1
Modifications:	Fig. 24: Aligned TSSOP package outline drawing to JEDEC MO-153			
XS3A4051 v.1	20220211	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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