



# PXN5R4-30QL

30 V, N-channel Trench MOSFET

15 April 2021

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic-level compatible
- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)

## 3. Applications

- DC-to-DC converters
- Battery management
- Low-side load-switch
- Switching circuits

## 4. Quick reference data

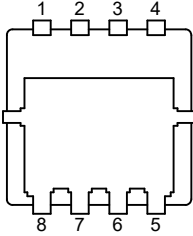
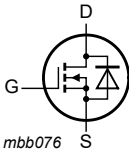
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-	30	V
V <sub>GS</sub>	gate-source voltage			-20	-	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-	22	A
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 14.2 A; T <sub>j</sub> = 25 °C		-	4.6	5.4	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 12.3 A; T <sub>j</sub> = 25 °C		-	5.8	7.2	mΩ
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.3 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C		-	11.6	17.4	nC

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN5R4-30QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN5R4-30QL	8AP

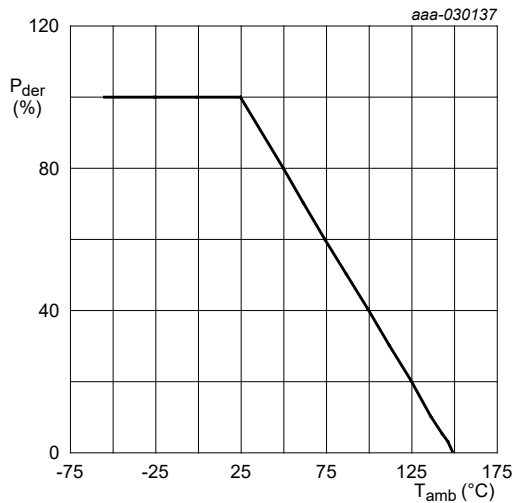
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

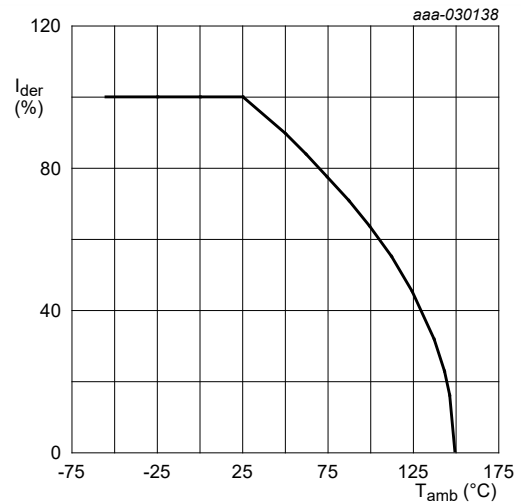
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	30	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	22	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	14	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	9	A
		V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C		-	66	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	101	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	4.5	W
		T <sub>amb</sub> = 25 °C	[1]	-	1.8	W
		T <sub>sp</sub> = 25 °C		-	39	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1.8	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^{\circ}\text{C})} \times 100\%$$

**Fig. 1. Normalized total power dissipation as a function of ambient temperature**



$$I_{der} = \frac{I_D}{I_D(25^{\circ}\text{C})} \times 100\%$$

**Fig. 2. Normalized continuous drain current as a function of ambient temperature**

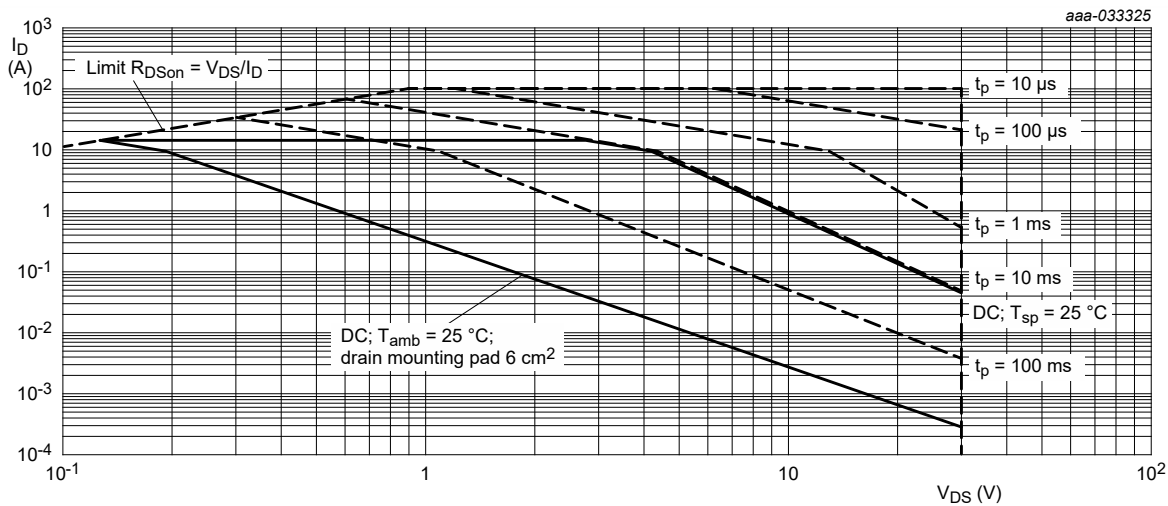


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	145	185	K/W
			[2]	-	55	70	K/W
		in free air; $t \leq 5$ s	[2]	-	23	28	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	2.3	3.2	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

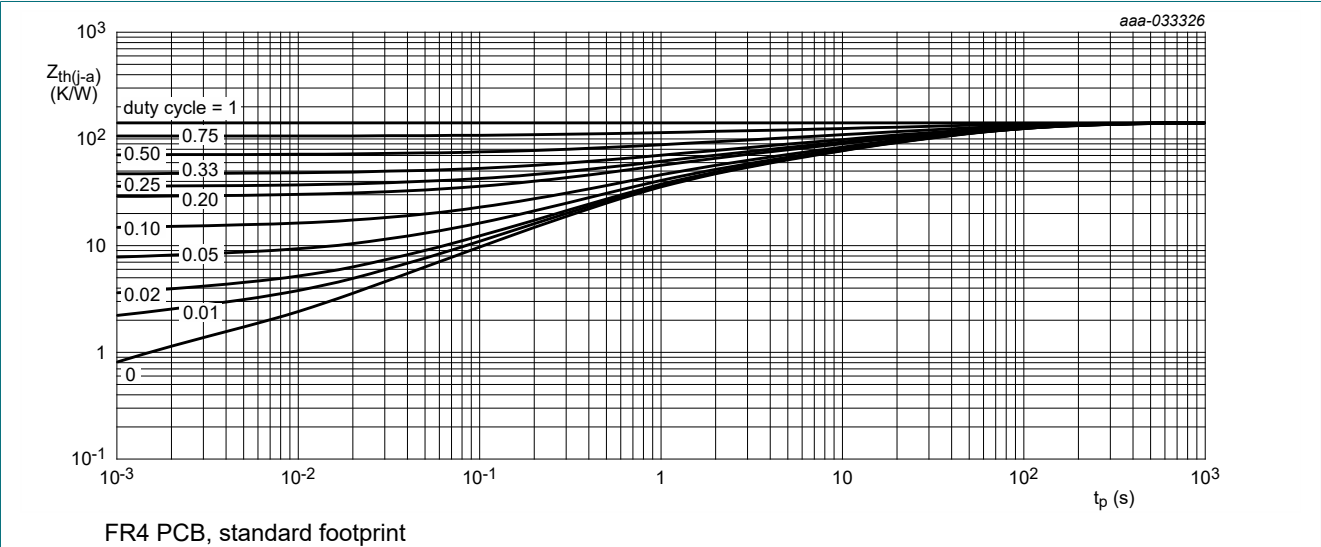


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

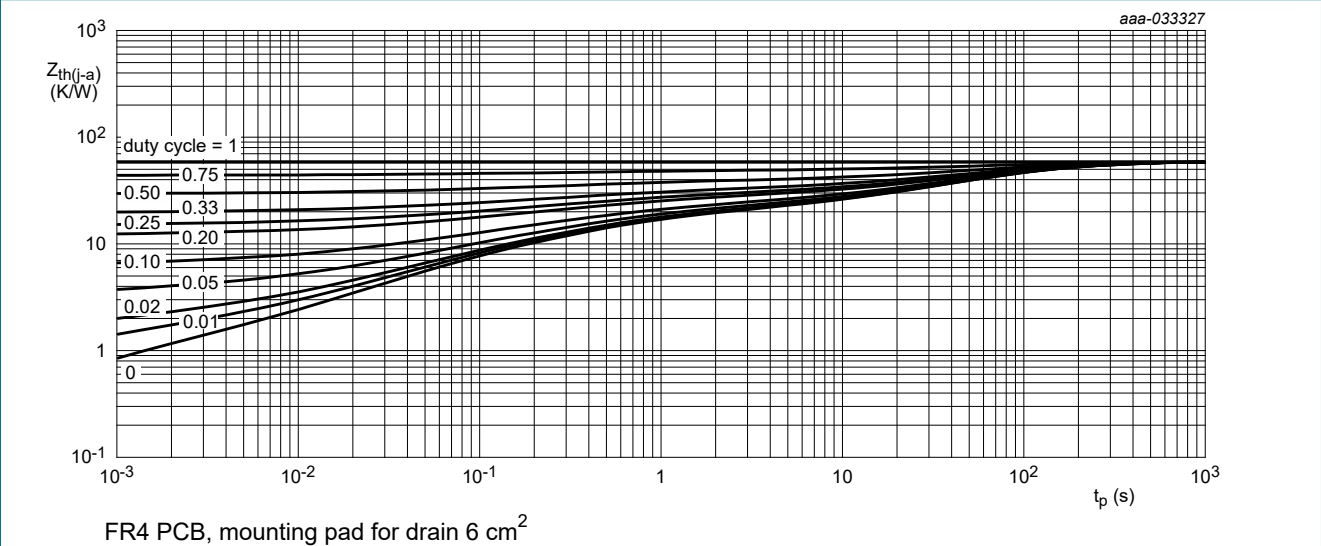


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		30	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		1	1.6	2.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 14.2 A; T <sub>j</sub> = 25 °C		-	4.6	5.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 14.2 A; T <sub>j</sub> = 150 °C		-	7.5	8.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 12.3 A; T <sub>j</sub> = 25 °C		-	5.8	7.2	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 14.2 A; T <sub>j</sub> = 25 °C		-	37	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	0.6	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 14.2 A; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C		-	24.2	36.3	nC
		V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.3 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C		-	11.6	17.4	nC
Q <sub>GS</sub>	gate-source charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.3 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C		-	4	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge			-	2	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge			-	2	-	nC
Q <sub>GD</sub>	gate-drain charge			-	3.3	-	nC
V <sub>GSpl</sub>	gate-source plateau voltage	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.3 A; T <sub>j</sub> = 25 °C		-	2.6	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	1600	-	pF
C <sub>oss</sub>	output capacitance			-	270	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	98	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.3 A; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C		-	9	-	ns
t <sub>r</sub>	rise time			-	13	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	11	-	ns
t <sub>f</sub>	fall time			-	5	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.8 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.7	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 1.8 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 15 V; T <sub>j</sub> = 25 °C		-	18	-	ns
Q <sub>r</sub>	recovered charge			-	11	-	nC
t <sub>a</sub>	reverse recovery rise time			-	12	-	ns
t <sub>b</sub>	reverse recovery fall time			-	6	-	ns

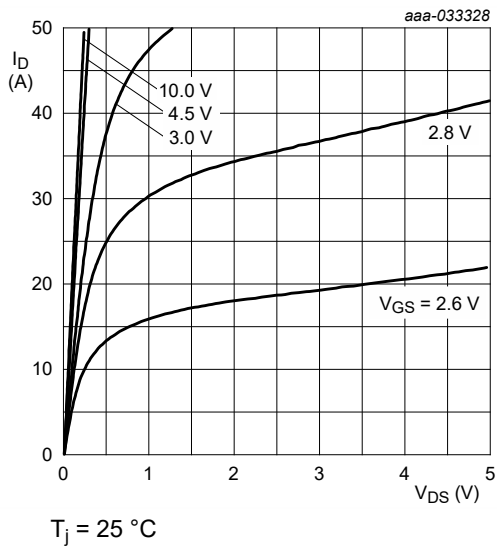


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

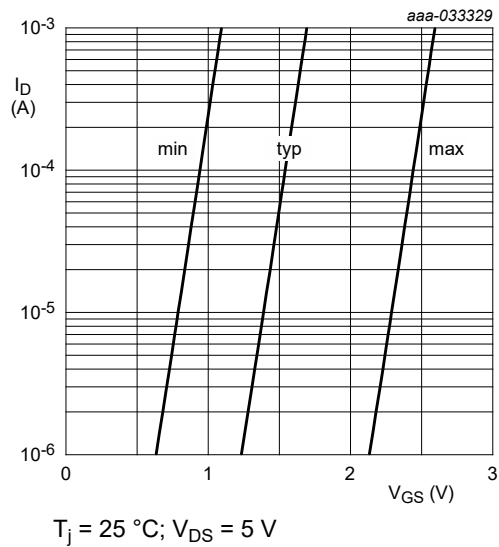


Fig. 7. Subthreshold drain current as a function of gate-source voltage

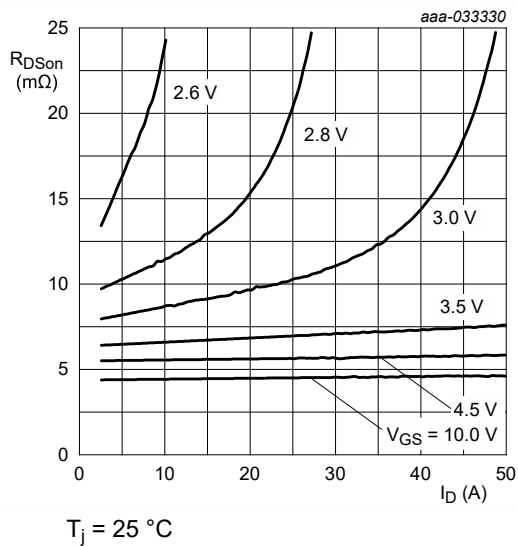


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

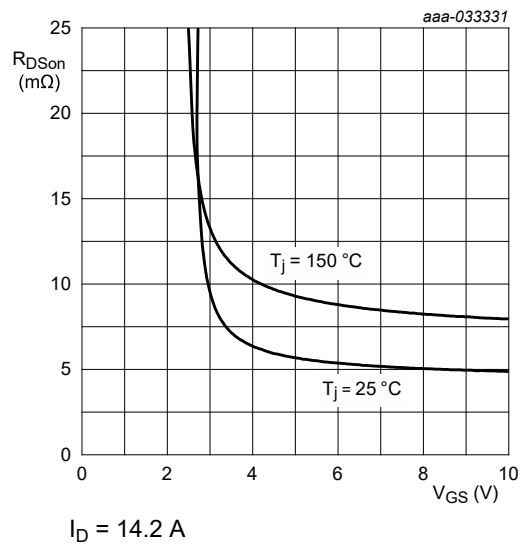


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

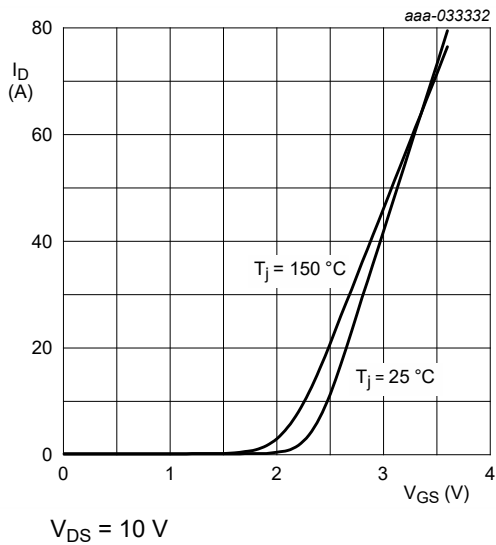


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

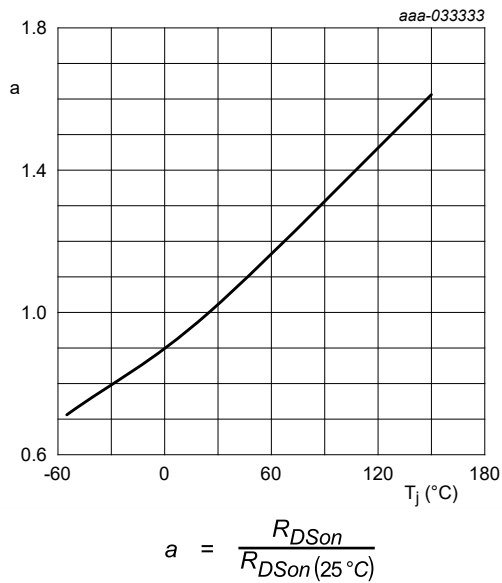


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

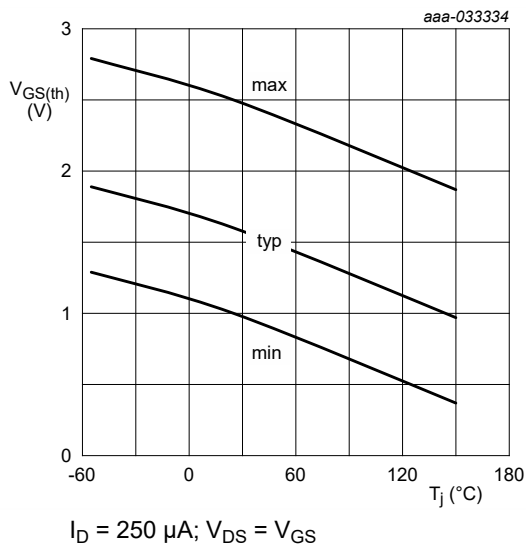


Fig. 12. Gate-source threshold voltage as a function of junction temperature

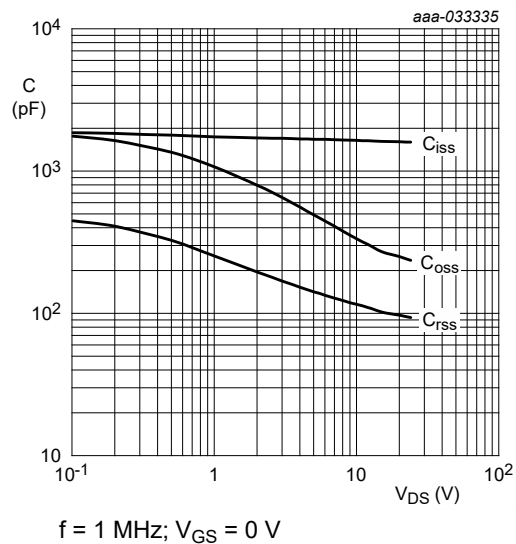


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



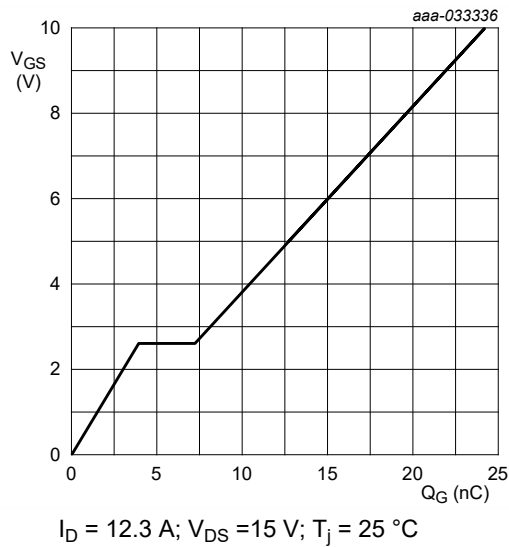


Fig. 14. Gate-source voltage as a function of gate charge; typical values

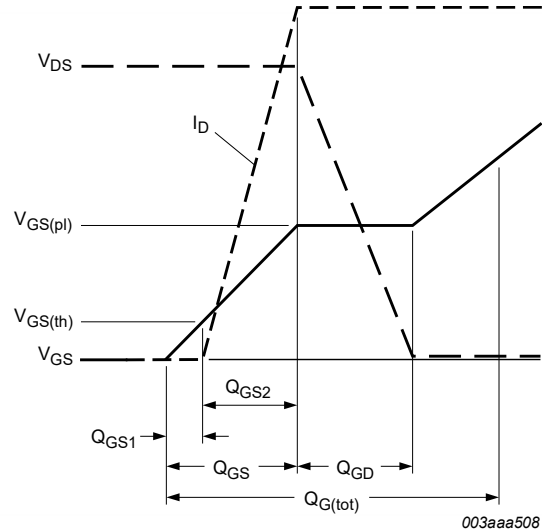


Fig. 15. Gate charge waveform definitions

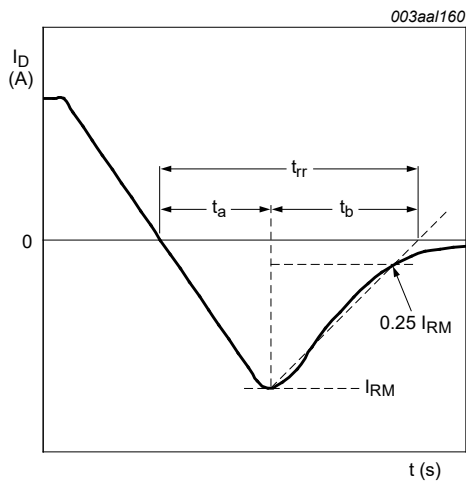


Fig. 16. Reverse recovery timing definition

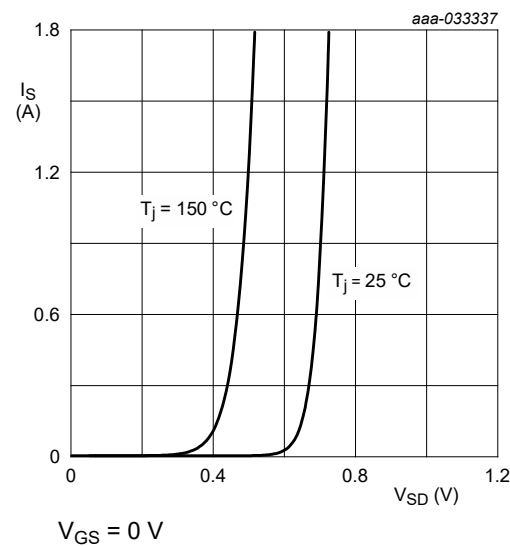


Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

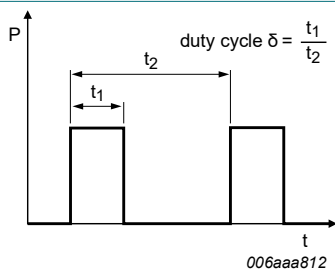
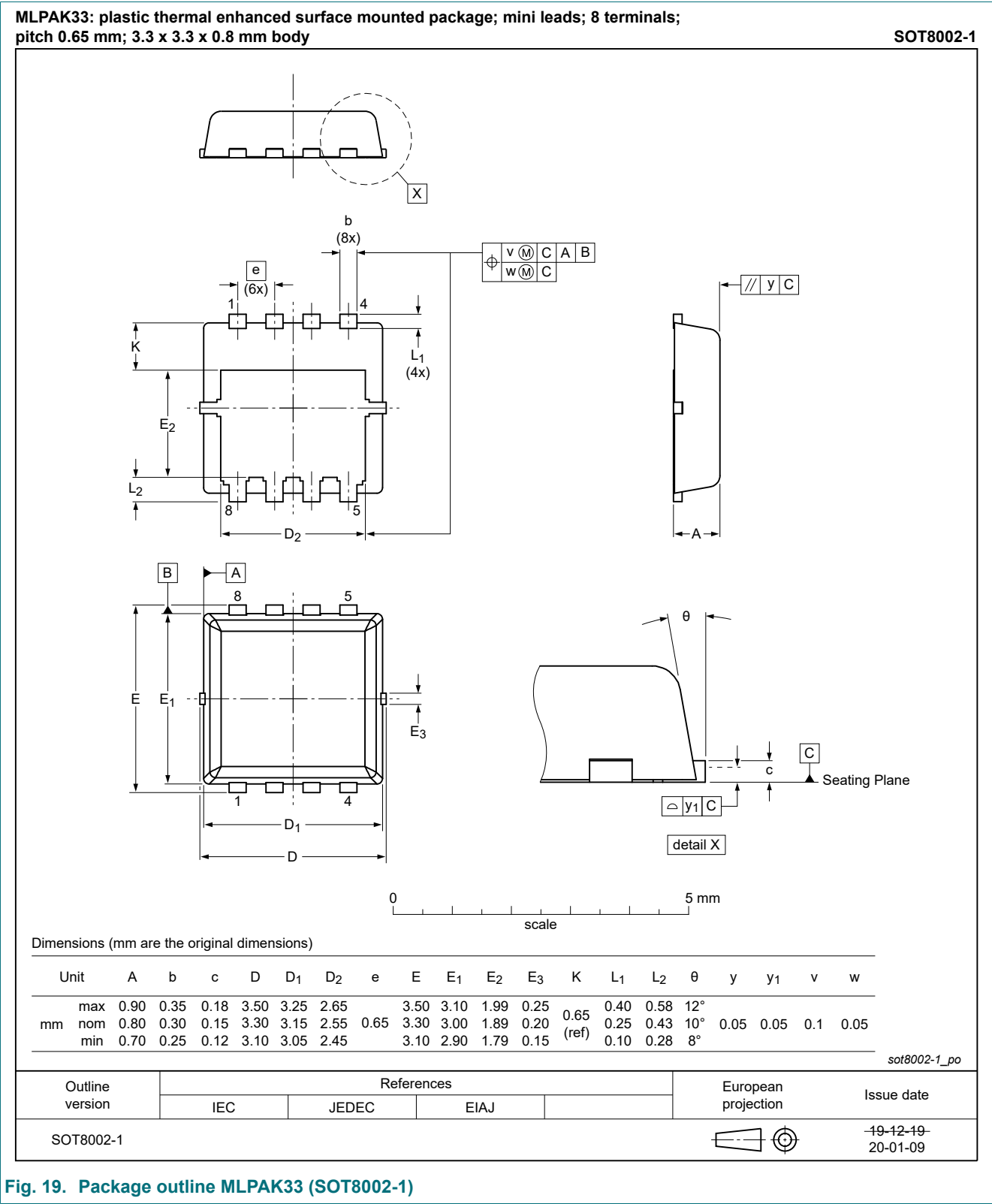


Fig. 18. Duty cycle definition

12. Package outline



13. Soldering

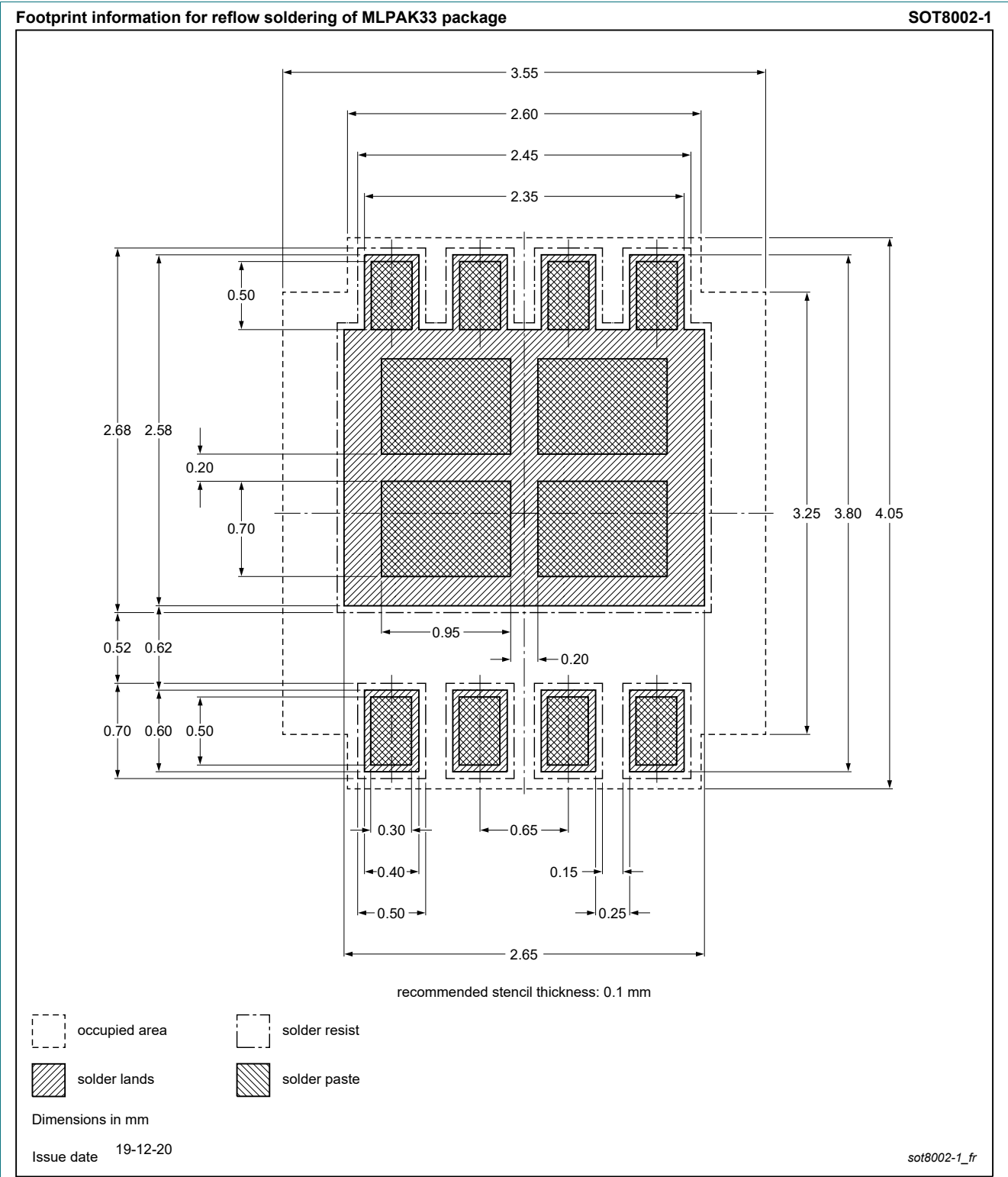


Fig. 20. Reflow soldering footprint for MLPAK33 (SOT8002-1)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXN5R4-30QL v.1	20210415	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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