



# PSMNR70-30YLH

N-channel 30 V, 0.82 mΩ, 300 A logic level MOSFET in LPAK56 using NextPowerS3 technology

12 November 2019

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package optimized for low  $R_{DS(on)}$ . Low  $I_{DSS}$  leakage even when hot, high efficiency and high current rated to 300 A, optimized for DC load switch and hot-swap applications.

## 2. Features and benefits

- 100% avalanche tested at  $I_{(AS)} = 190$  A
- Optimized for low  $R_{DS(on)}$
- Low leakage  $< 1$  μA at 25 °C
- Low spiking and ringing for low EMI designs
- Optimized for 4.5 V gate drive
- Copper-clip for low parasitic inductance and resistance
- High reliability LPAK package, qualified to 175 °C
- Wave solderable; exposed leads for optimal solder coverage and visual solder inspection

## 3. Applications

- Hot swap
- e-fuse
- Power OR-ing
- DC switch / Load switch
- Battery protection
- Brushed and BLDC (brushless) motor control
- Synchronous rectification in AC-DC and DC-DC applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	30	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	-	300	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	268	W
T <sub>j</sub>	junction temperature			-55	-	175	°C
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	0.66	0.82	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	0.86	1.1	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		2.9	16	32	nC
Q <sub>G(tot)</sub>	total gate charge			21	46	76	nC

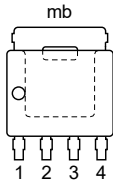
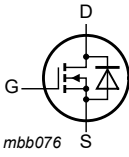
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
S	softness factor	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 16</a>	-	0.96	-	

[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-30YLH	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-30YLH	H7030L

## 8. Limiting values

Table 5. Limiting values

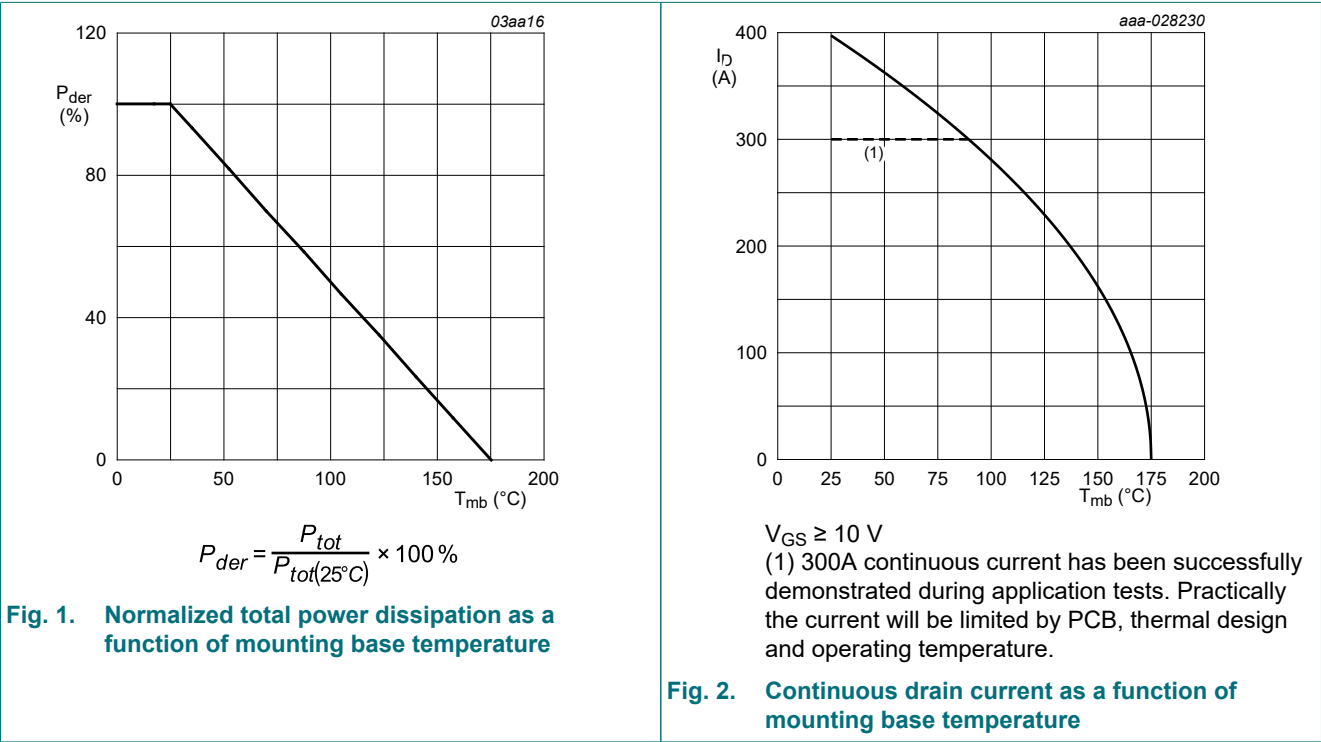
In accordance with the Absolute Maximum Rating System (IEC 60134).

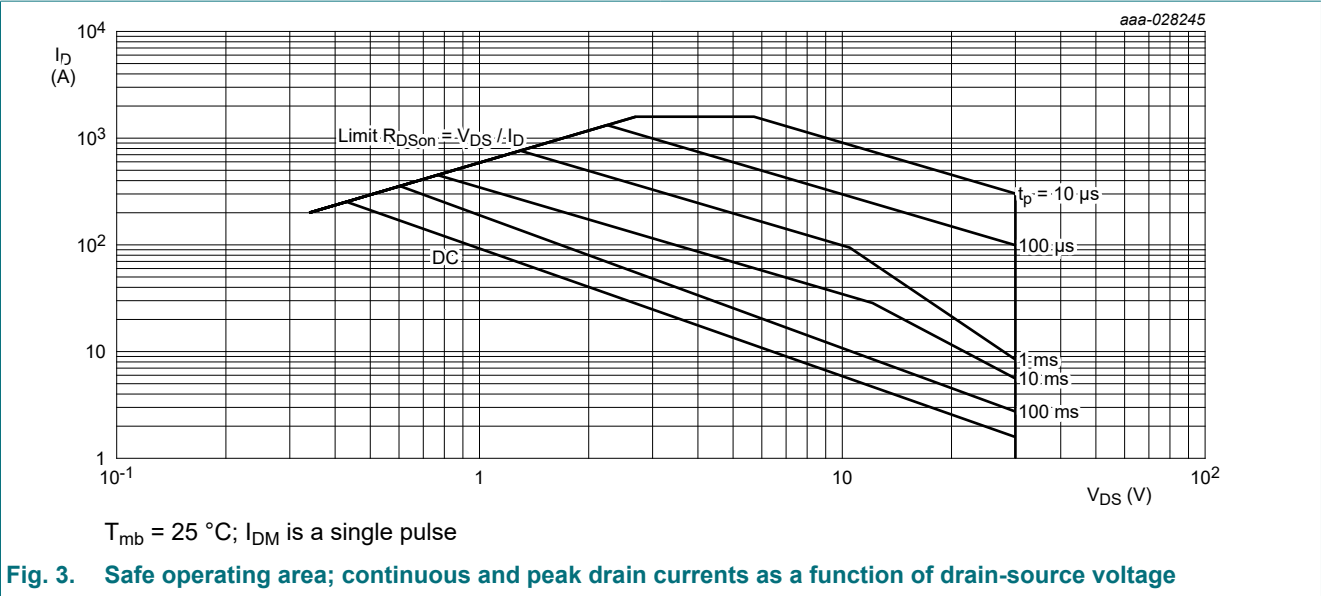
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	268	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	300	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>	-	281	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>	-	1589	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	268	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1589	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 25 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 4.9 ms	[2]	-	2.4	J
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 30 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω	[2]	-	190	A

- [1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

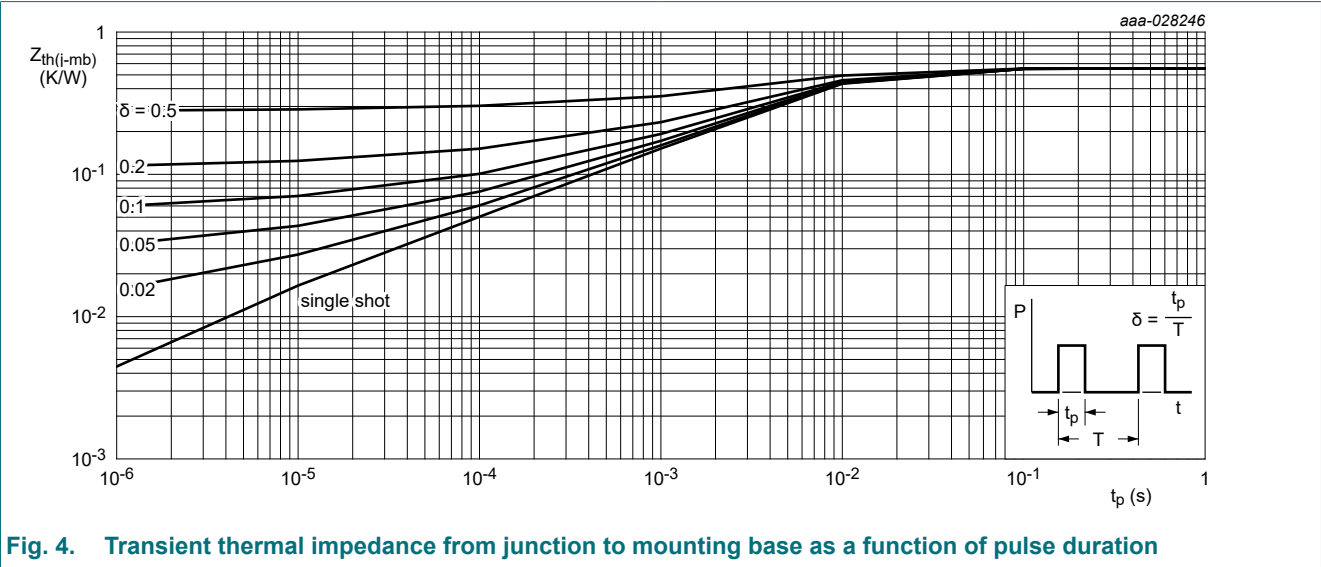


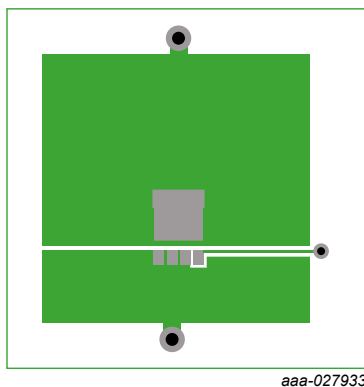


9. Thermal characteristics

Table 6. Thermal characteristics

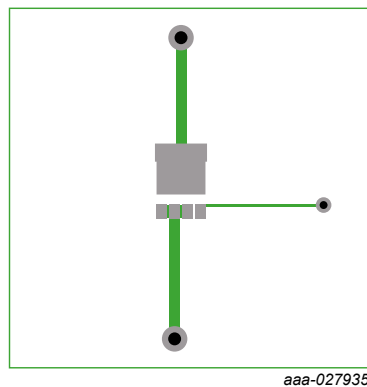
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>		-	0.48	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>		-	42	-	K/W
		<a href="#">Fig. 6</a>		-	85	-	K/W





Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

**Fig. 5. PCB layout for thermal resistance from junction to ambient**



70 μm thick copper on FR4 board

**Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient**

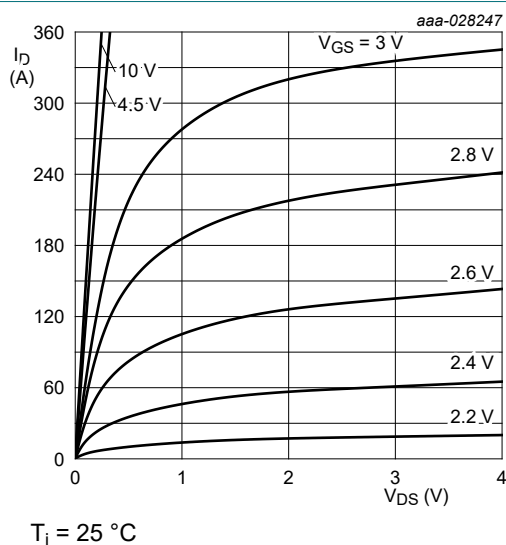
## 10. Characteristics

**Table 7. Characteristics**

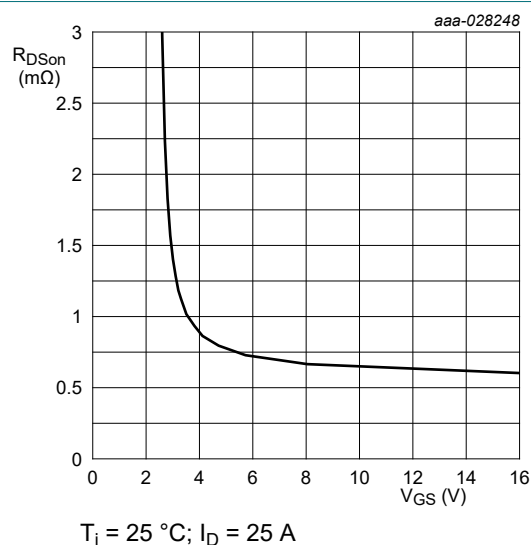
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 mA; V_{DS} = V_{GS}; T_j = 25 ^\circ C$	1.2	1.5	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_j \leq 150 ^\circ C$	-	-4.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 ^\circ C$	-	-	1	μA
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 125 ^\circ C$	-	6.4	-	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 ^\circ C;$ <a href="#">Fig. 10</a>	-	0.66	0.82	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150 ^\circ C;$ <a href="#">Fig. 11</a>	-	-	1.5	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 ^\circ C;$ <a href="#">Fig. 10</a>	-	0.86	1.1	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 ^\circ C;$ <a href="#">Fig. 11</a>	-	-	2	mΩ
$R_G$	gate resistance	$f = 1 MHz; T_j = 25 ^\circ C$	0.5	1.3	3.3	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V;$ <a href="#">Fig. 12; Fig. 13</a>	21	46	76	nC
		$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V;$ <a href="#">Fig. 12; Fig. 13</a>	43	95	157	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	50	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		3	11	21	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			2.2	8	15	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			0.86	3.2	6.1	nC
$Q_{GD}$	gate-drain charge			2.9	16	32	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	2.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a>		3284	5473	8210	pF
$C_{oss}$	output capacitance			1702	2836	4254	pF
$C_{rss}$	reverse transfer capacitance			129	478	1147	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$ ; $R_L = 0.6\text{ }\Omega$ ; $V_{GS} = 4.5\text{ V}$ ; $R_{G(ext)} = 5\text{ }\Omega$		-	28	-	ns
$t_r$	rise time			-	51	-	ns
$t_{d(off)}$	turn-off delay time			-	61	-	ns
$t_f$	fall time			-	45	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$		-	62	-	nC
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 15</a>		-	0.75	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 16</a>		-	46	-	ns
$Q_r$	recovered charge		[1]	-	50	-	nC
$t_a$	reverse recovery rise time			-	23.4	-	ns
$t_b$	reverse recovery fall time			-	22.5	-	ns
$S$	softness factor			-	0.96	-	

[1] includes capacitive recovery



**Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values**

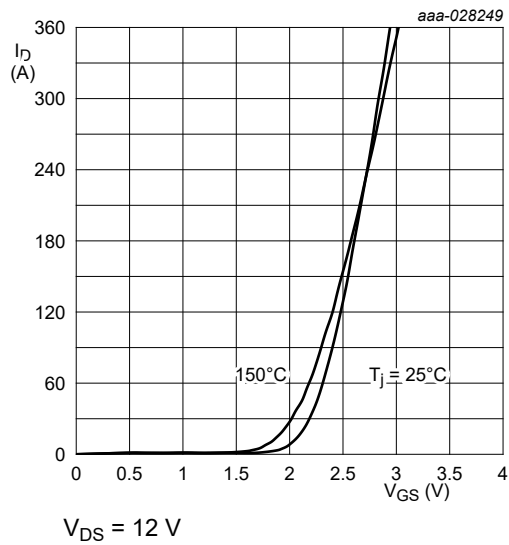


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

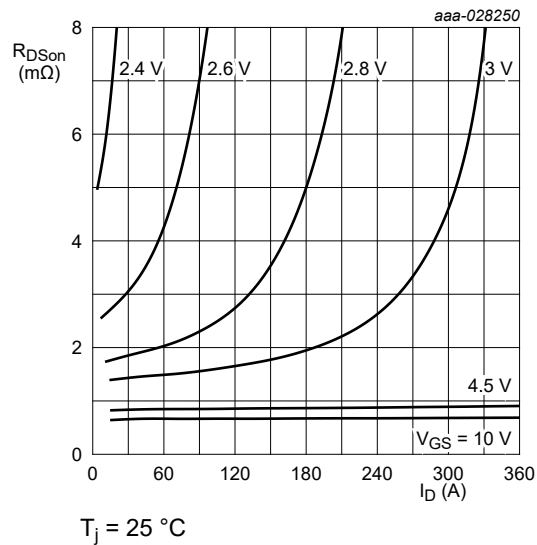


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

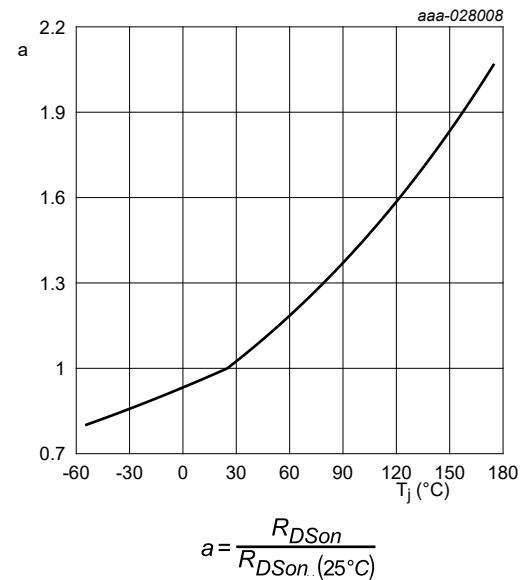


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

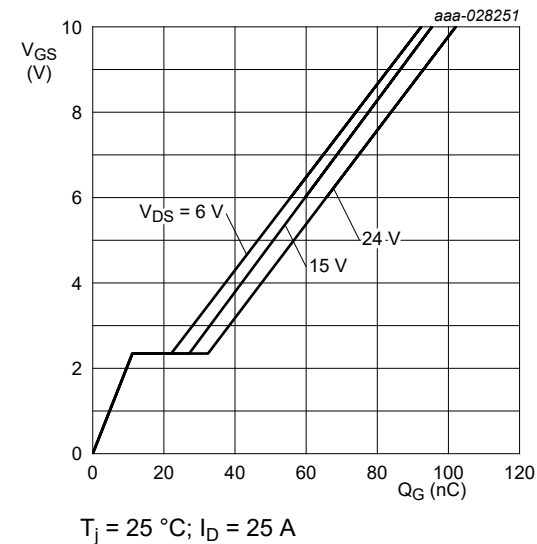
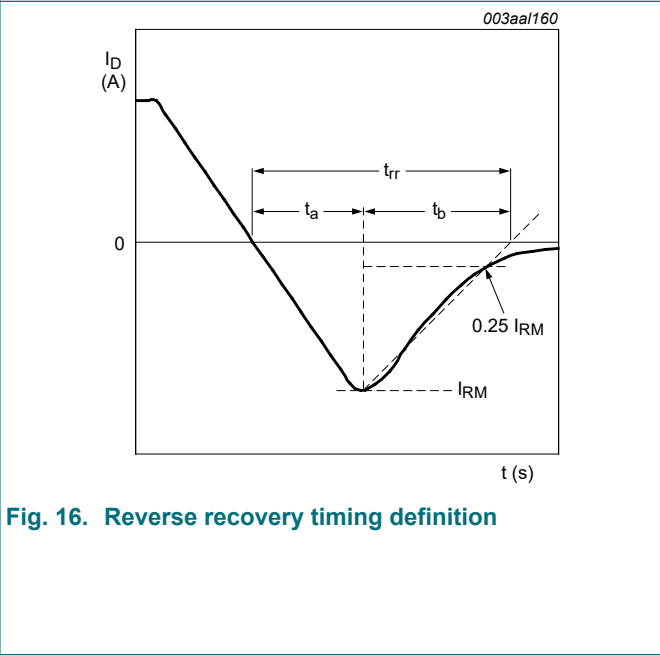
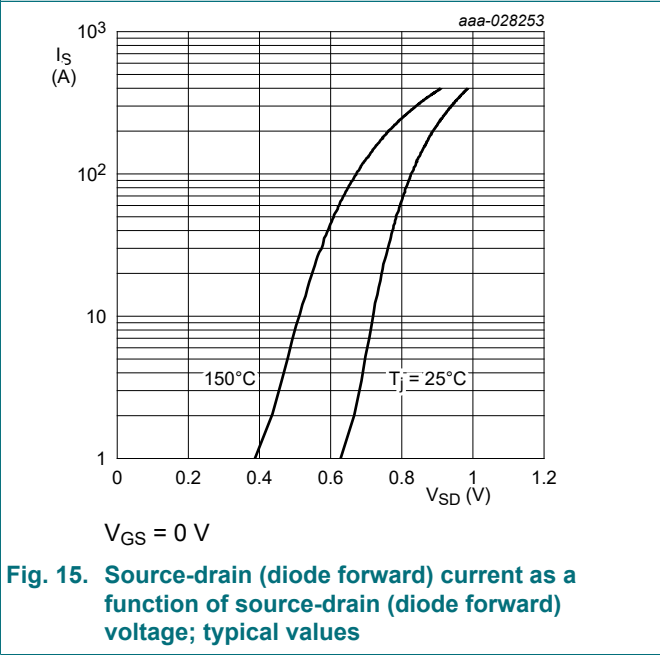
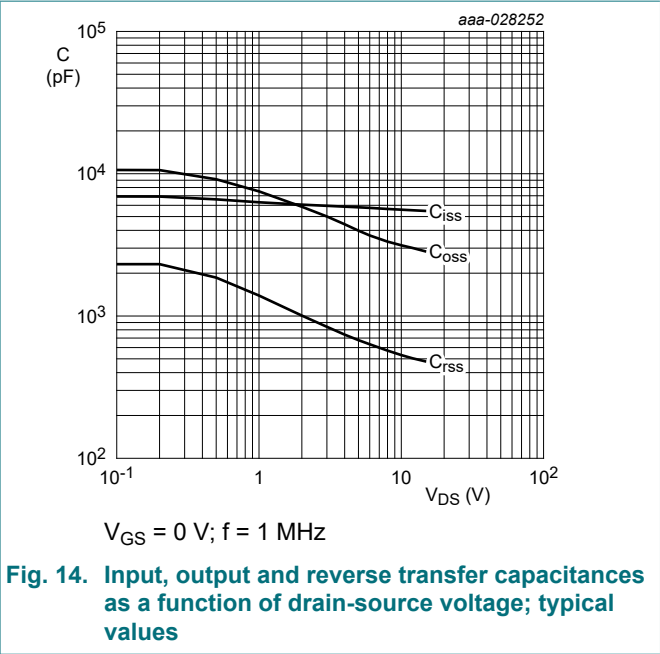
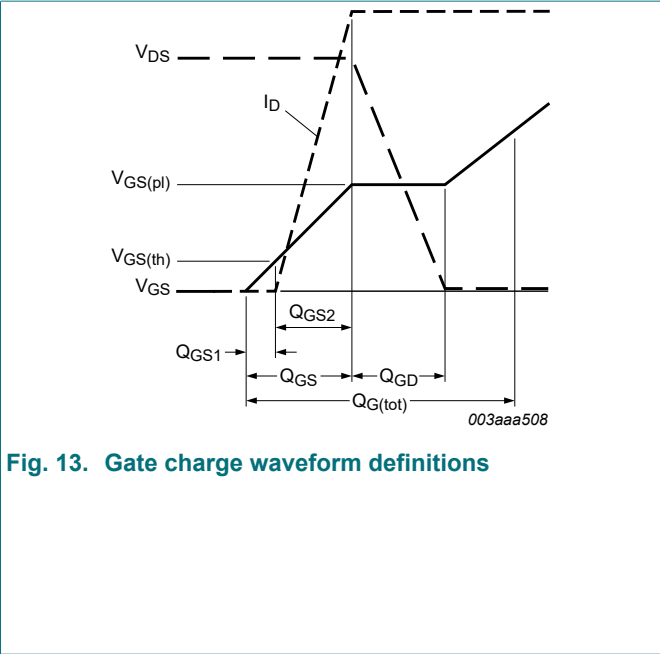


Fig. 12. Gate-source voltage as a function of gate charge; typical values





11. Package outline

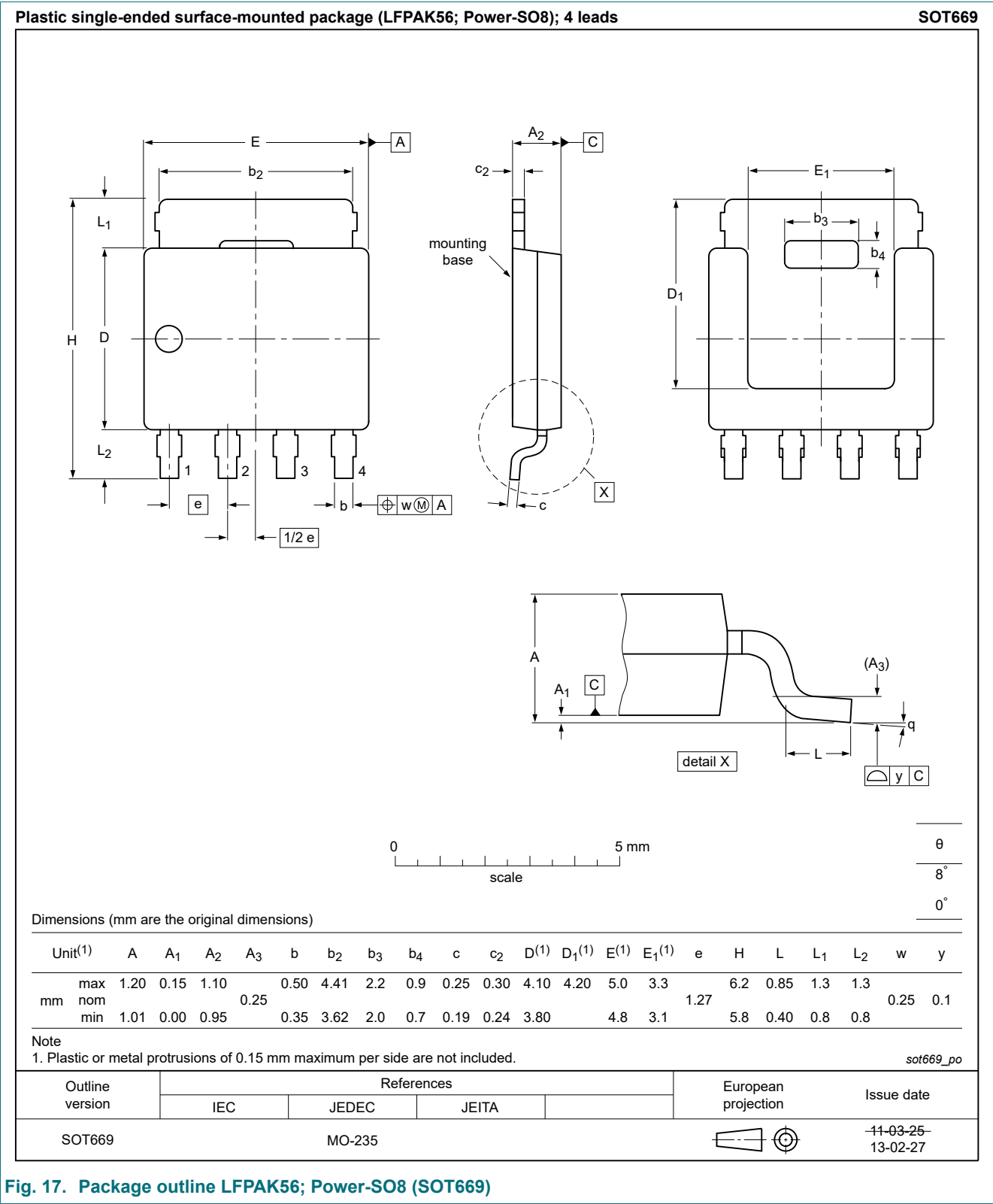
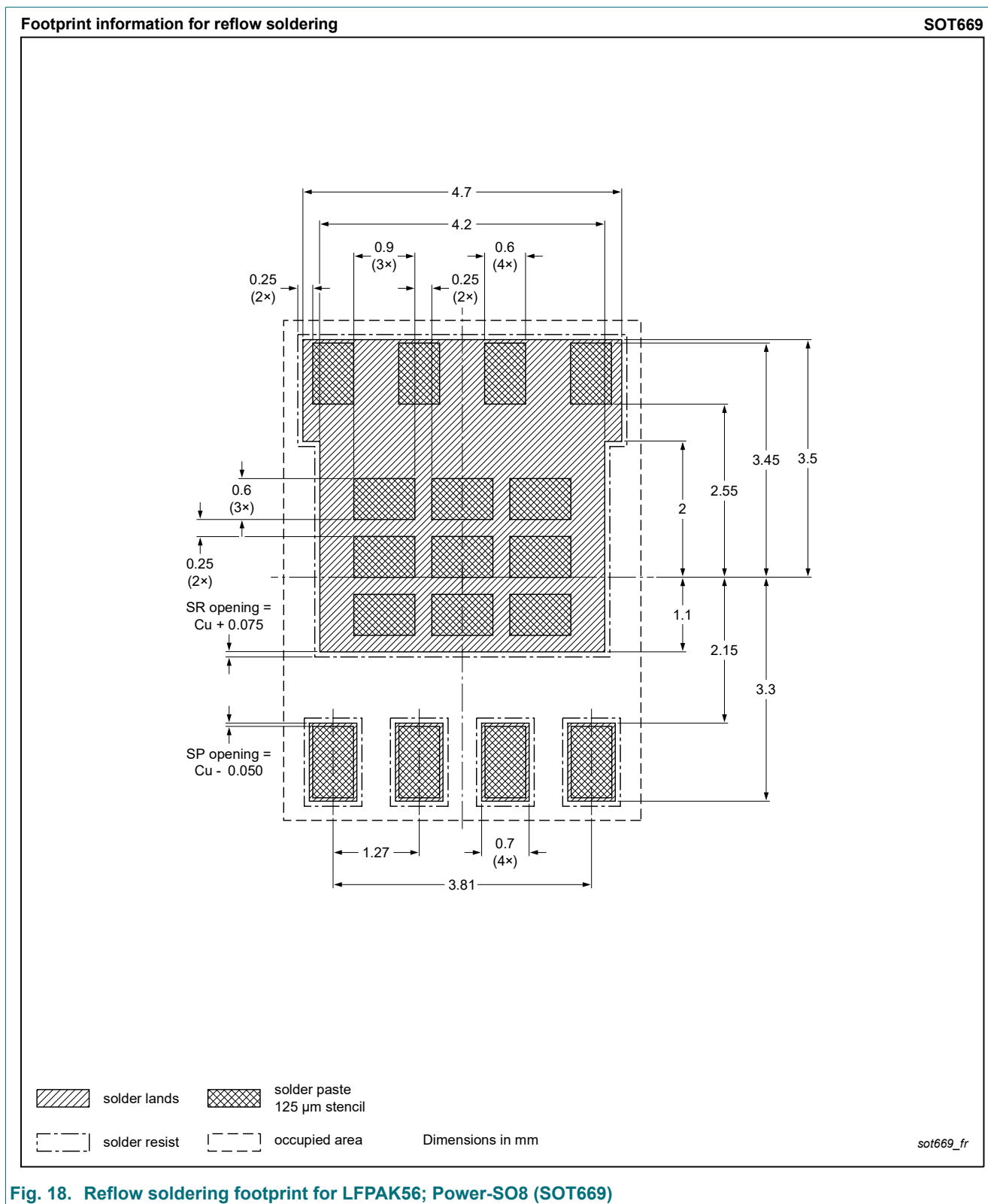


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

## 12. Soldering



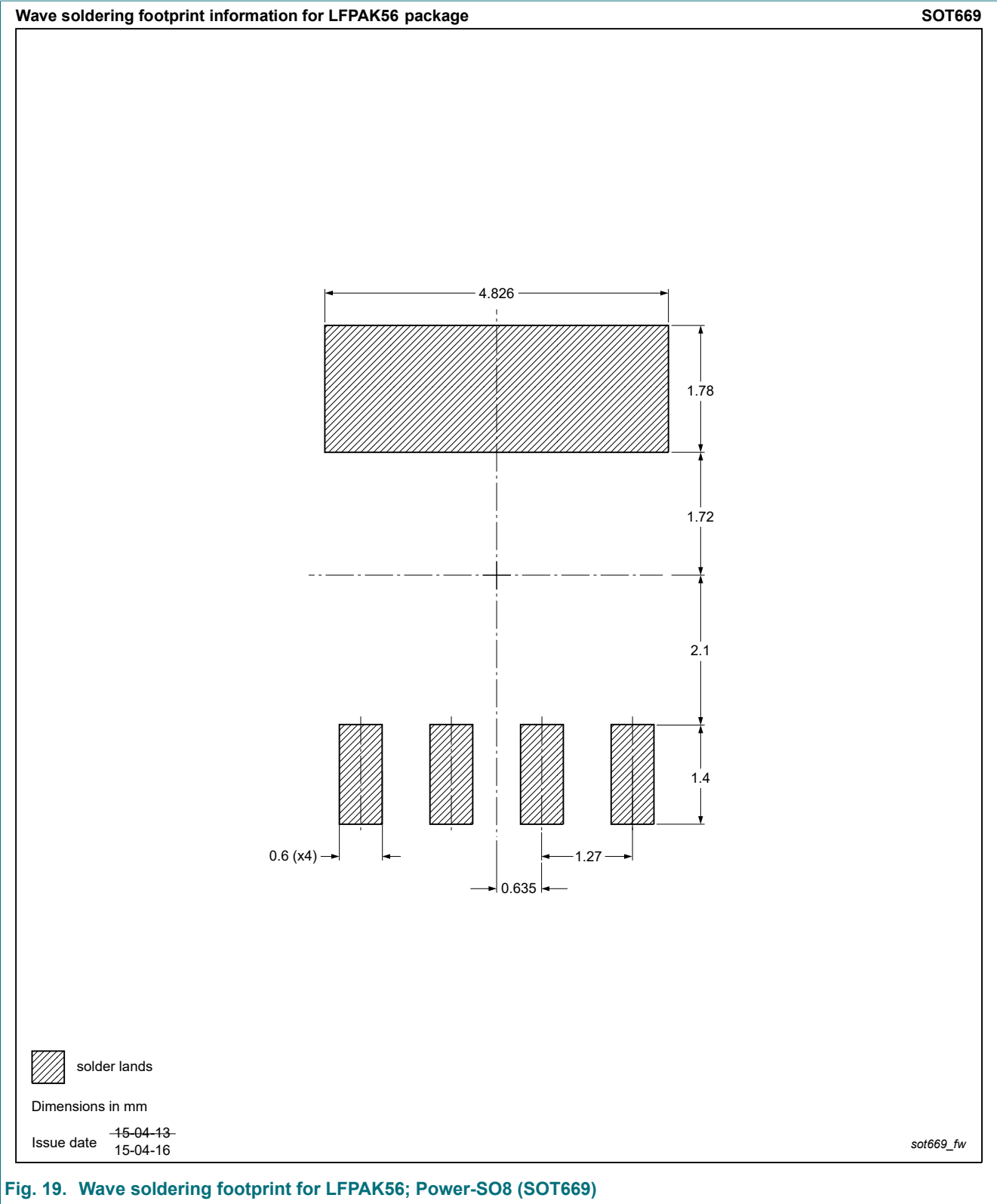


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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