

PSMN7R6-60PS

N-channel 60 V 7.8 m Ω standard level MOSFET Rev. 03 — 28 October 2010

Product data sheet

Product profile 1.

1.1 General description

Standard level N-channel MOSFET in a TO-220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	60	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	-	-	92	Α
P _{tot}	total power dissipation	$T_{mb} = 25 ^{\circ}\text{C}$; see Figure 2	-	-	149	W
Static chara	acteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 13}{\text{Figure } 9};$ see Figure 9	-	5.9	7.8	mΩ
Dynamic ch	naracteristics					
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 30 V; see <u>Figure 15</u> ; see <u>Figure 14</u>	-	10.6	-	nC
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$V_{GS} = 10 \text{ V}; T_{j(init)} = 25 \text{ °C};$ $I_D = 92 \text{ A}; V_{sup} \le 100 \text{ V};$ $R_{GS} = 50 \Omega; unclamped$	-	-	110	mJ



Pinning information

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			SOT78 (TO-220AB)	

Ordering information 3.

Table 3. **Ordering information**

Type number	Package		
	Name	Description	Version
PSMN7R6-60PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

Limiting values

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	-	65	Α
		V _{GS} = 10 V; T _{mb} = 25 °C; see <u>Figure 1</u>	-	92	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; see <u>Figure 3</u>	-	389	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	149	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drai	in diode				
Is	source current	T _{mb} = 25 °C	-	92	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$	-	389	Α
Avalanche r	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 92 A; $V_{sup} \le$ 100 V; R_{GS} = 50 Ω ; unclamped	-	110	mJ

PSMN7R6-60PS

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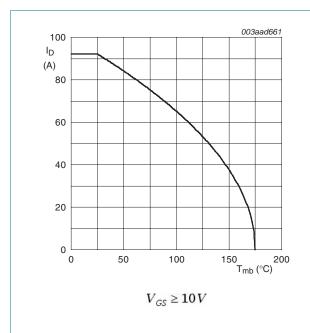


Fig 1. Continuous drain current as a function of mounting base temperature

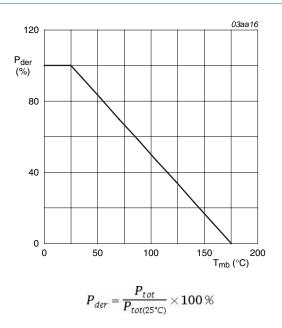
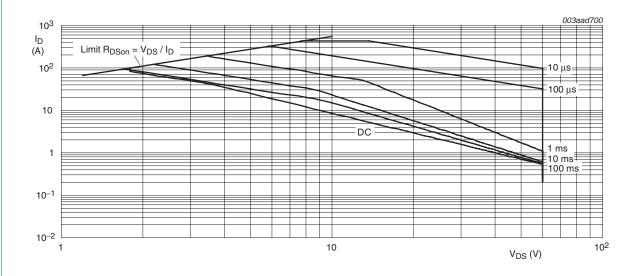


Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25 \,{}^{\circ}C; I_{DM}$ is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Table 5. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <u>Figure 4</u>	-	0.49	1.01	K/W

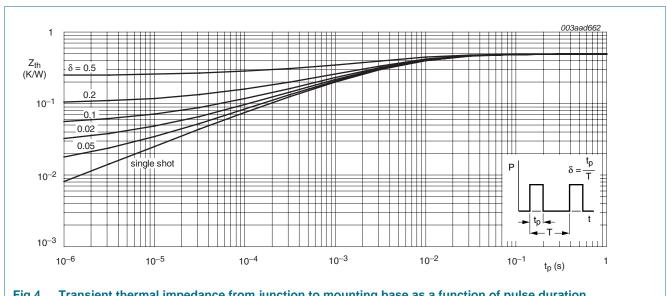


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

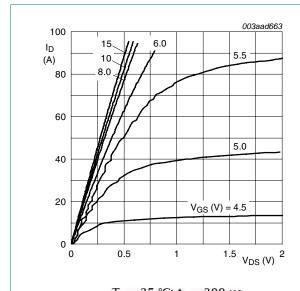
6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 11	1	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 11	-	-	4.6	V
I _{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	100	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ °C};$ see Figure 12	-	13.3	18	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see <u>Figure 13</u> ; see <u>Figure 9</u>	-	5.9	7.8	mΩ
R _G	gate resistance	f = 1 MHz	-	0.98	-	Ω
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; \ V_{DS} = 30 \text{ V}; \ V_{GS} = 10 \text{ V};$	-	38.7	-	nC
Q_{GS}	gate-source charge	see Figure 14; see Figure 15	-	12.9	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	6.9	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	6	-	nC
Q_GD	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 30 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 15; see Figure 14	-	10.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 30 \text{ V}$; see Figure 14; see Figure 15	-	5.6	-	V
C _{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{Figure 8}}; \text{ see}$	-	2651	-	pF
C _{oss}	output capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{ or see 16}}$	-	342	-	pF
C _{rss}	reverse transfer capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{Figure 8}}; \text{ see}$	-	183	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	19	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	21	-	ns
t _{d(off)}	turn-off delay time		-	37	-	ns
t _f	fall time		-	13	-	ns

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dra	in diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 17</u>	-	0.86	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = 100 \text{ A/}\mu\text{s}$;	-	40.4	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}$	-	56	-	nC



 $T_j = 25$ °C; $t_p = 300 \, \mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

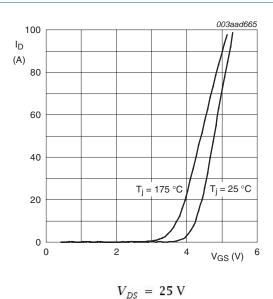


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

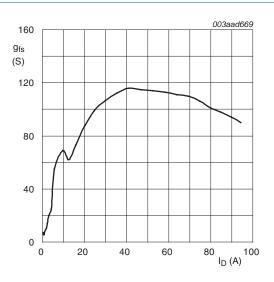
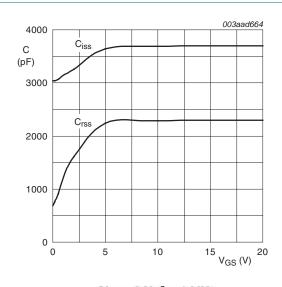


Fig 6. Forward transconductance as a function of drain current; typical values



 $V_{DS} = 0 \text{ V; } f = 1 \text{ MHz}$

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

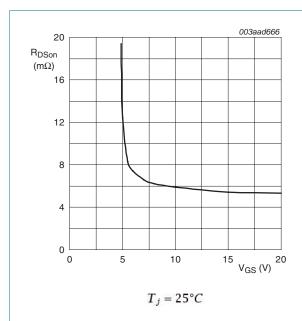
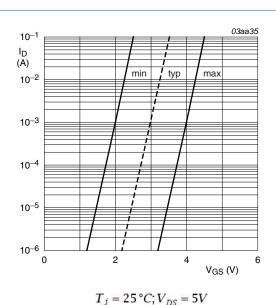


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



- J - D - C, - DS - D

Fig 10. Sub-threshold drain current as a function of gate-source voltage

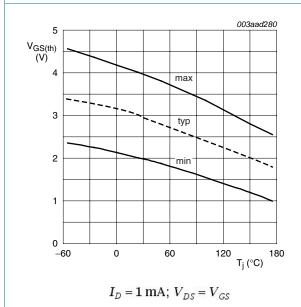


Fig 11. Gate-source threshold voltage as a function of junction temperature

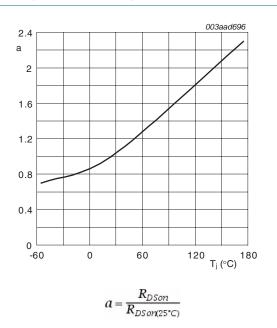


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature.

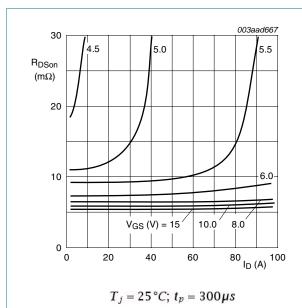


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

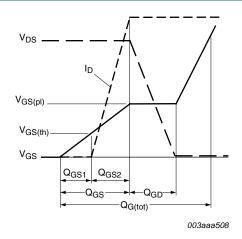
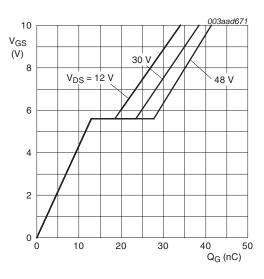
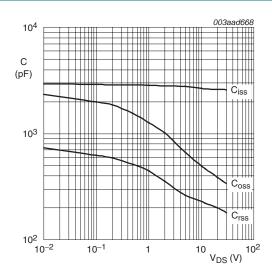


Fig 15. Gate charge waveform definitions



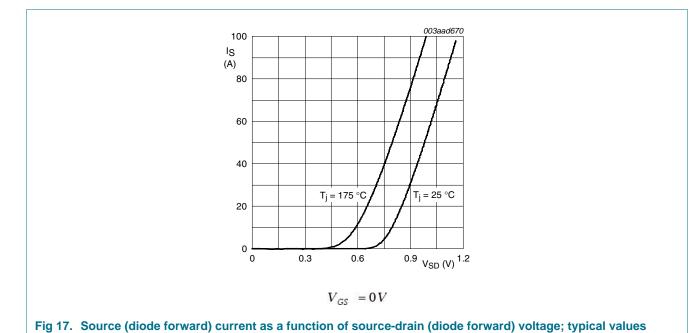
 $T_j = 25^{\circ}C; I_D = 25 A$

Fig 14. Gate-source voltage as a function of gate charge; typical values

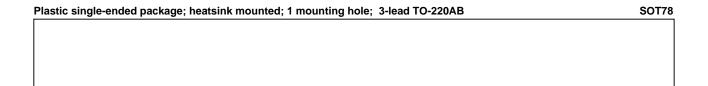


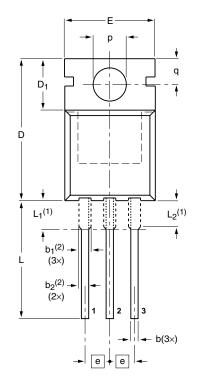
$$V_{DS} = 0V$$
; $f = 1 \text{ MHz}$

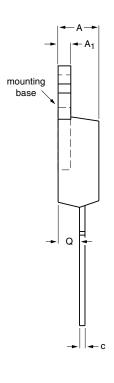
Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

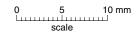


7. Package outline









DIMENSIONS (mm are the original dimensions)

UNI	ТА	A ₁	b	b ₁ (2)	b ₂ (2)	С	D	D ₁	E	е	L	L ₁ (1)	L ₂ ⁽¹⁾ max.	р	q	Q	
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2	

Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13	

Fig 18. Package outline SOT78 (TO-220AB)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN7R6-60PS v.3	20101028	Product data sheet	-	PSMN7R6-60PS v.2
Modifications:	 Various changes 	to content.		
PSMN7R6-60PS v.2	20100122	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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