

PSMN1R6-30BL

N-channel 30 V 1.9 m Ω logic level MOSFET in D2PAK Rev. 1 — 22 March 2012 Product

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _i ≥ 25 °C; T _i ≤ 175 °C		-	-	30	V
I _D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	[1]	-	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	306	W
T _j	junction temperature			-55	-	175	°C
Static char	racteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 ^{\circ}\text{C};$ see Figure 13; see Figure 6		-	2.21	2.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 6		-	1.58	1.9	mΩ
Dynamic o	haracteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$		-	27	-	nC
Q _{G(tot)}	total gate charge	see Figure 14; see Figure 15		-	101	-	nC
	ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped		-	-	1.7	J

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

	•	•		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]	mb	D D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R6-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R6-30BL	PSMN1R6-30BL

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

		3 7				
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	$V_{GS} = 10 \text{ V; } T_{mb} = 100 \text{ °C; see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u>	-	100	Α
		$V_{GS} = 10 \text{ V; } T_{mb} = 25 \text{ °C; see } Figure 1$	<u>[1]</u>	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 3		-	1268	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	306	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drai	n diode					
Is	source current	T _{mb} = 25 °C	<u>[1]</u>	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1268	Α
Avalanche r	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; unclamped		-	1.7	J

[1] Continuous current is limited by package.

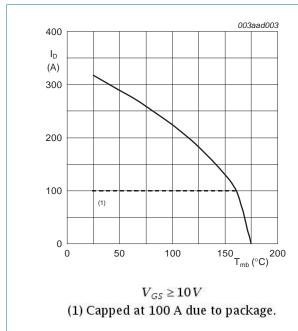
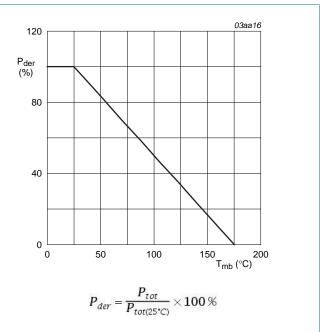
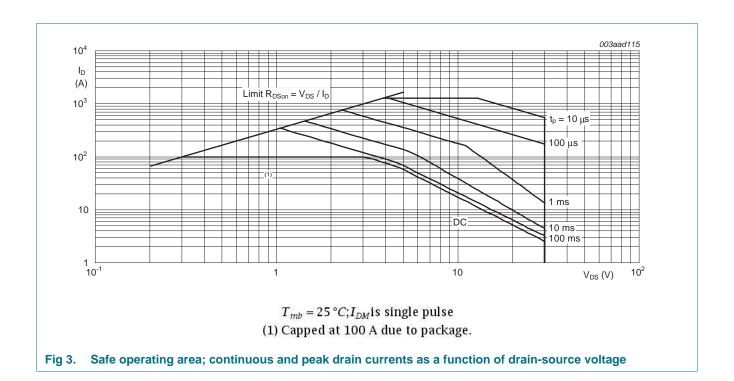


Fig 1. Continuous drain current as a function of mounting base temperature



 Normalized total power dissipation as a function of mounting base temperature

PSMN1R6-30BL



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.22	0.49	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W

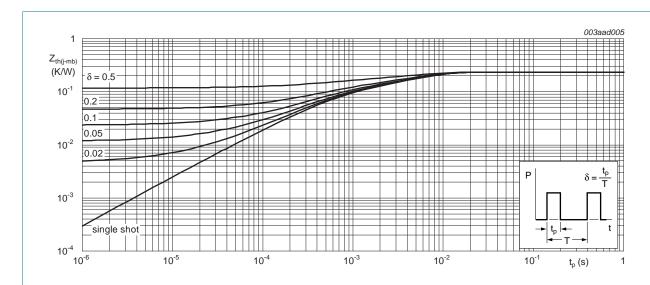


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
V _{GS(th)} gate-source	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	1.3	1.7	2.15	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 12	0.5	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 12	-	-	2.45	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	5	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	150	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nΑ
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nΑ
R _{DSon} drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 13; see Figure 6	-	3	3.5	mΩ	
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 6	-	1.84	2.2	mΩ
	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ see Figure 13; see Figure 6	-	2.21	2.6	mΩ	
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}; \text{see}$ Figure 6	-	1.58	1.9	mΩ
R_G	gate resistance	f = 1 MHz	-	0.98	-	Ω
Dynamic c	haracteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	212	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	193	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	101	-	nC
Q_{GS}	gate-source charge	see Figure 14; see Figure 15	-	33	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	20	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	13	-	nC
Q _{GD}	gate-drain charge		-	27	-	nC
V _{GS(pI)}	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.5	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz;	-	12493	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	2486	-	pF
C _{rss}	reverse transfer capacitance		-	1034	-	pF

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 Table 7.
 Characteristics ...continued

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$	-	104	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	163	-	ns
t _{d(off)}	turn-off delay time		-	174	-	ns
t _f	fall time		-	87	-	ns
Source-dra	ain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17	-	0.77	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	64	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	79	-	nC

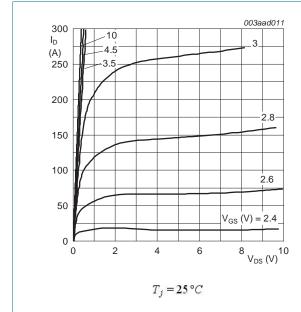


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

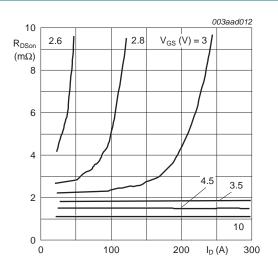


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

 $T_j = 25\,^{\circ}C$

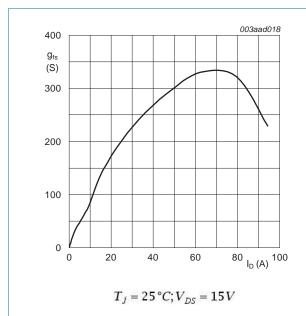


Fig 7. Forward transconductance as a function of drain current; typical values

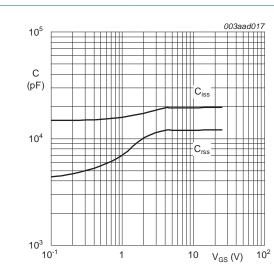
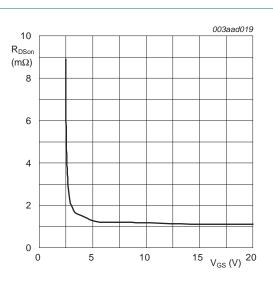


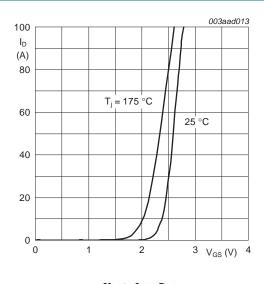
Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

 $V_{DS} = 0V; f = 1MHz$



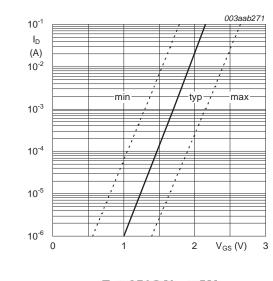
 $T_j = 25 \,^{\circ}C; I_D = 25A$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $T_j=25\,^{\circ}C; V_{DS}=5\,V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage

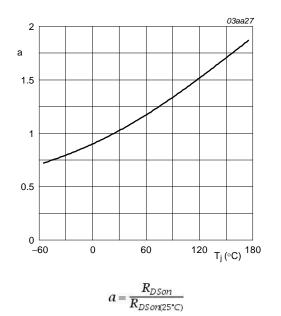
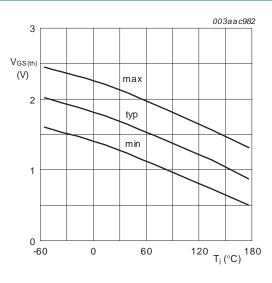


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 12. Gate-source threshold voltage as a function of junction temperature

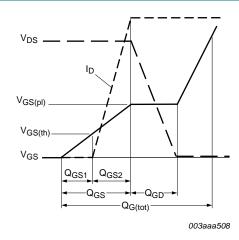


Fig 14. Gate charge waveform definitions

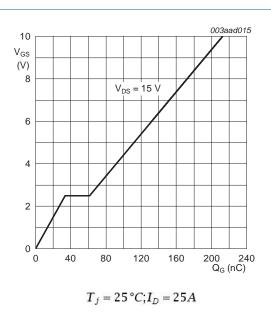
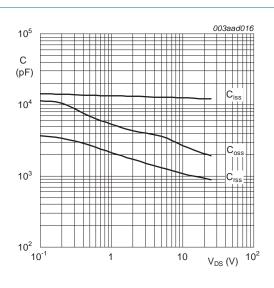


Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

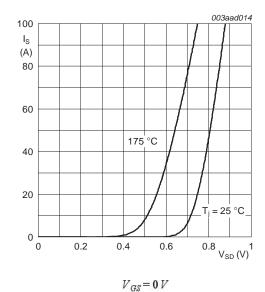


Fig 17. Source current as a function of source-drain voltage; typical values

8. Package outline

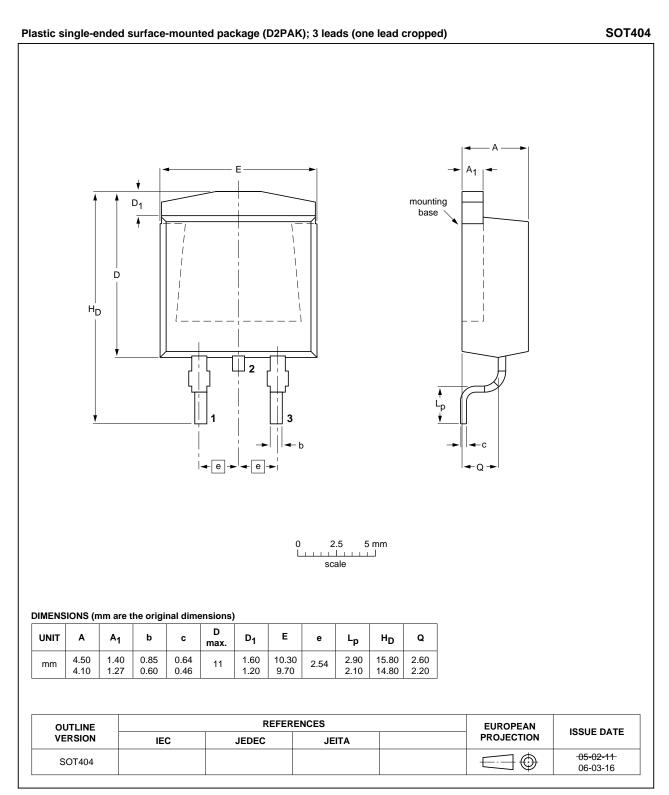


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R6-30BL v.1	20120322	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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