



PSMN1R0-40YSH

N-channel 40 V, 1 mΩ, 290 A standard level MOSFET in LPAK56E using NextPower-S3 Schottky-Plus technology

25 April 2019

Product data sheet

1. General description

290 Amp, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56E package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 290 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I_{DSS} leakage
- Strong linear-mode / SOA rating
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch and eFuse

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	290	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	333	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10		-	0.85	1	mΩ
Dynamic characteristics							

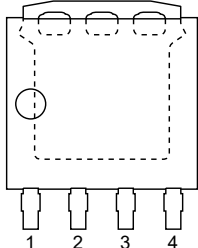
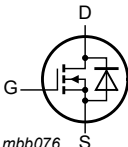
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 12 ; Fig. 13	-	13	27	nC
$Q_{G(tot)}$	total gate charge		-	87	122	nC

[1] 290A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-40YSH	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-40YSH	1H0S40J

8. Limiting values

Table 5. Limiting values

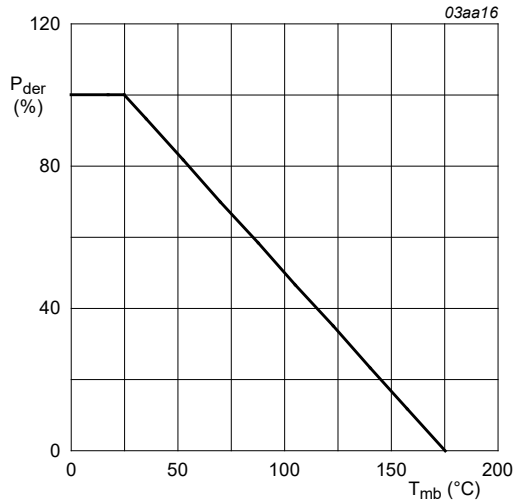
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$	-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed	-	45	V
V_{DGR}	drain-gate voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 1	-	333	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2	[1]	290	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 2	-	277	A

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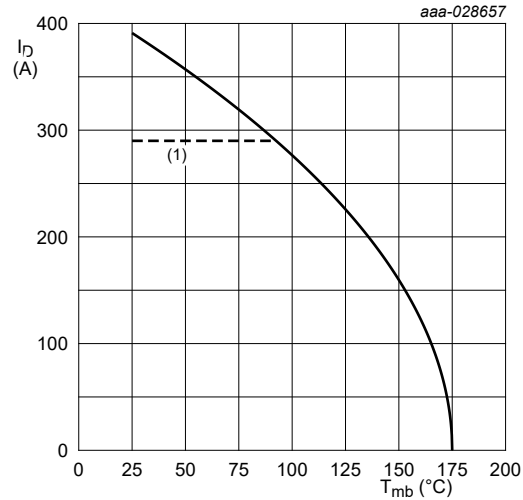
Symbol	Parameter	Conditions		Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$; Fig. 3		-	1564	A
T_{stg}	storage temperature			-55	175	$^\circ C$
T_j	junction temperature			-55	175	$^\circ C$
$T_{sld(M)}$	peak soldering temperature			-	260	$^\circ C$
Source-drain diode						
I_S	source current	$T_{mb} = 25^\circ C$		-	278	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$		-	1564	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 83 A$; $V_{sup} \leq 40 V$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 V$; $T_{j(init)} = 25^\circ C$; unclamped; $t_p = 0.27 ms$	[2]	-	578	mJ
		$I_D = 25 A$; $V_{sup} \leq 40 V$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 V$; $T_{j(init)} = 25^\circ C$; unclamped; $t_p = 4.2 ms$	[2]	-	2710	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 40 V$; $V_{GS} = 10 V$; $T_{j(init)} = 25^\circ C$; $R_{GS} = 50 \Omega$	[2]	-	190	A

- [1] 290A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

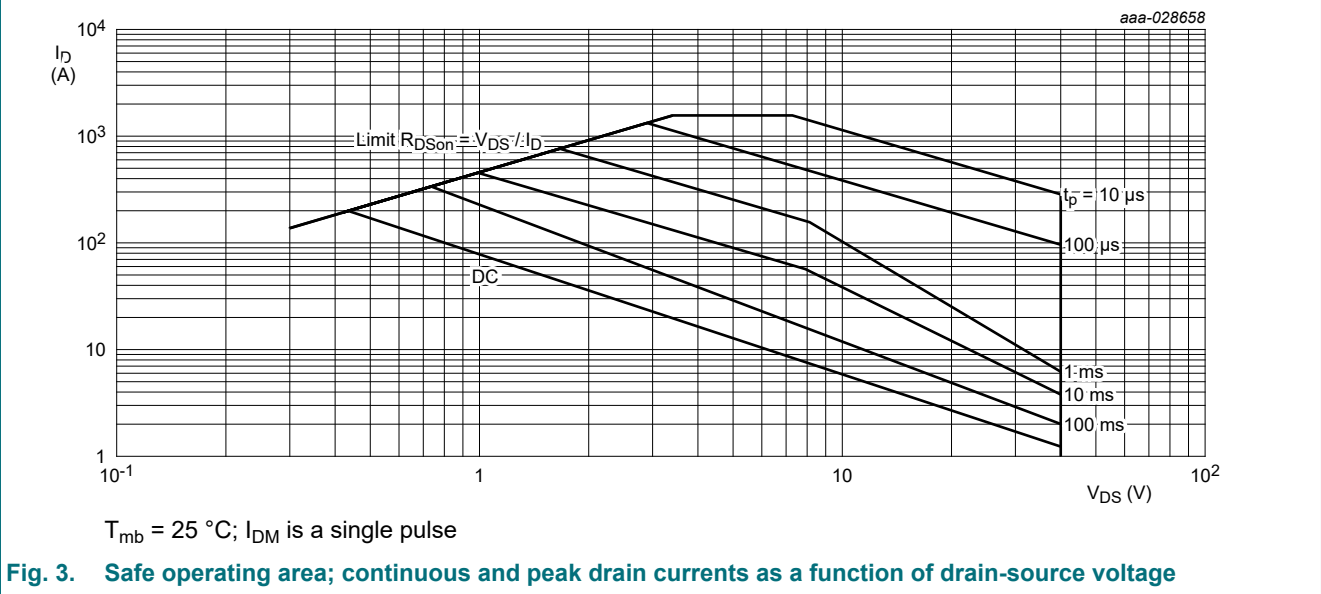


$V_{GS} \geq 10 V$

(1) 290A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

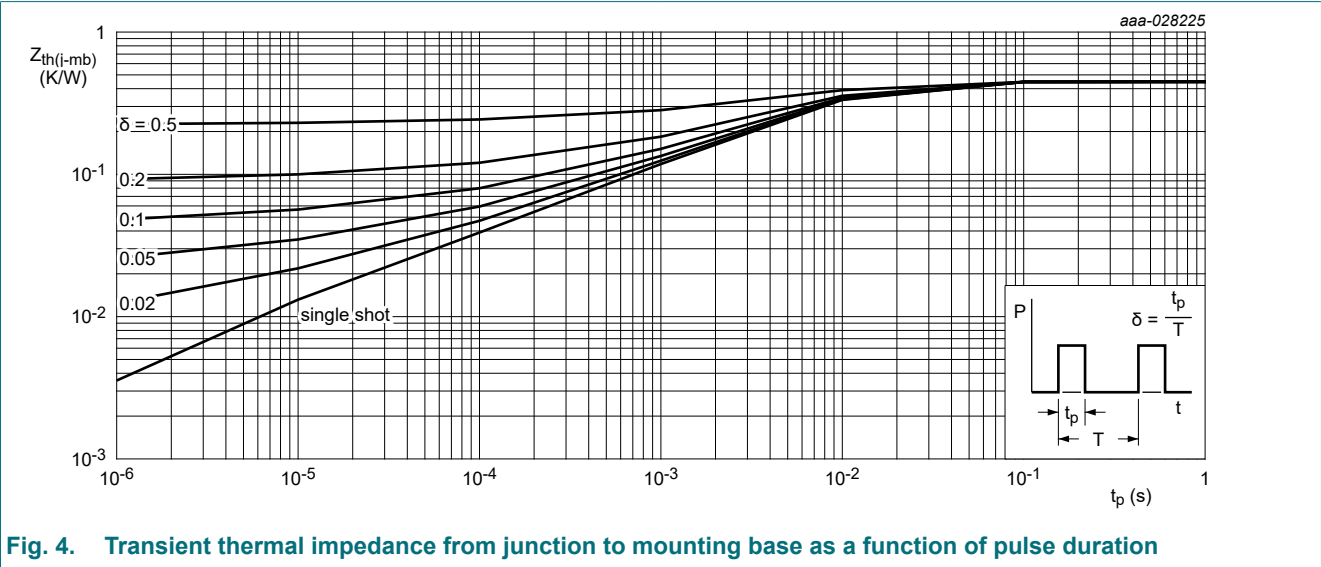
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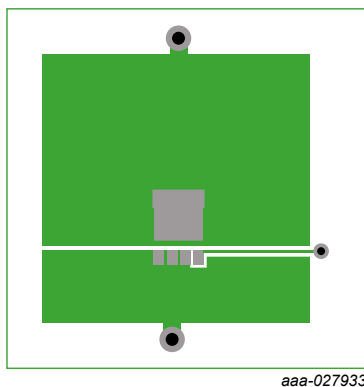
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.33	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W

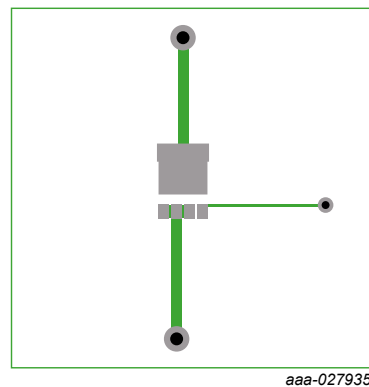


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Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

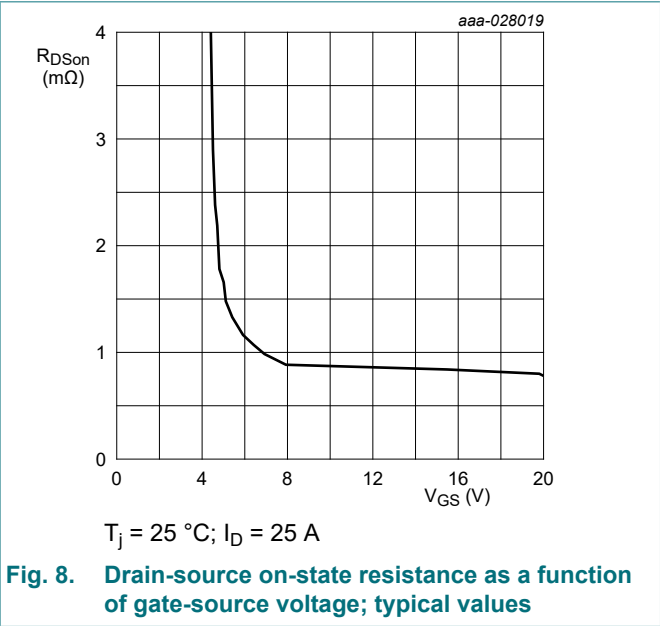
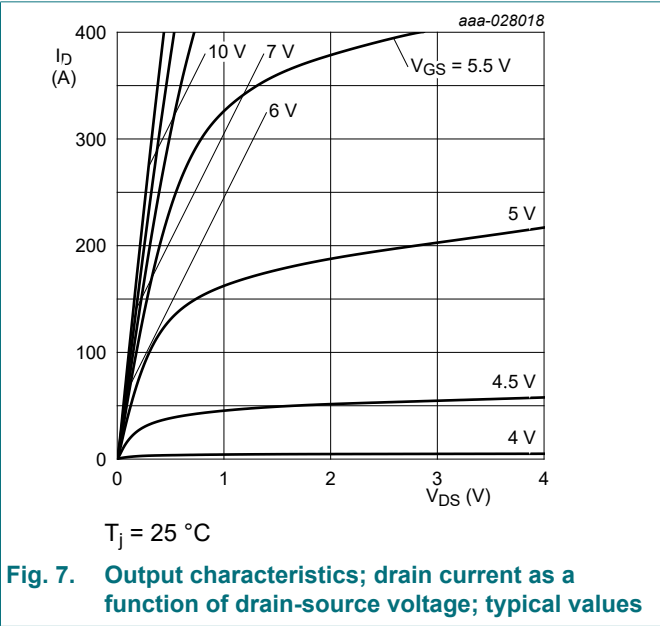
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$	2.4	3	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$	-	-7.4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	1	μA
		$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	13	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C; \text{Fig. 10}$	-	0.85	1	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C; \text{Fig. 11}$	-	-	2.2	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$	0.5	1.2	2.9	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; \text{Fig. 12; Fig. 13}$	-	87	122	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	42	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; \text{Fig. 12; Fig. 13}$	-	26	39	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	18	27	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	8.3	13	nC
Q_{GD}	gate-drain charge		-	13	27	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 20 V; \text{Fig. 12; Fig. 13}$	-	4.3	-	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 14		-	6738	9433	pF
C _{oss}	output capacitance			-	1767	2474	pF
C _{rss}	reverse transfer capacitance			-	310	682	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 0.8 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	22	-	ns
t _r	rise time			-	17	-	ns
t _{d(off)}	turn-off delay time			-	50	-	ns
t _f	fall time			-	20	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz; T _j = 25 °C		-	59	-	nC
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 15		-	0.77	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; Fig. 16		-	45	-	ns
Q _r	recovered charge		[1]	-	53	-	nC
t _a	reverse recovery rise time			-	25	-	ns
t _b	reverse recovery fall time			-	20	-	ns

[1] includes capacitive recovery



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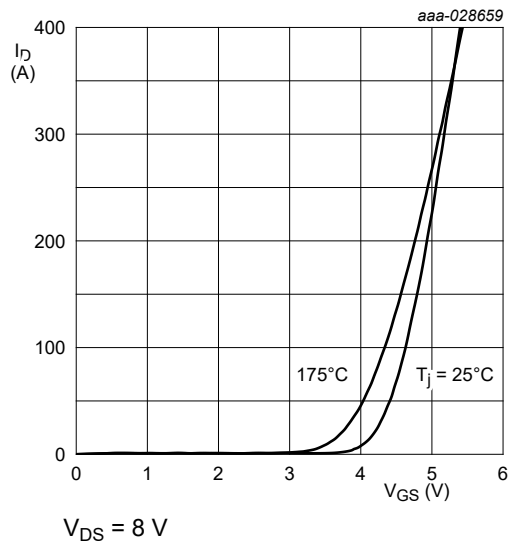


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

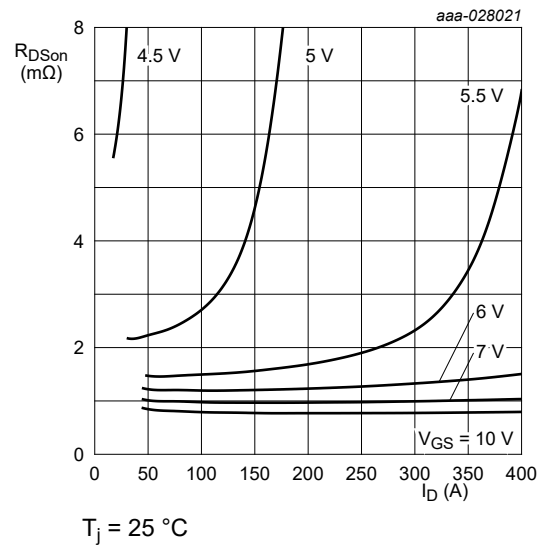


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

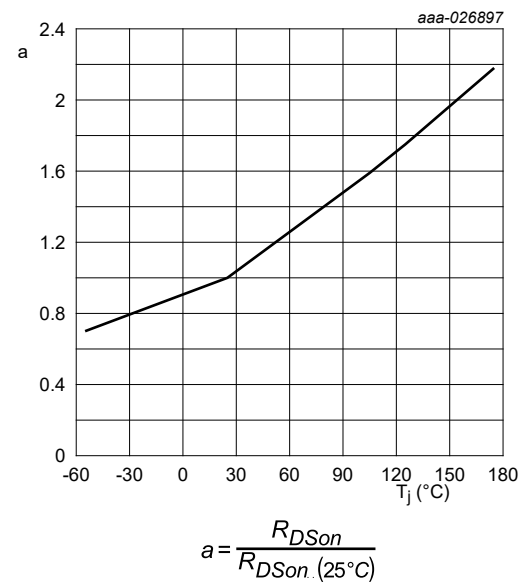


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

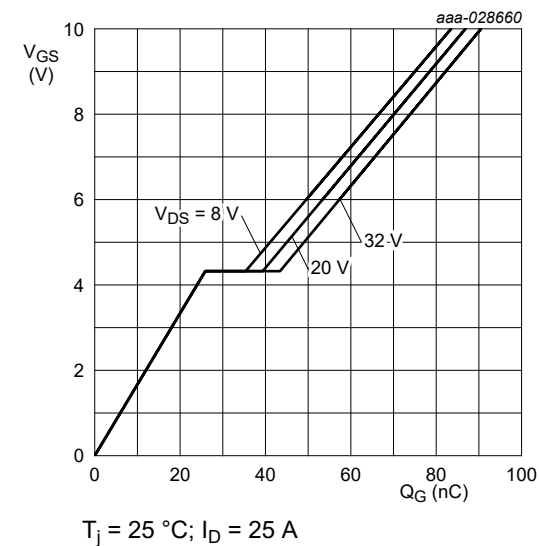


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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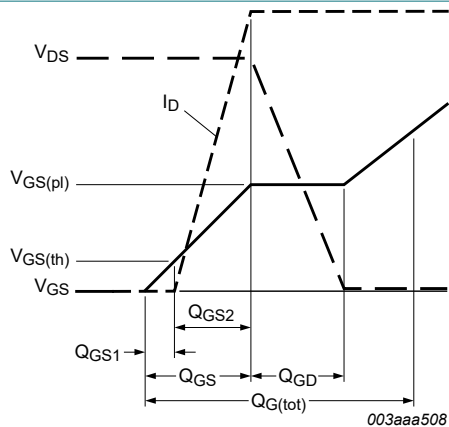
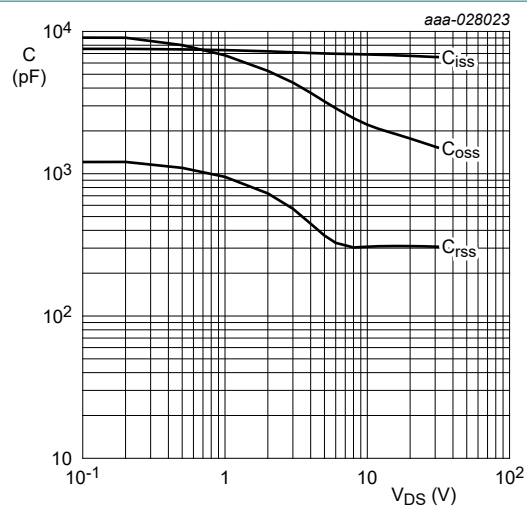
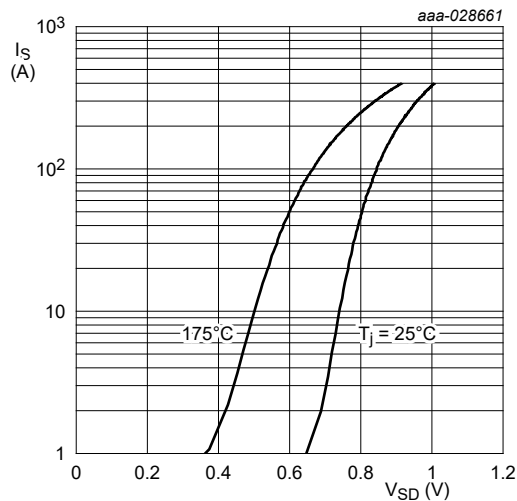


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

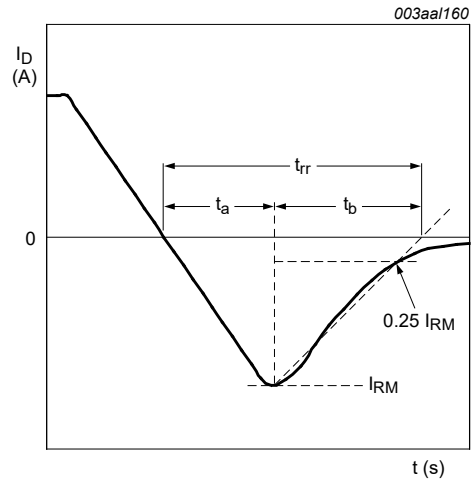


Fig. 16. Reverse recovery timing definition

11. Package outline

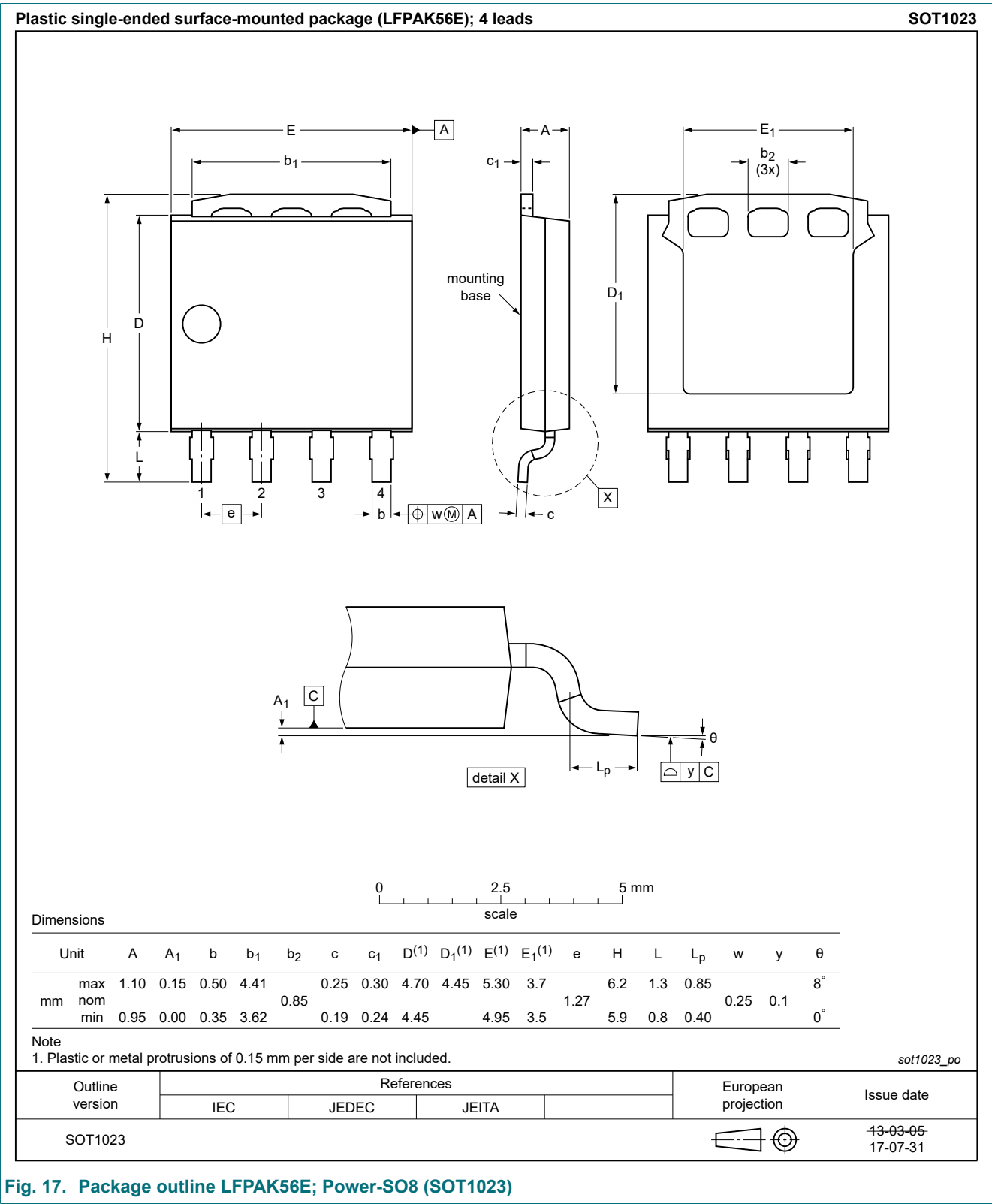


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

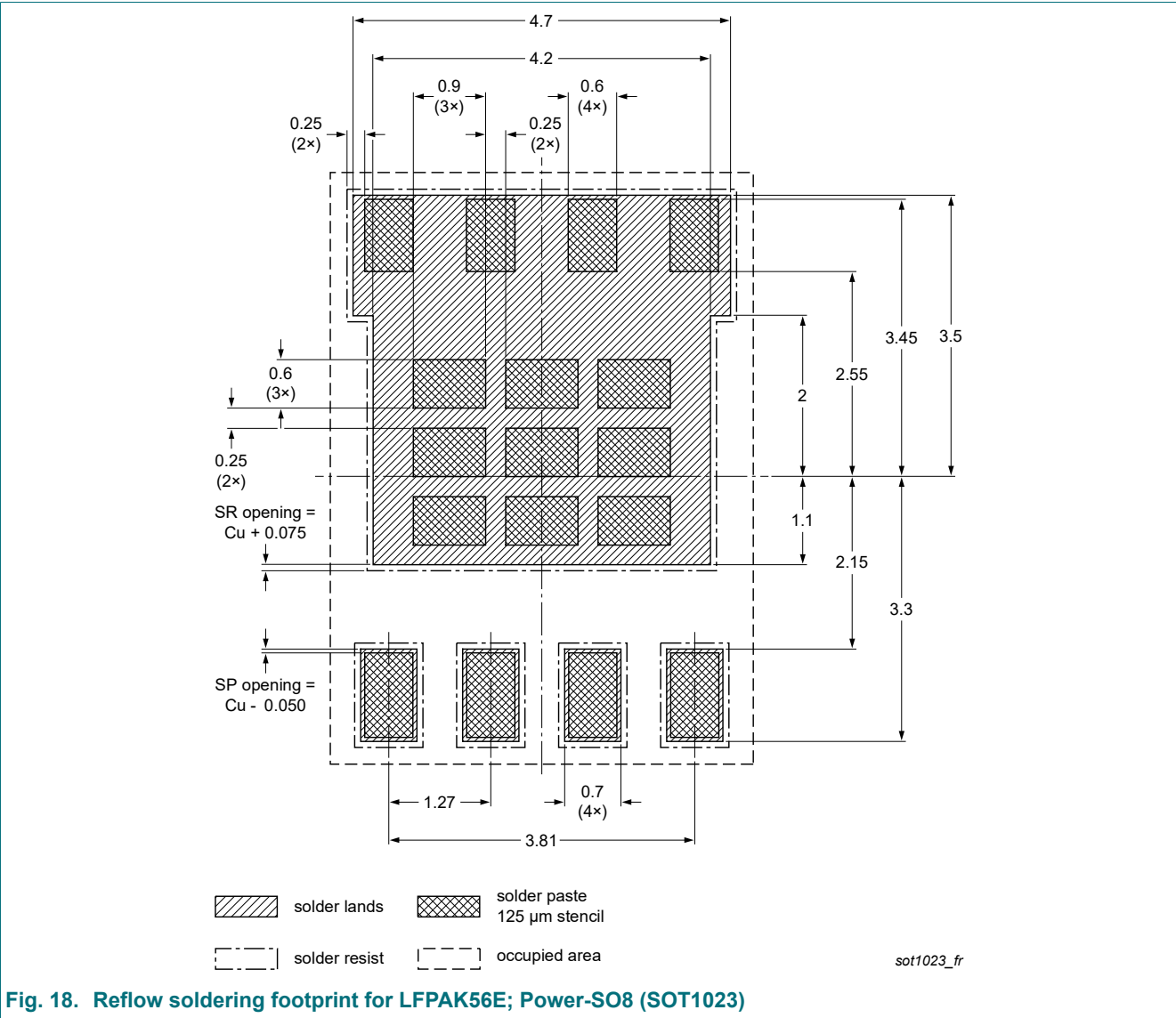


Fig. 18. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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