

PSMN057-200P

N-channel TrenchMOS SiliconMAX standard level FET Rev. 02 — 4 January 2011 Product de

Product data sheet

Product profile 1.

1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

DC-to-DC converters

Switched-mode power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit		
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	200	V		
I _D	drain current	T _{mb} = 25 °C	-	-	39	Α		
P _{tot}	total power dissipation		-	-	250	W		
Static characteristics								
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V; } I_D = 17 \text{ A;}$ $T_j = 25 \text{ °C}$	-	41	57	mΩ		
Dynamic c	Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10 \text{ V; } I_{D} = 39 \text{ A;}$ $V_{DS} = 160 \text{ V; } T_{j} = 25 \text{ °C}$	-	37	50	nC		



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	mb	D
3	S	source		_G (EA)
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			SOT78 (TO-220AB)	

3. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PSMN057-200P	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	200	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ	-	200	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{mb} = 100 °C	-	27.5	Α
		T _{mb} = 25 °C	-	39	Α
I _{DM}	peak drain current	pulsed; T _{mb} = 25 °C	-	156	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C	-	250	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drai	n diode				
Is	source current	T _{mb} = 25 °C	-	39	Α
I _{SM}	peak source current	pulsed; T _{mb} = 25 °C	-	156	Α
Avalanche r	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 35 A; V_{sup} ≤ 50 V; unclamped; t_p = 100 μs; R_{GS} = 50 Ω	-	300	mJ
I _{AS}	non-repetitive avalanche current	$V_{sup} \le 50 \text{ V; } V_{GS} = 10 \text{ V;}$ $T_{j(init)} = 25 \text{ °C; } R_{GS} = 50 \Omega; \text{ unclamped}$	-	35	Α

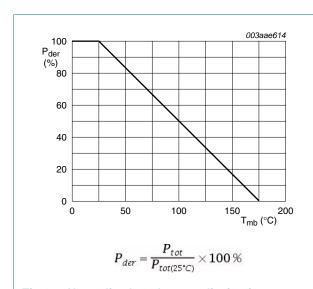


Fig 1. Normalized total power dissipation as a function of mounting base temperature

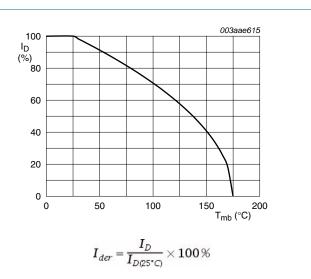


Fig 2. Normalized continuous drain current as a function of mounting base temperature

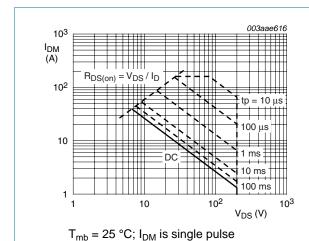


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

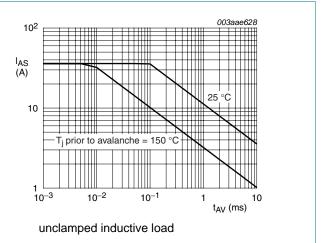


Fig 4. Single-shot avalanche rating; avalanche current as a function of avalanche period

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.6	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	-	60	-	K/W

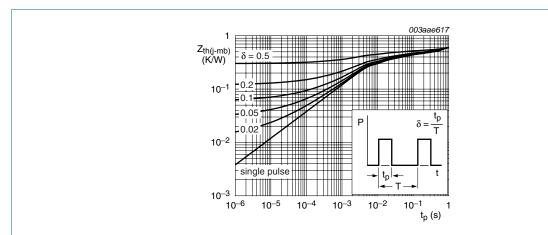


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source breakdown	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	178	-	-	V
	voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	200	-	-	V
$V_{GS(th)}$	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_i = -55 \text{ °C}$	-	-	6	V
	voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_i = 175 \text{ °C}$	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_i = 25 \text{ °C}$	2	3	4	V
I _{DSS}	drain leakage current	$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.03	10	μΑ
		$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_i = 175 \text{ °C}$	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 175 ^{\circ}\text{C}$	-	-	165	mΩ
	resistance	$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 25 \text{ °C}$	-	41	57	mΩ
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 39 \text{ A}; V_{DS} = 160 \text{ V}; V_{GS} = 10 \text{ V};$	-	96	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	13	-	nC
Q_{GD}	gate-drain charge		-	37	50	nC
C _{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	3750	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	385	-	pF
C _{rss}	reverse transfer capacitance		-	180	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 100 \text{ V}; R_L = 2.7 \Omega; V_{GS} = 10 \text{ V};$	-	18	-	ns
t _r	rise time	$R_{G(ext)} = 5.6 \Omega; T_j = 25 \degree C$	-	58	-	ns
t _{d(off)}	turn-off delay time		-	105	-	ns
t _f	fall time		-	78	-	ns
L _D	internal drain inductance	measured from drain lead to centre of die ; $T_j = 25 ^{\circ}\text{C}$	-	4.5	-	nΗ
		measured from tab to centre of die ; $T_j = 25 ^{\circ}\text{C}$	-	3.5	-	nΗ
L _S	internal source inductance	measured from source lead to source bond pad ; $T_j = 25$ °C	-	7.5	-	nΗ
Source-d	rain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	133	-	ns
Q _r	recovered charge	$V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	895	-	nC

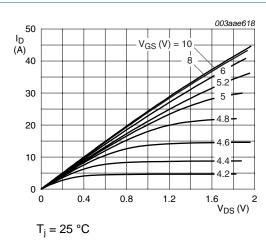


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

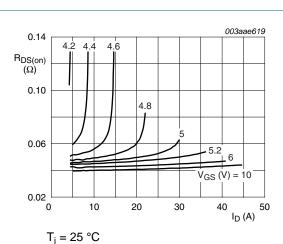


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

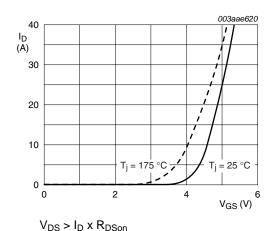


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

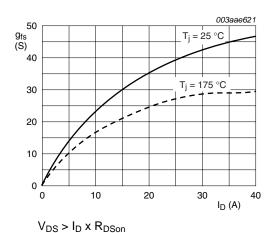


Fig 9. Forward transconductance as a function of drain current; typical values

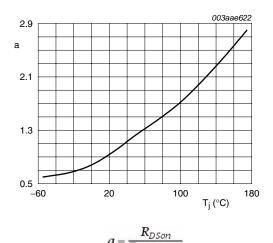
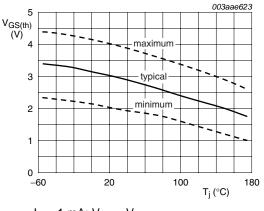


Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature

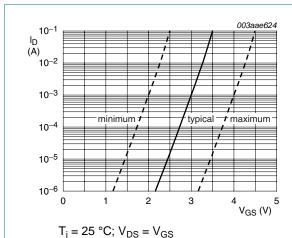
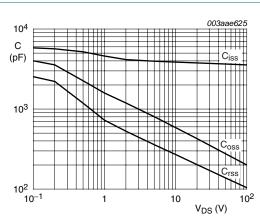


Fig 12. Sub-threshold drain current as a function of gate-source voltage



 $V_{GS} = 0 V$; f = 1 MHz

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

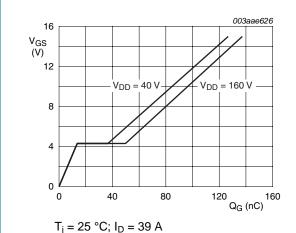
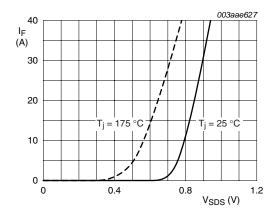


Fig 14. Gate-source voltage as a function of gate charge; typical values

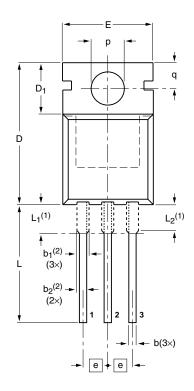


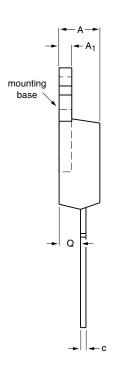
 $V_{GS} = 0 V$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB SOT78





0 5 10 mm

DIMENSIONS (mm are the original dimensions)

UNI	T A	A ₁	b	b ₁ (2)	b ₂ (2)	С	D	D ₁	E	е	L	L ₁ (1)	L ₂ ⁽¹⁾ max.	р	q	Q	
mm	1 4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2	

Notes

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig 16. Package outline SOT78 (TO-220AB)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
PSMN057-200P v.2	20110104	Product data sheet	-	PSMN057-200P v.1			
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 						
 Legal texts have been adapted to the new company name where appropriate. 							
PSMN057-200P v.1	20000601	Product specification	-	-			

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Nexperia

N-channel TrenchMOS SiliconMAX standard level FET

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