

PSMN017-30EL

N-channel 30 V 17 m Ω logic level MOSFET in I2PAK Rev. 2 — 3 April 2012 Produc

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel MOSFET in I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[1]	-	-	32	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	47	W
Tj	junction temperature			-55	-	175	°C
Static cha	racteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 13</u>		-	18.7	23.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 13</u>		-	13.4 17	17	mΩ
Dynamic o	characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; V_{DS} = 15 \text{ V};$		-	1.94	-	nC
Q _{G(tot)}	total gate charge	see Figure 14; see Figure 15		-	5.1	-	nC
Avalanche	ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 32 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω ; unclamped		-	-	13	mJ
							_

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		$G \longrightarrow A$
mb	D	mounting base; connected to drain		mbb076 S
			SOT226 (I2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN017-30EL	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

4. Limiting values

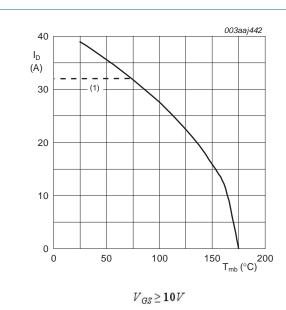
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u>	-	25.5	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	32	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$; see Figure 3		-	154	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	47	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	n diode					
Is	source current	T _{mb} = 25 °C		-	32	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	154	Α
Avalanche r	uggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 32 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω ; unclamped		-	13	mJ

^[1] Continuous current is limited by package.

PSMN017-30EL



(1) Capped at 32A due to package

Fig 1. Continuous drain current as a function of mounting base temperature

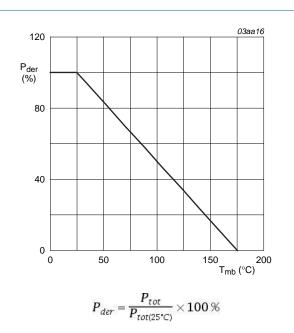
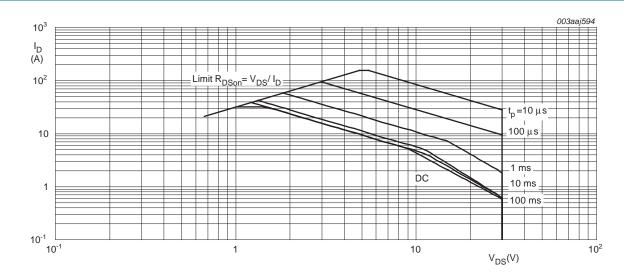


Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	3.18	3.2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		-	60	-	K/W

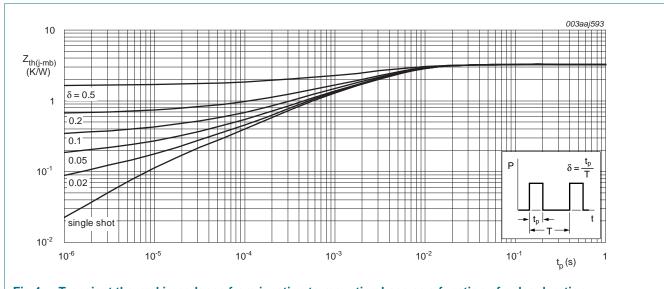


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source breakdown	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see Figure 10; see Figure 11	1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 175 °C; see <u>Figure 11</u>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	-	2.45	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.3	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 ^{\circ}\text{C}$	-	-	50	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 °C;$ see Figure 12	-	-	43.2	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 13	-	18.7	8.7 23.4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12	-	24	31.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ °C};$ see Figure 12	-	-	23.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 13	-	13.4	17	mΩ
R _G	gate resistance	f = 1 MHz	-	2.03	-	Ω
Dynamic	characteristics					
	total gate charge	$I_D = 10 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	10.7	-	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14; see Figure 15	-	9.55	-	nC
		$I_D = 10 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$;	-	5.1	-	nC
Q _{GS}	gate-source charge	see <u>Figure 14</u> ; see <u>Figure 15</u>	-	1.52	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	1	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	0.5	-	nC
Q _{GD}	gate-drain charge		-	1.94	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 \text{ A}$; $V_{DS} = 15 \text{ V}$; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.86	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	552	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	127	-	pF
C _{rss}	reverse transfer capacitance		-	64	-	pF

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}$; $R_L = 1.5 \Omega$; $V_{GS} = 4.5 \text{ V}$;	-	10.7	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$	-	9.2	-	ns
t _{d(off)}	turn-off delay time		-	11.4	-	ns
t _f	fall time		-	5.1	-	ns
Source-dr	ain diode					
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see Figure 17	-	0.89	1.2	V
t _{rr}	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	17.3	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	6.5	-	nC

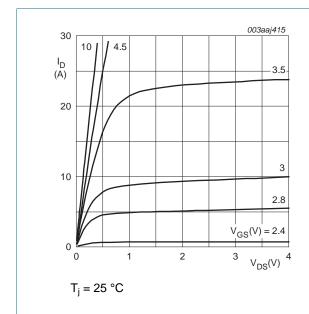


Fig 5. Output characteristics; drain current as a function of drain-source voltage; typical values

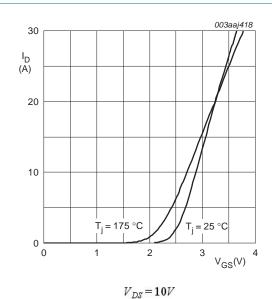


Fig 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

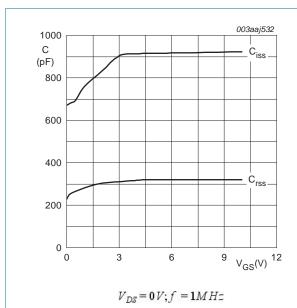


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

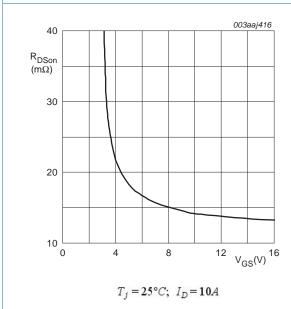


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

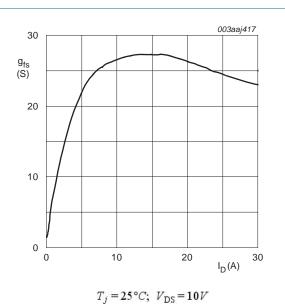
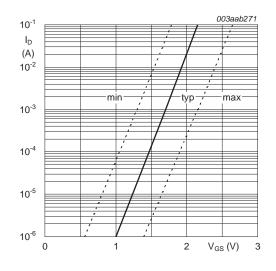


Fig 8. Forward transconductance as a function of drain current; typical values



 $T_j=25\,^{\circ}C; V_{DS}=5\,V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

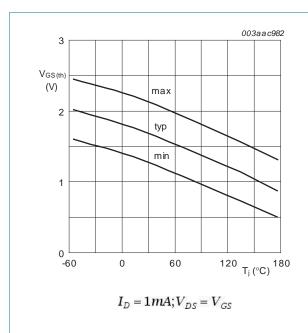


Fig 11. Gate-source threshold voltage as a function of junction temperature

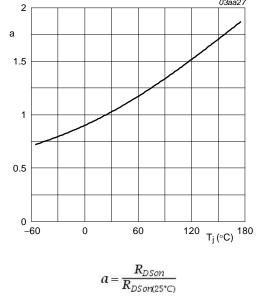


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

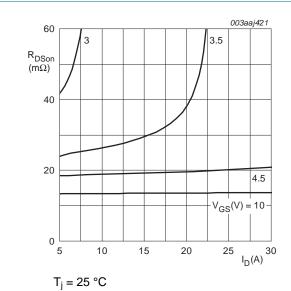


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

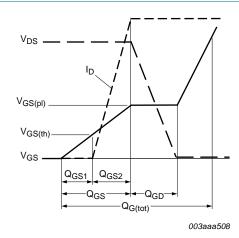


Fig 14. Gate charge waveform definitions

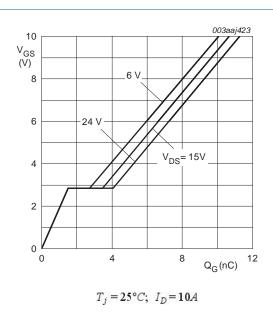
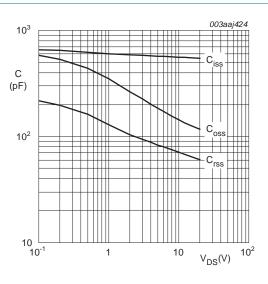
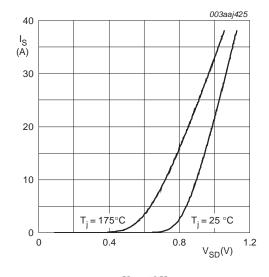


Fig 15. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = \mathbf{0}V; \ f = \mathbf{1}MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = \mathbf{0} V$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

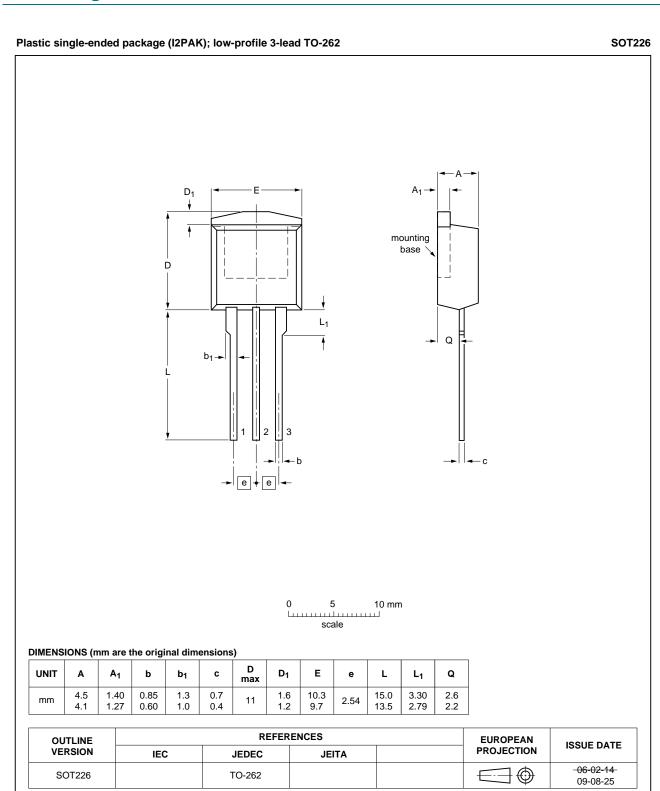


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN017-30EL v.2	20120403	Product data sheet	-	PSMN017-30EL v.1
Modifications:	 Status change 	d from objective to product.		
	 Various change 	es to content.		
PSMN017-30EL v.1	20120228	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1] [2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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N-channel 30 V 17 mΩ logic level MOSFET in I2PAK

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