PSMN012-60MS

N-channel 60 V 12 mΩ standard level MOSFET in LFPAK33 19 December 2019 Product data sheet

1. General description

Standard level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of motor, industrial, communications and domestic equipment.

2. Features and benefits

- · High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- LFPAK33 package is footprint compatible with other 3.3 mm footprint types
- Qualified to 175 °C

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	60	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	-	53	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	-	75	W
Tj	junction temperature		-55	-	175	°C
Static chara	acteristics		•	'		
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 15 A; T_{j} = 25 °C; Fig. 11	-	10	12	mΩ
Dynamic ch	naracteristics		•	'		
Q_{GD}	gate-drain charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 10 V;	-	8.5	-	nC
Q _{G(tot)}	total gate charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	24.8	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	Source		D
2	S	Source		
3	S	Source		$G \longrightarrow G$
4	G	Gate		mbb076 S
mb	D	Mounting base; connected to drain	1 2 3 4 LFPAK33 (SOT1210)	



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6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN012-60MS	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN012-60MS	M12S60

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$		-	60	V
V_{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	75	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>		-	53	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>		-	37	А
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3		-	211	А
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain	n diode		'			
I _S	source current	T _{mb} = 25 °C		-	53	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	211	Α
Avalanche ru	uggedness	•		'		,
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 53 A; $V_{sup} \le 60$ V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1]	-	34.3	mJ

^[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 $^{\circ}\text{C}.$

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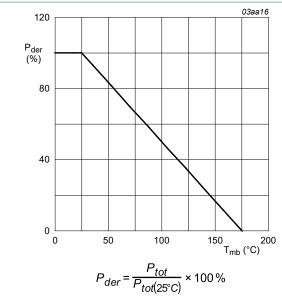


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

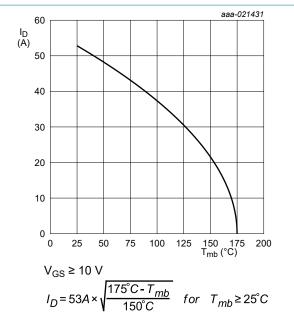
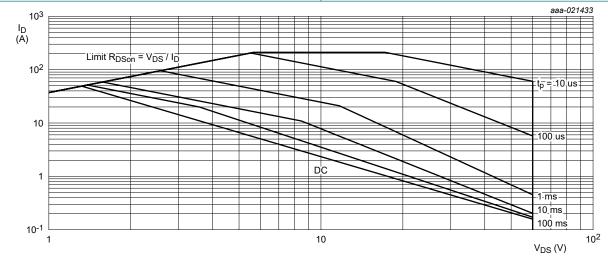


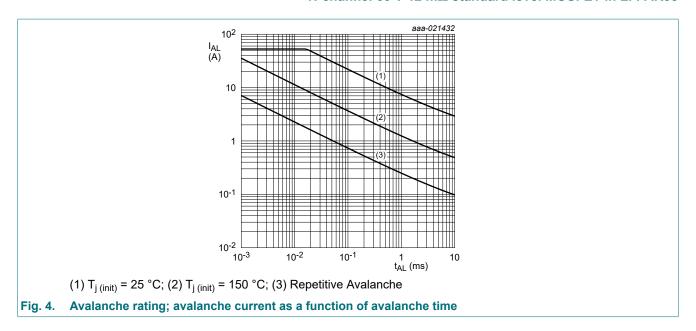
Fig. 2. Continuous drain current as a function of mounting base temperature



 T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

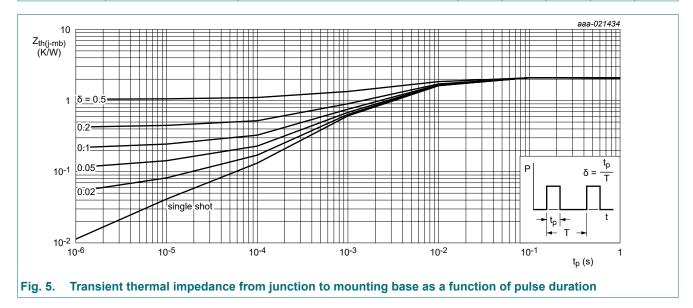
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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<u>Fig. 5</u>	-	1.82	2	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static chara	cteristics		•		·		
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
,	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$		54	-	-	V

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 9$	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_{D} = 15 A; T_{j} = 25 °C; Fig. 11	-	10	12	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 ^{\circ}\text{C};$ Fig. 12		-	27	mΩ
Dynamic ch	naracteristics		,	'	1	
Q _{G(tot)}	total gate charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 10 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	24.8	-	nC
Q _{GS}	gate-source charge		-	5.6	-	nC
Q _{GD}	gate-drain charge		-	8.5	-	nC
C _{iss}	input capacitance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ °C};$ Fig. 12 $I_D = 15 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}; \text{ Fig. 13}; \text{ Fig. 14}$ $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ Fig. 15}$	-	1222	1625	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	167	200	pF
C _{rss}	reverse transfer capacitance		-	104	143	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 45 \text{ V}; R_L = 3 \Omega; V_{GS} = 10 \text{ V};$	-	6.6	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	9.7	-	ns
t _{d(off)}	turn-off delay time		-	17.4	-	ns
t _f	fall time		-	10.5	-	ns
Source-drai	in diode		,	'		
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; <u>Fig. 16</u>	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	19.5	-	ns
Q _r	recovered charge	V _{DS} = 25 V; T _j = 25 °C	-	16.6	-	nC
		I				

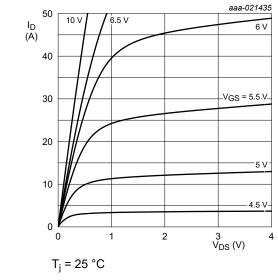


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

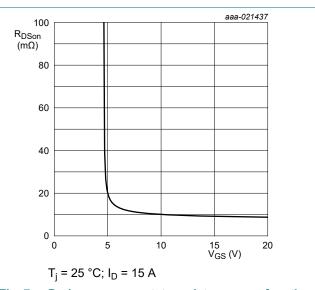


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

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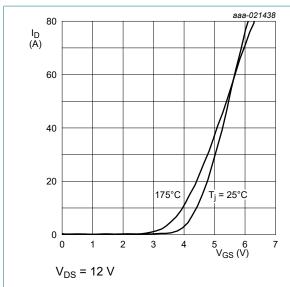


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

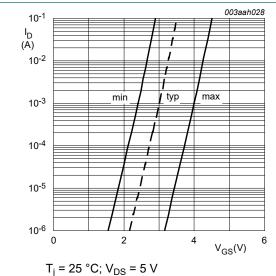


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

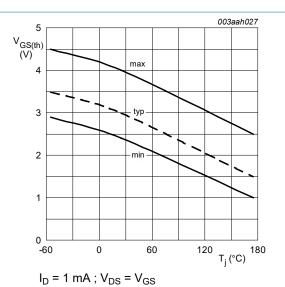


Fig. 9. Gate-source threshold voltage as a function of junction temperature

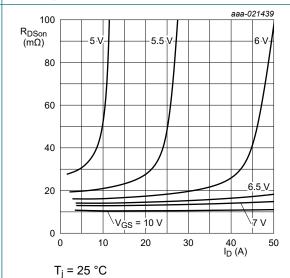


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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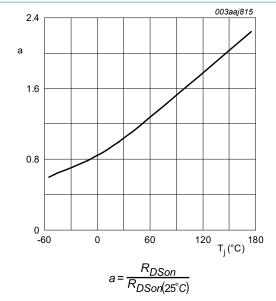


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

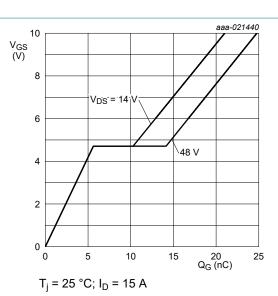


Fig. 13. Gate-source voltage as a function of gate charge; typical values

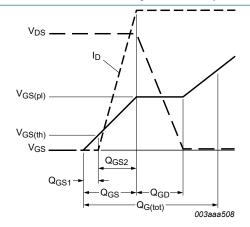


Fig. 14. Gate charge waveform definitions

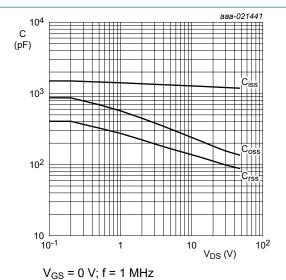


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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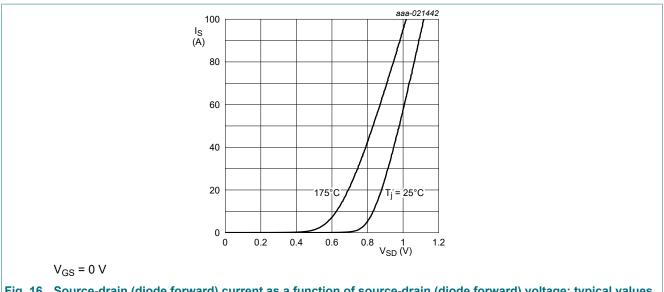


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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11. Package outline

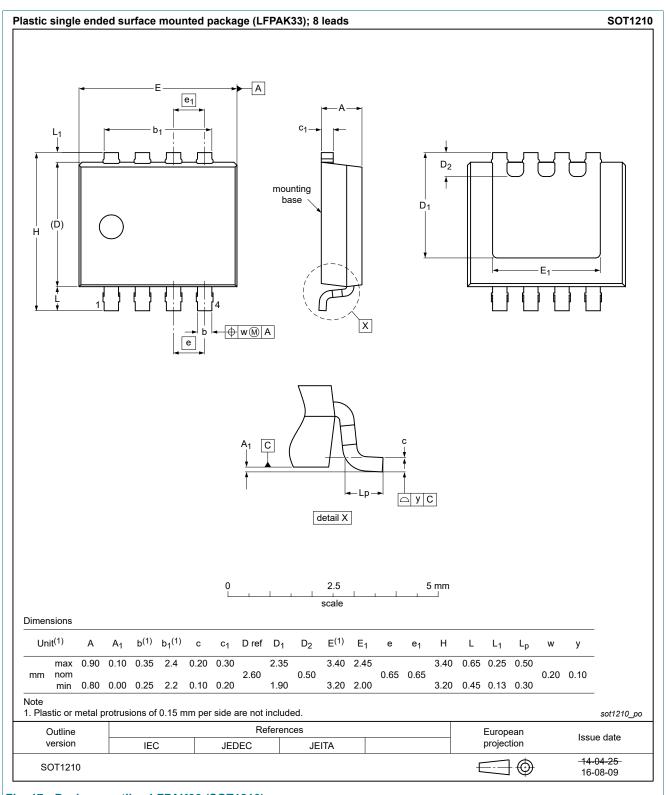
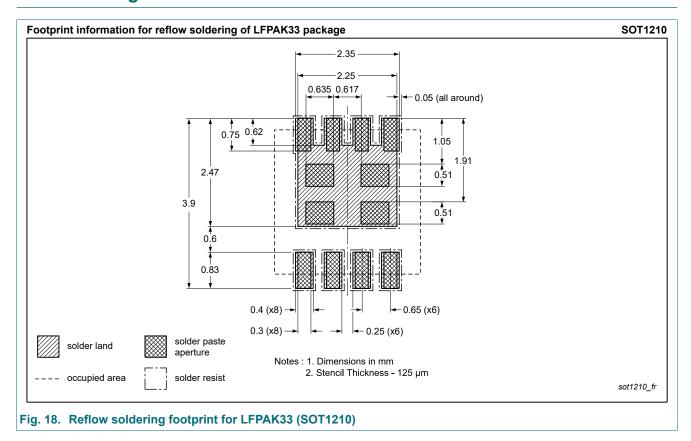


Fig. 17. Package outline LFPAK33 (SOT1210)

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12. Soldering



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13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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