



PSMN011-60MS

N-channel 60 V 11.3 mΩ standard level MOSFET in LPAK33

4 June 2013

Product data sheet

1. General description

Standard level enhancement mode N-channel MOSFET in LPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources
- LPAK33 package is footprint compatible with other 3.3mm types
- Qualified to 175 °C

3. Applications

- AC-to-DC converters
- Synchronous rectification
- DC-DC converters

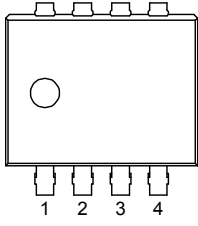
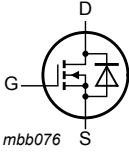
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	-	61	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	-	91	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	9.6	11.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14 ; Fig. 15	-	5.8	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN011-60MS	LPAK33	Plastic single ended surface mounted package (LPAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN011-60MS	M11S60

8. Limiting values

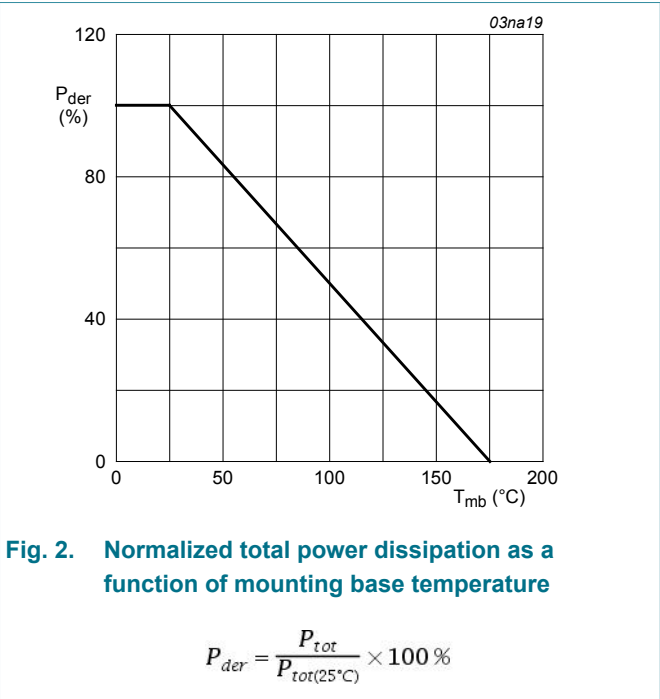
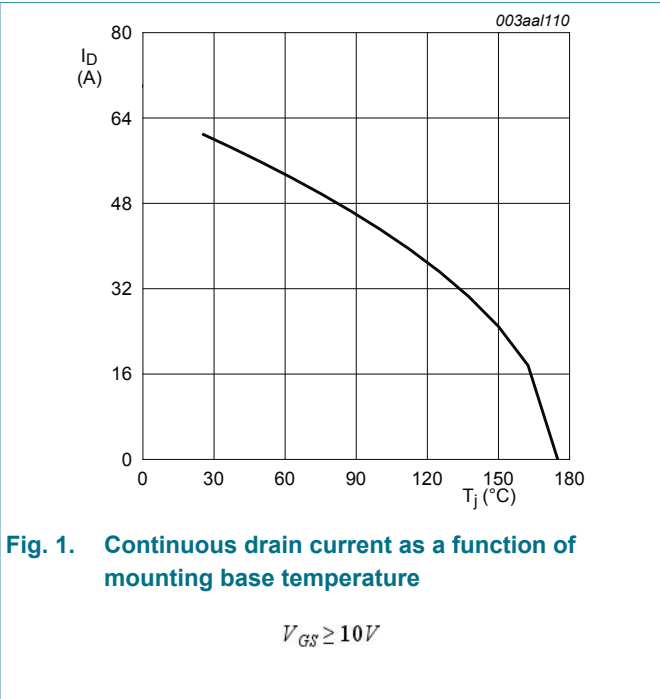
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	-	61	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1	-	43	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 4	-	244	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	91	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	70	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	244	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 61 A; V _{sup} ≤ 60 V; R _{GS} = 50 Ω; unclamped; Fig. 3		-	48.1	mJ

[1] Continuous current is limited by package



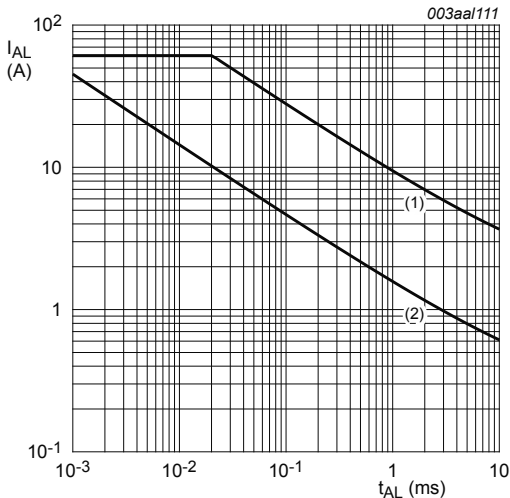


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_j (int) = 25^\circ C$; (2) $T_j (int) = 100^\circ C$

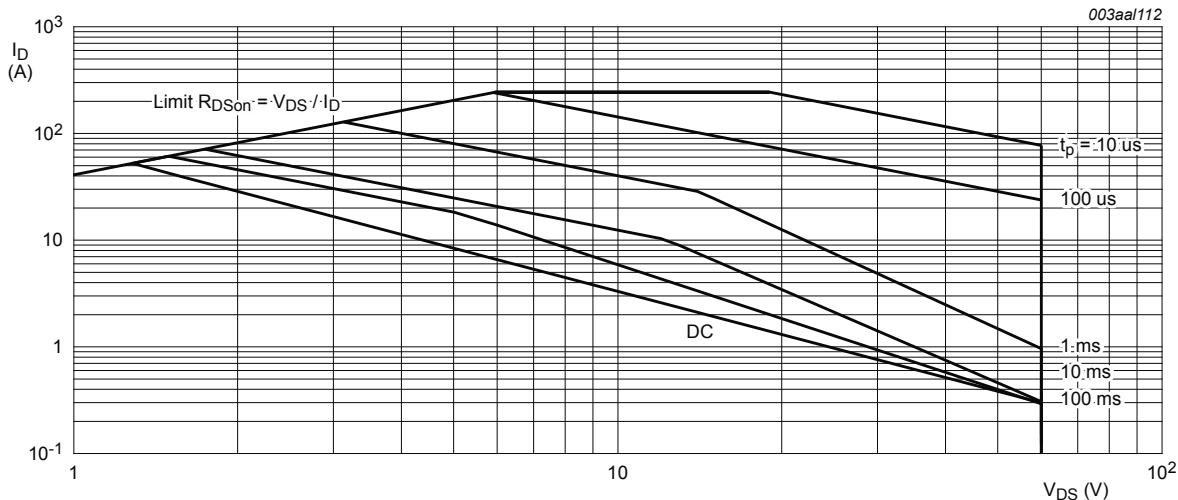


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.44	1.65	K/W

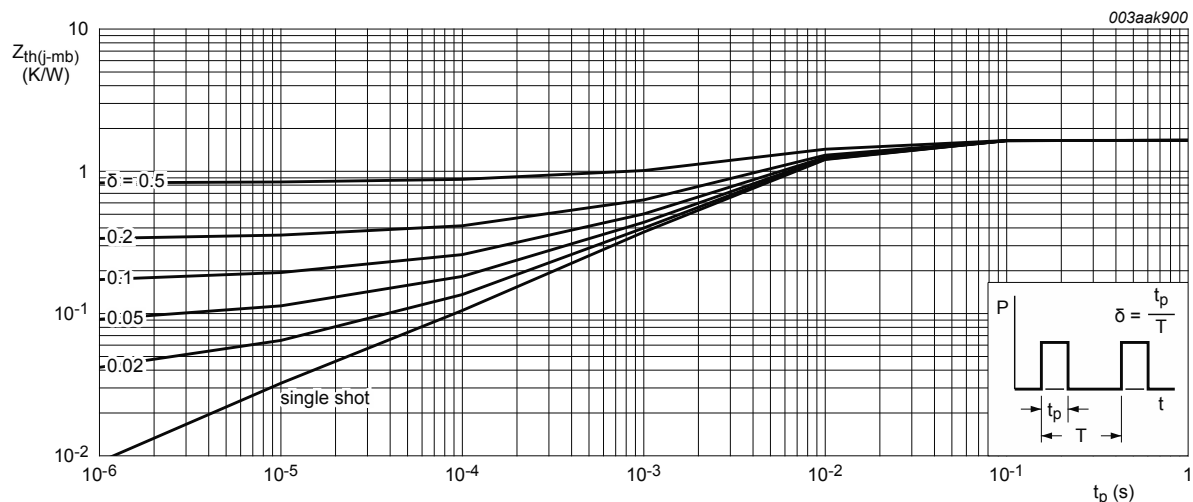


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 ^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 ^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 175 ^\circ C$; Fig. 10	1	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 25 ^\circ C$; Fig. 10 ; Fig. 11	2.3	3	4	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_J = -55 ^\circ C$; Fig. 10	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_J = 25 ^\circ C$	-	0.054	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_J = 175 ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_J = 25 ^\circ C$; Fig. 12	-	9.6	11.3	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_J = 175 ^\circ C$; Fig. 13	-	-	24.4	mΩ
R_G	gate resistance	$f = 1 MHz$	-	2.75	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 30 V; V_{GS} = 10 V$; $T_J = 25 ^\circ C$; Fig. 14 ; Fig. 15	-	23	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GS}	gate-source charge	I _D = 15 A; V _{DS} = 30 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	6.1	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	3.9	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	2.2	-	nC
Q _{GD}	gate-drain charge			-	5.8	-	nC
C _{iss}	input capacitance	V _{DS} = 30 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	1368	-	pF
C _{oss}	output capacitance			-	191	-	pF
C _{rss}	reverse transfer capacitance			-	108	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	6.7	-	ns
t _r	rise time			-	8.46	-	ns
t _{d(off)}	turn-off delay time			-	16.9	-	ns
t _f	fall time			-	9.18	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.84	1.2	V
t _{rr}	reverse recovery time	I _S = 15 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 30 V; T _j = 25 °C		-	21.7	-	ns
Q _r	recovered charge			-	19.2	-	nC

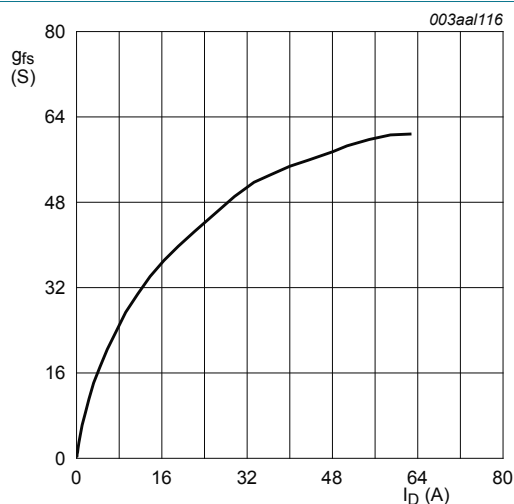


Fig. 6. Forward transconductance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$$

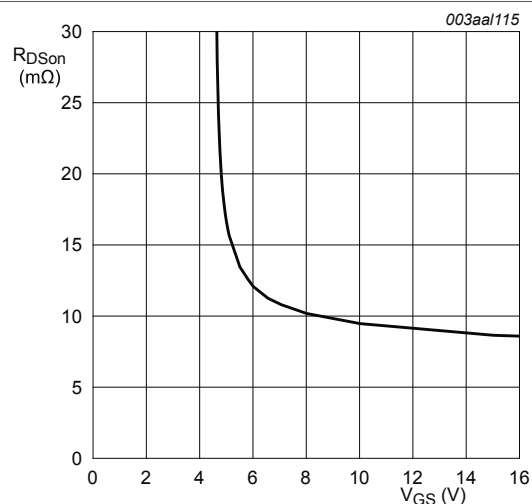
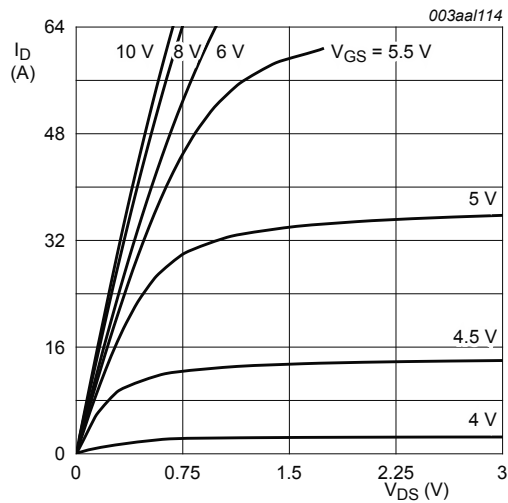


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^\circ\text{C}; I_D = 15\text{ A}$$



$T_j = 25\text{ }^{\circ}\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

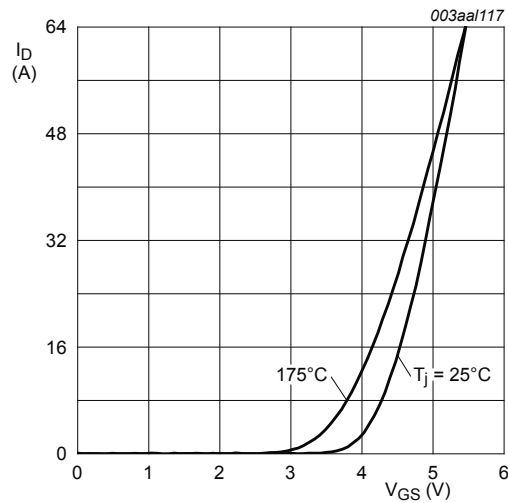


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

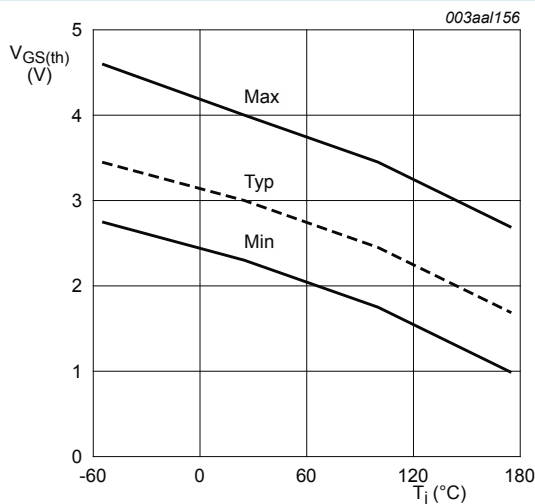


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

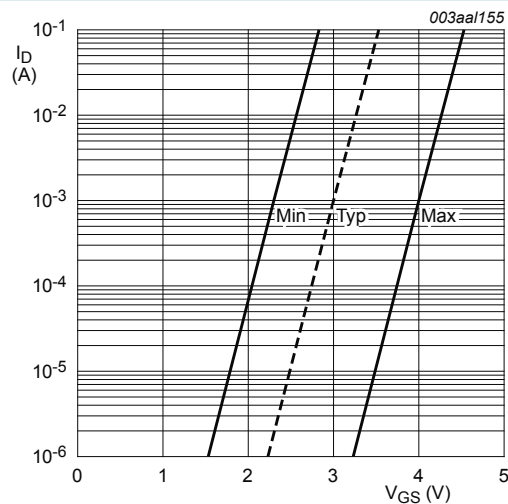


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 5\text{ V}$

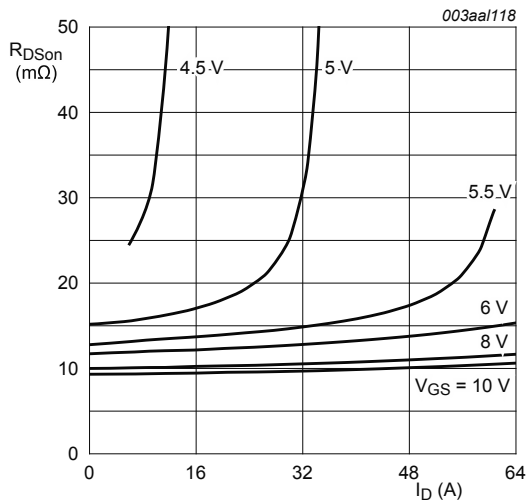


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

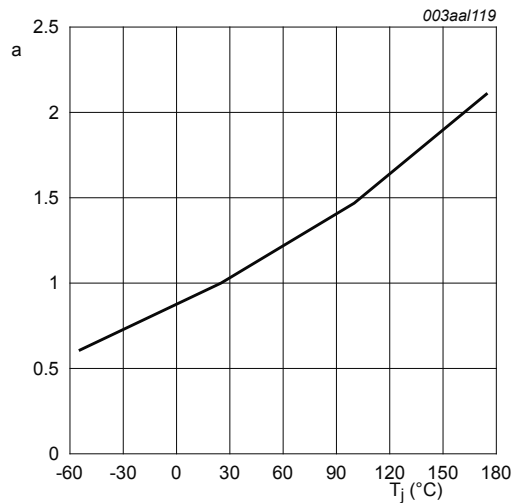


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

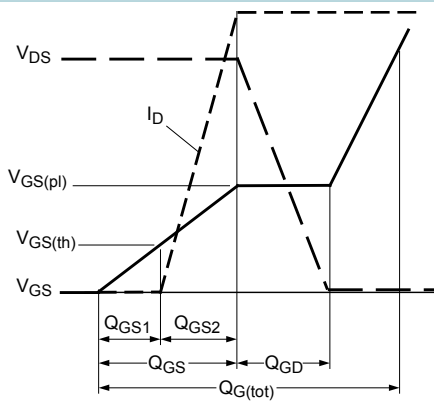


Fig. 14. Gate charge waveform definitions

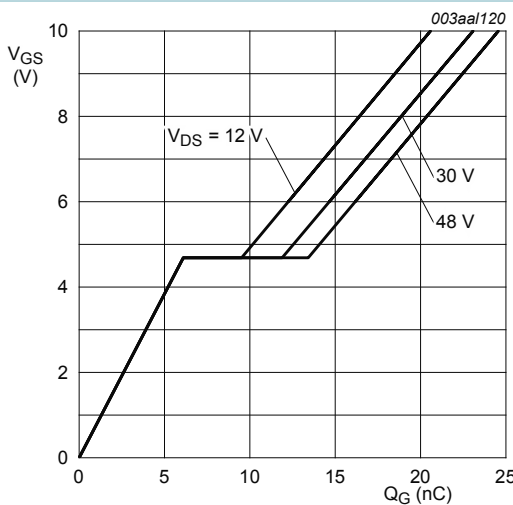


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 15\text{ A}$$

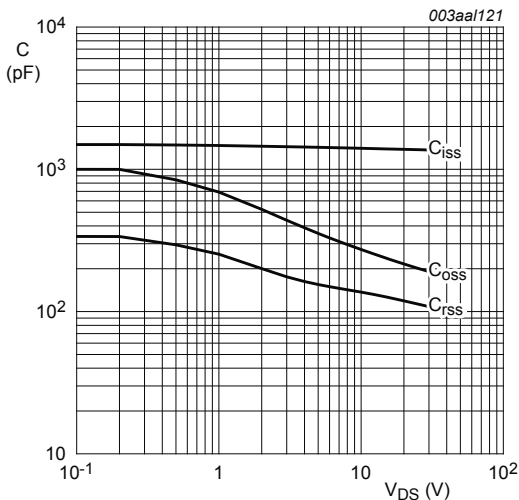


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS}=0V; f=1MHz$

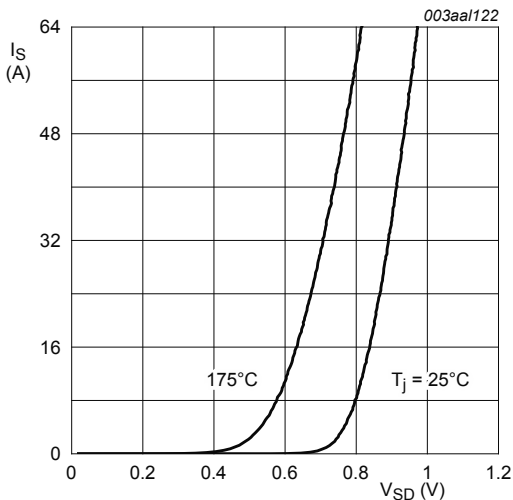


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS}=0V$

11. Package outline

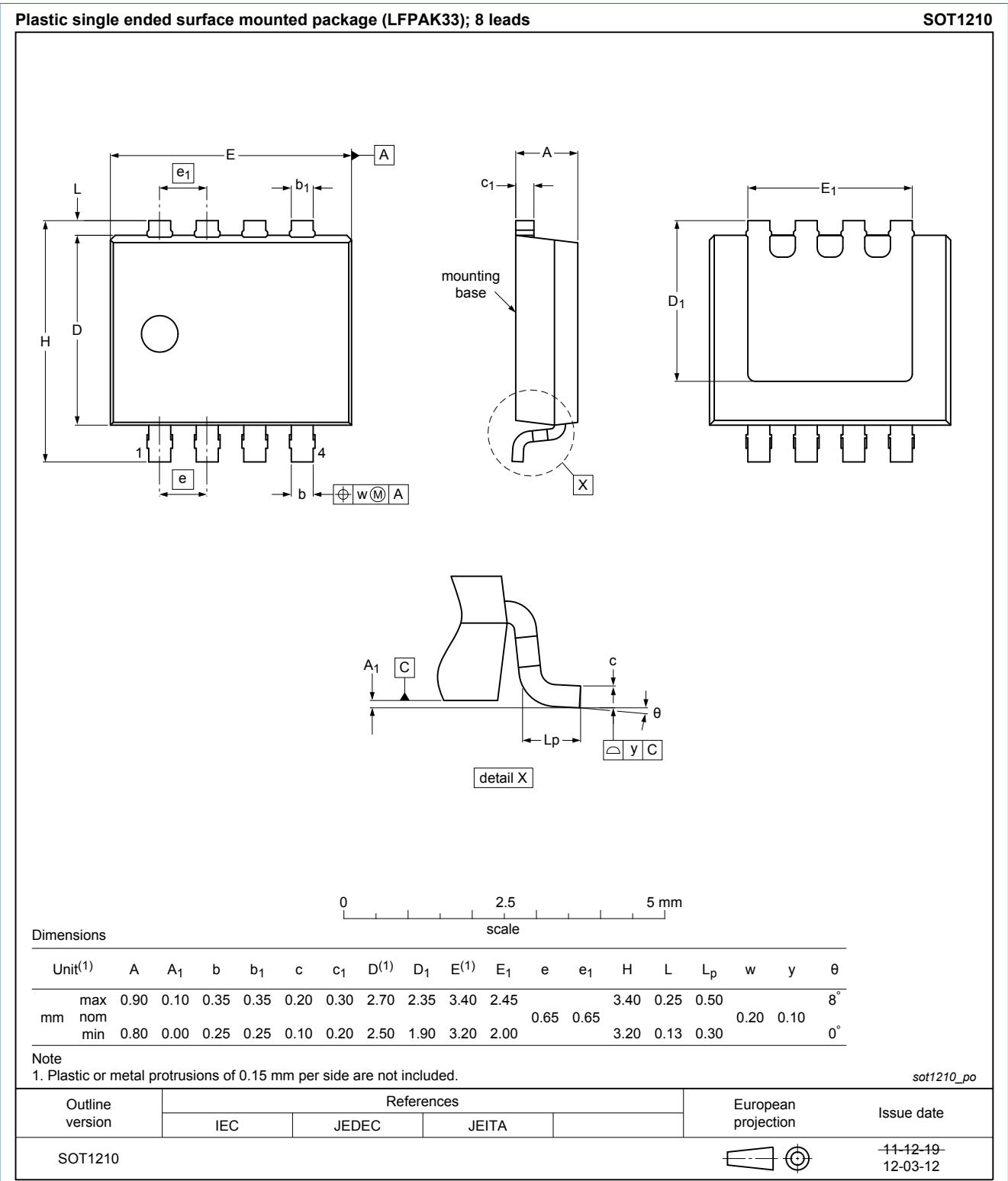


Fig. 18. Package outline LPAK33 (SOT1210)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12

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