



PIMC32-Q

50 V, 500 mA NPN/PNP Resistor-Equipped double Transistor (RET); R1 = 2.2 kΩ, R2 = 10 kΩ

16 February 2022

Product data sheet

1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PIMN32-Q

PNP/PNP complement: PIMP32-Q

2. Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital applications
- Cost-saving alternative to BC807-Q / BC817-Q series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

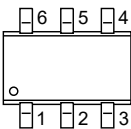
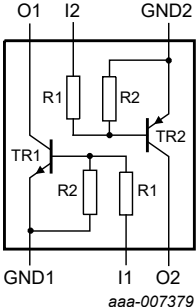
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity where applicable						
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	500	mA
R1	bias resistor 1 (input)	[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio	[1]	4.1	4.55	5	

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 SC-74; TSOP6 (SOT457)	 aaa-007379
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PIMC32-Q	SC-74; TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PIMC32-Q	4H

8. Limiting values

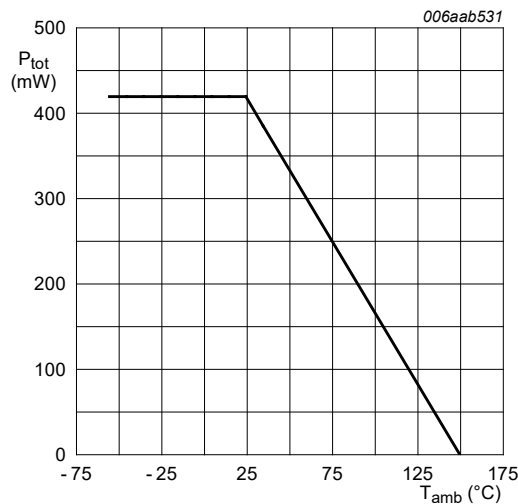
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity where applicable						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
V_I	input voltage			-5	12	V
I_O	output current			-	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	290	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	420	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.

50 V, 500 mA NPN/PNP Resistor-Equipped double Transistor (RET); R1 = 2.2 kΩ, R2 = 10 kΩ



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

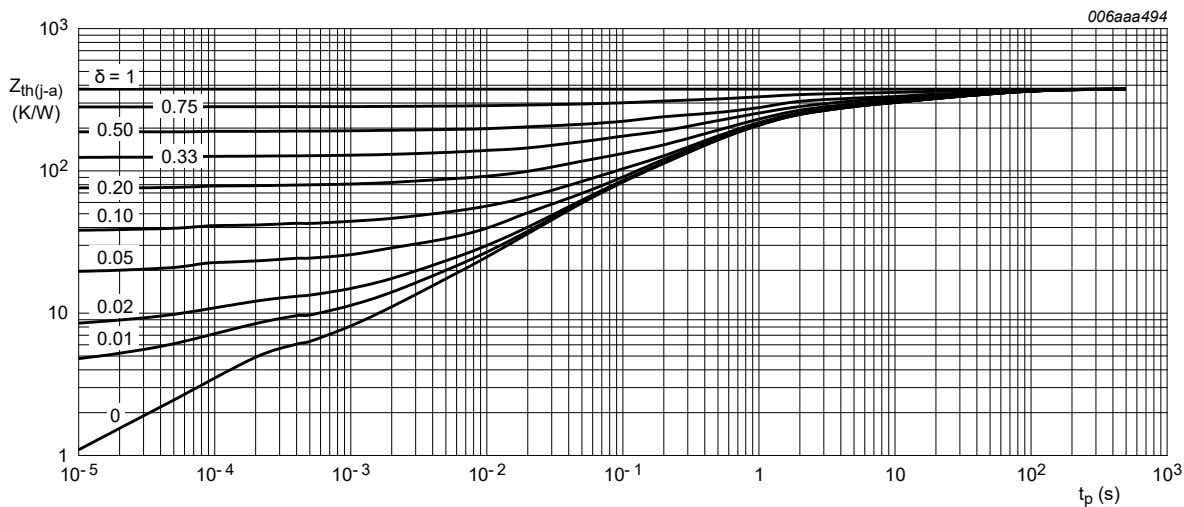
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	432	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	105	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	298	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35μm copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity where applicable							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\ \mu\text{A}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10\ \text{mA}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\ \text{V}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50\ \text{V}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	-	0.5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\ \text{V}$; $I_C = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	-	0.65	mA
h_{FE}	DC current gain	$V_{CE} = 5\ \text{V}$; $I_C = 50\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		70	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\ \text{mA}$; $I_B = 2.5\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\ \text{V}$; $I_C = 100\ \mu\text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		0.4	0.65	1	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\ \text{V}$; $I_C = 20\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		0.5	0.95	1.4	V
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	4.1	4.55	5	
TR1 (NPN)							
C_c	collector capacitance	$V_{CB} = 10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	7	-	pF
f_T	transition frequency	$V_{CE} = 5\ \text{V}$; $I_C = 50\ \text{mA}$; $f = 100\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	[2]	-	225	-	MHz
TR2 (PNP)							
C_c	collector capacitance	$V_{CB} = -10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$		-	11	-	pF
f_T	transition frequency	$V_{CE} = -5\ \text{V}$; $I_C = -50\ \text{mA}$; $f = 100\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	[2]	-	140	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor

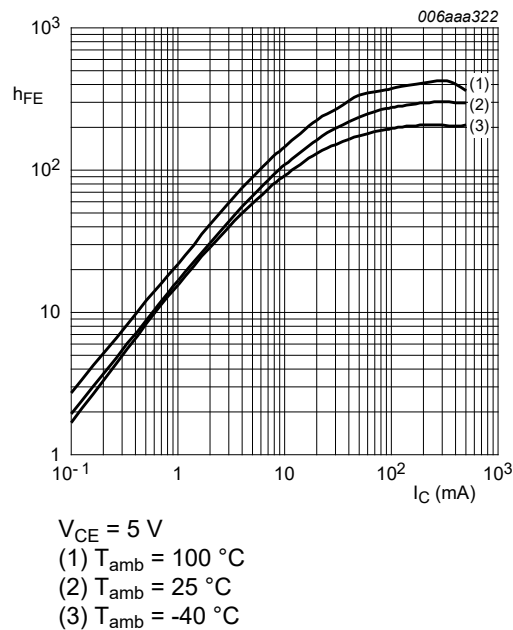


Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

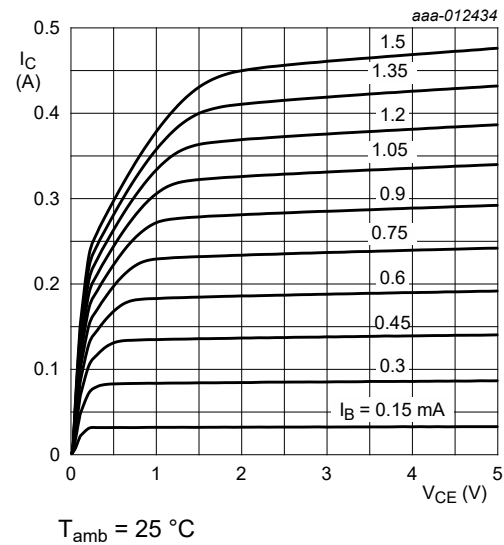


Fig. 4. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

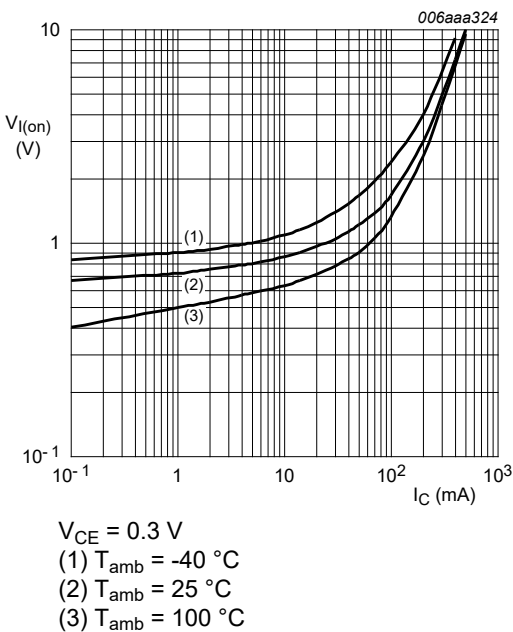


Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values

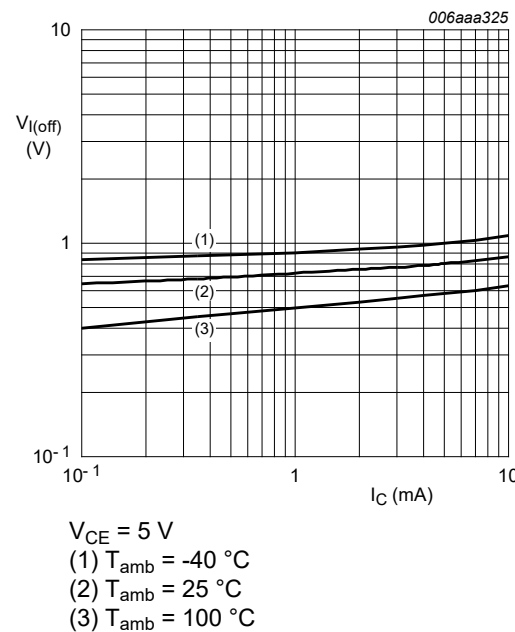
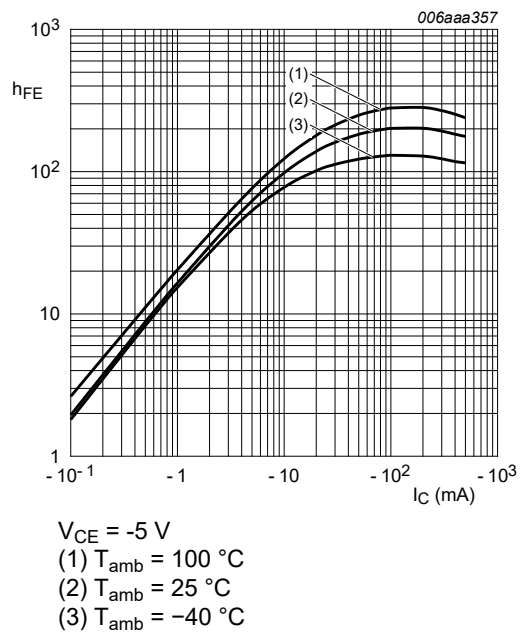
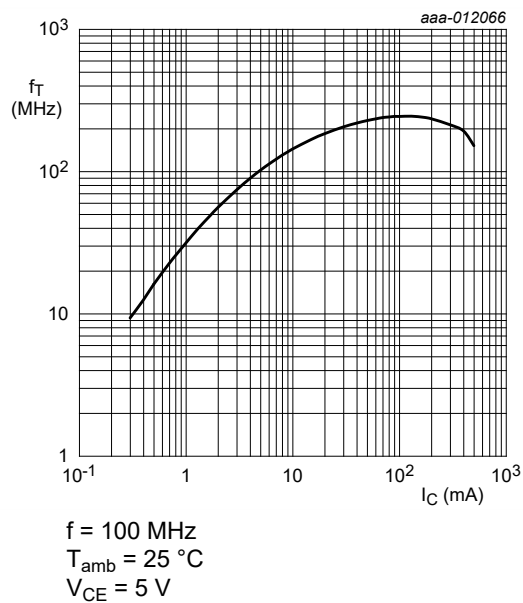
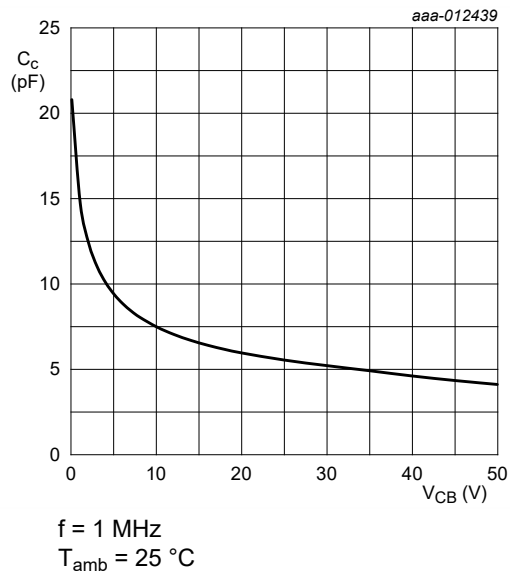
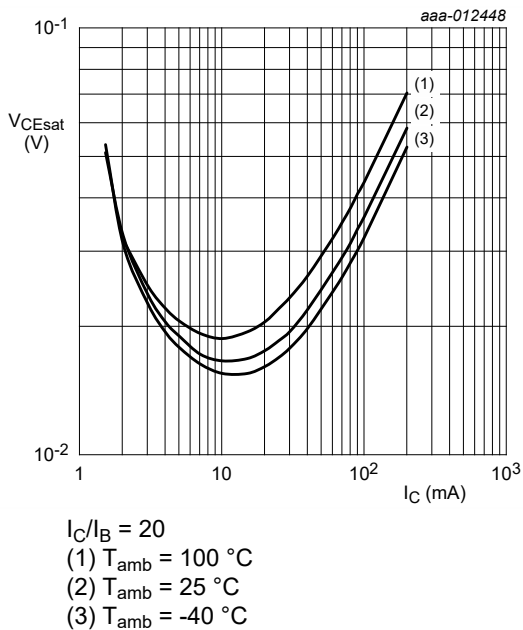


Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



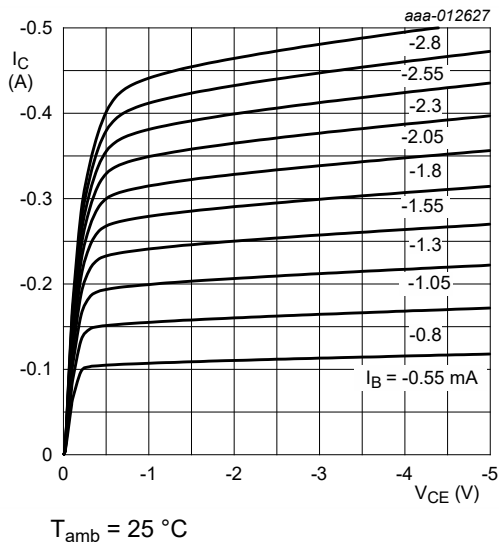


Fig. 11. TR2 (PNP): Collector current as a function of collector-emitter voltage, typical values

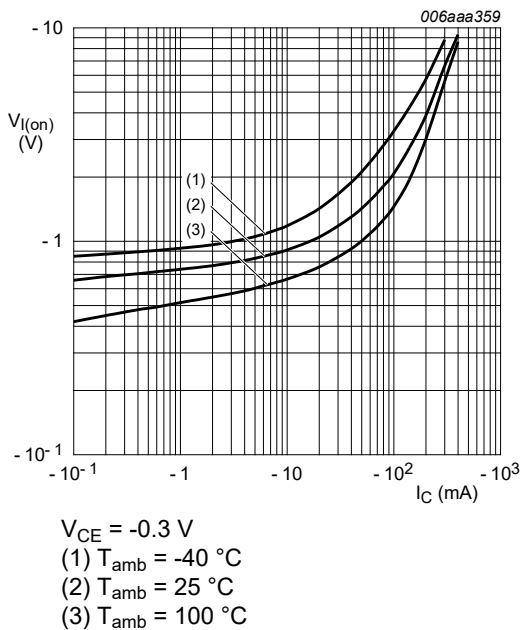


Fig. 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values

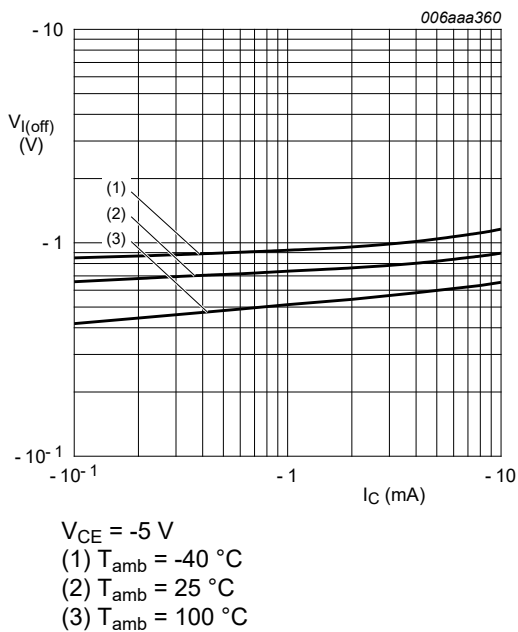


Fig. 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

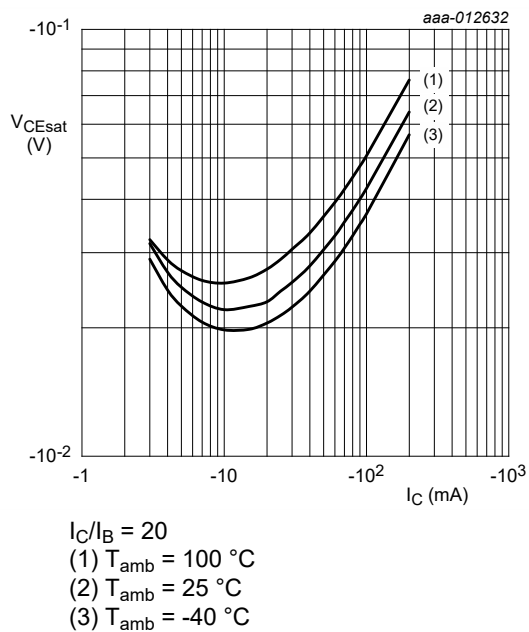


Fig. 14. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

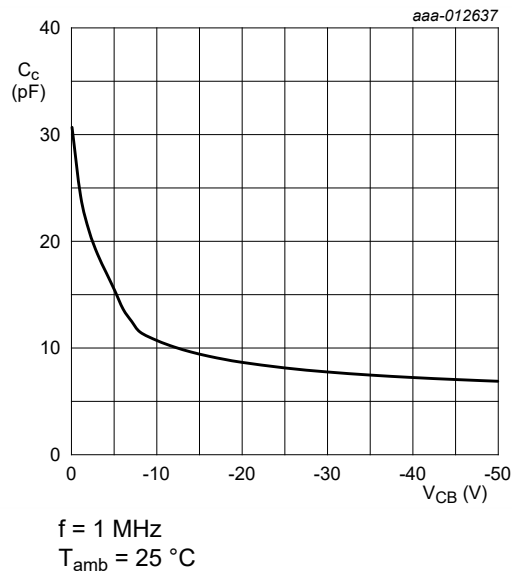


Fig. 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

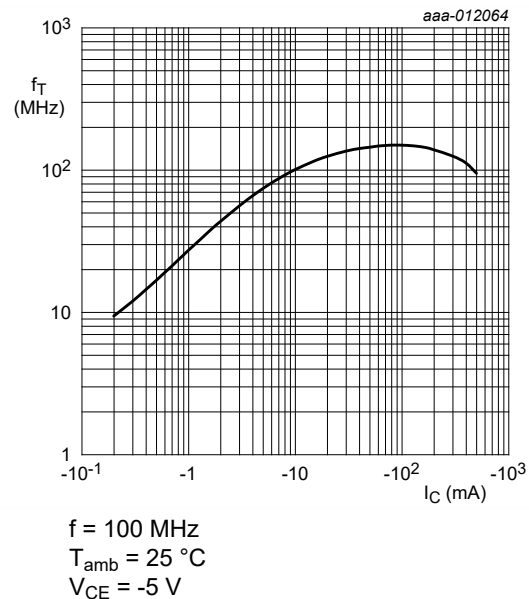


Fig. 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$RI = \frac{V(I_{I2}) - V(I_{II})}{I_{I2} - I_{II}}$$

- Calculation of bias resistor ratio (R_2/R_1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

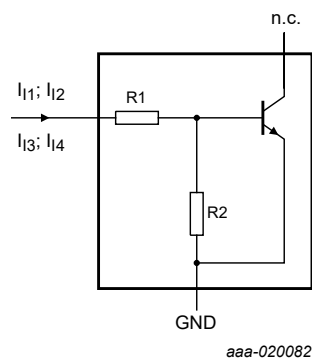


Fig. 17. TR1 (NPN): Resistor test circuit

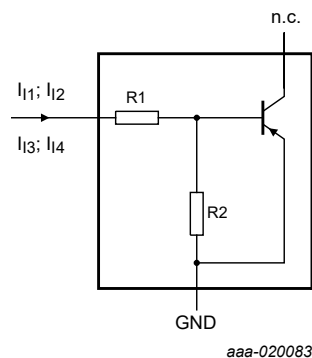


Fig. 18. TR2 (PNP): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

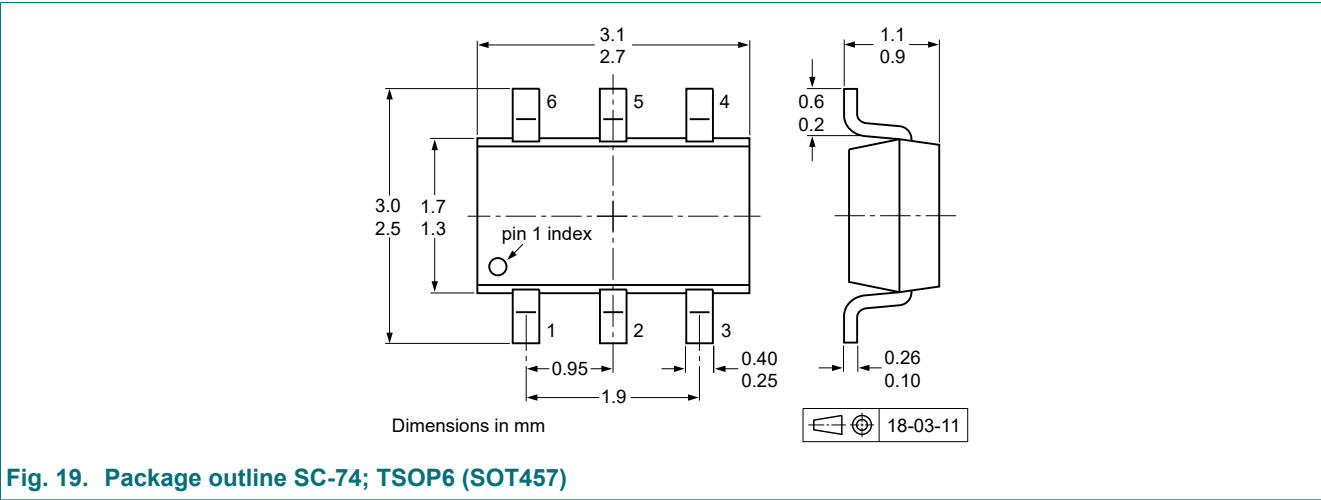
Per transistor; for the PNP transistor with negative polarity

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I _{I1}	I _{I2}	I _{I3}	I _{I4}
2.2	10	0.7 mA	0.8 mA	-0.45 mA	-0.55 mA

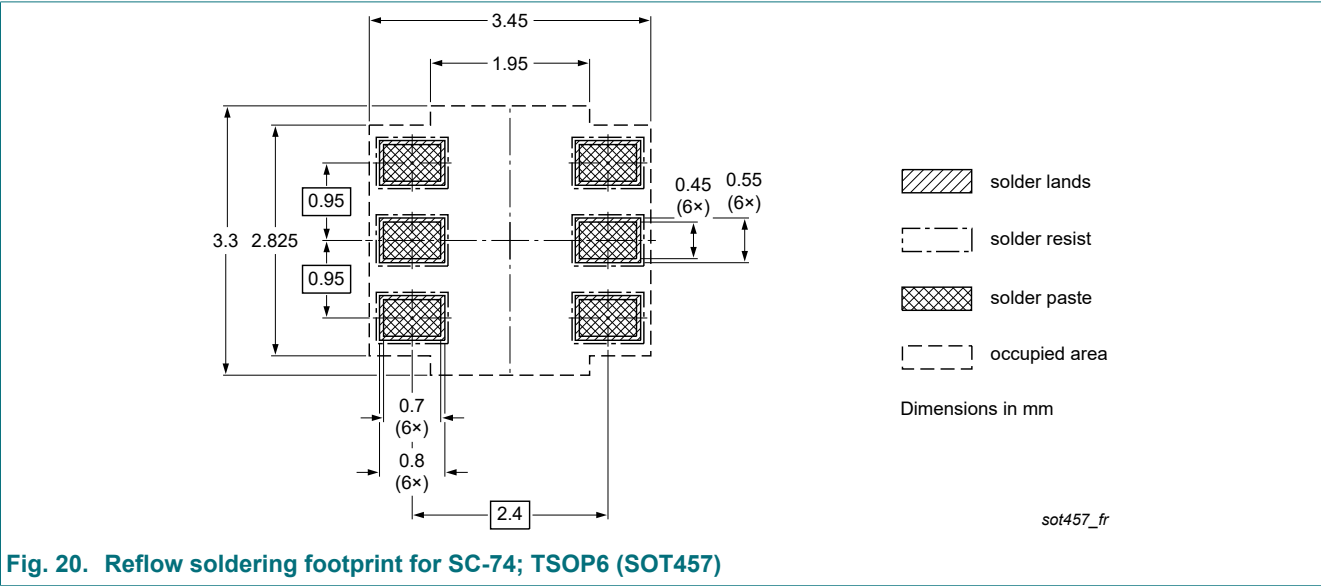
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



50 V, 500 mA NPN/PNP Resistor-Equipped double Transistor (RET); R1 = 2.2 kΩ, R2 = 10 kΩ

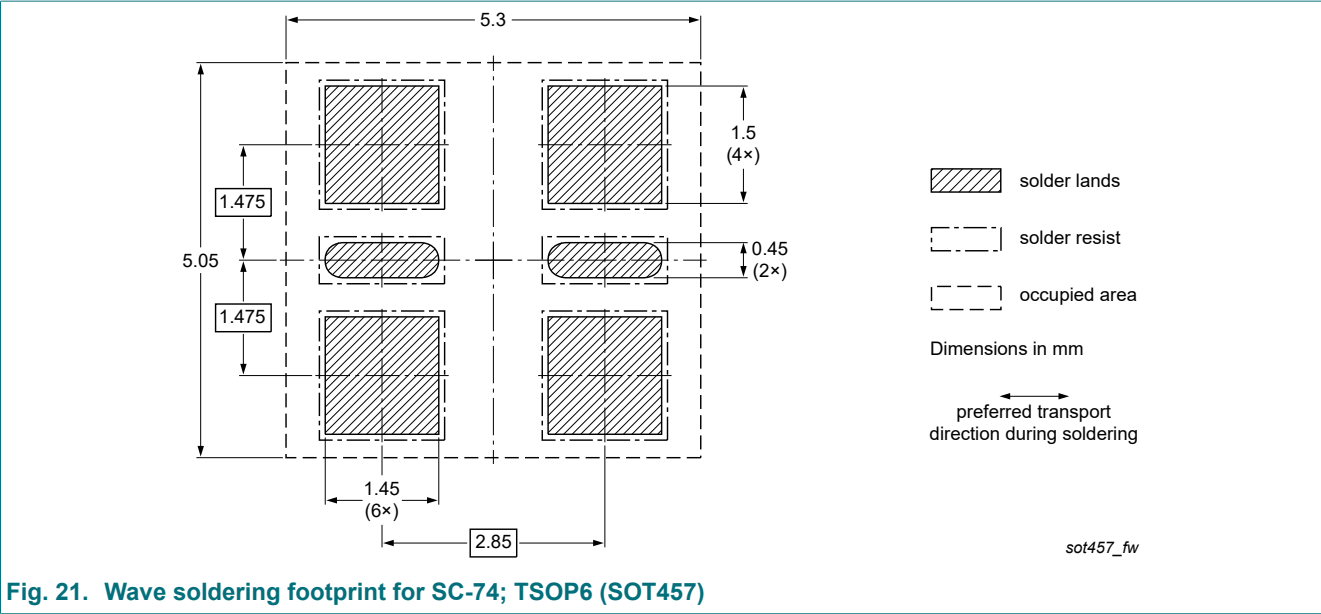


Fig. 21. Wave soldering footprint for SC-74; TSOP6 (SOT457)

50 V, 500 mA NPN/PNP Resistor-Equipped double Transistor (RET); R1 = 2.2 kΩ, R2 = 10 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMC32-Q v.1	20220216	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 16 February 2022

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