PHDMI2F4

ESD protection for ultra high-speed interfaces

Rev. 1 — 31 July 2014 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as Transition Minimized Differential Signaling (TDMS) lines of High-Definition Multimedia Interface (HDMI), standard 2.0 and lower, against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.5 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System ESD protection for HDMI, standard 2.0 and lower.
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.5 pF for each channel
- Design-friendly ‘pass-through’ signal routing

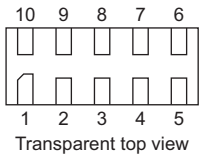
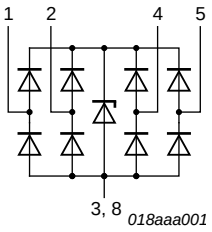
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection		
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PHDMI2F4	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 × 2.5 × 0.5 mm	SOT1176-1

4. Marking

Table 3. Marking codes

Type number	Marking code
PHDMI2F4	96

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		−0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 [1]			
		contact discharge	−10	+10	kV
		air discharge	−15	+15	kV
T_{amb}	ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

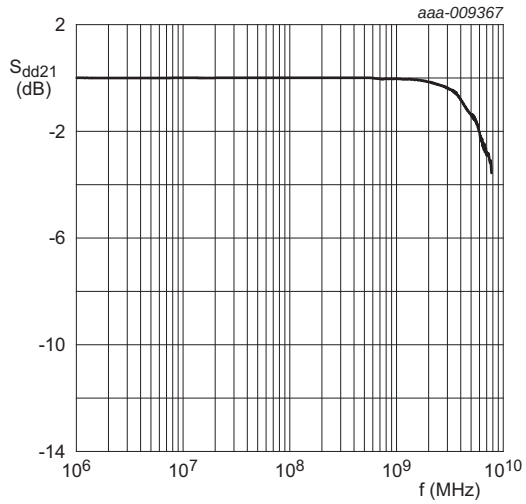
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_I = 1 mA	6	-	-	V
I_{LR}	reverse leakage current	per channel; V_I = 3 V	-	-	1	µA
V_F	forward voltage	I_I = 1 mA	-	0.7	-	V
C_{line}	line capacitance	f = 1 MHz; V_I = 3.3 V [1]	-	0.5	0.6	pF
ΔC_{line}	line capacitance difference	f = 1 MHz; V_I = 3.3 V [1]	-	0.05	-	pF
r_{dyn}	dynamic resistance	surge [2]				
		positive transient	-	0.41	-	Ω
		negative transient	-	0.26	-	Ω
		TLP [3]				
		positive transient	-	0.43	-	Ω
		negative transient	-	0.28	-	Ω
V_{CL}	clamping voltage	I_{PP} = 5.2 A [2]				
		positive transient	-	4.6	-	V
		I_{PP} = −4.4 A [2]				
		negative transient	-	−2.2	-	V

[1] This parameter is guaranteed by design.

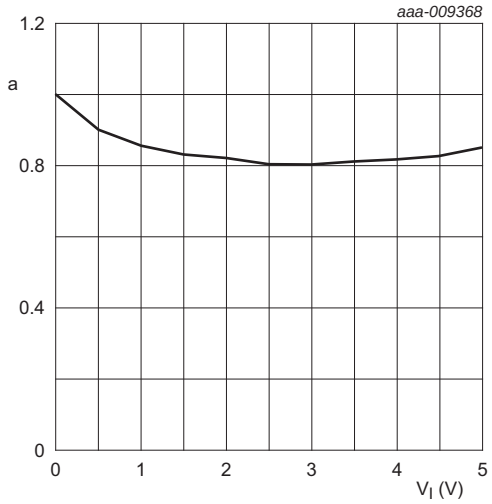
[2] According to IEC 61000-4-5 (8/20 µs current waveform).

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.



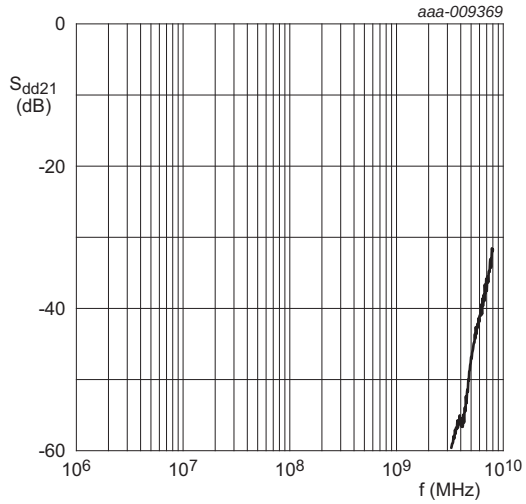
differential mode

Fig 1. Insertion loss; typical values



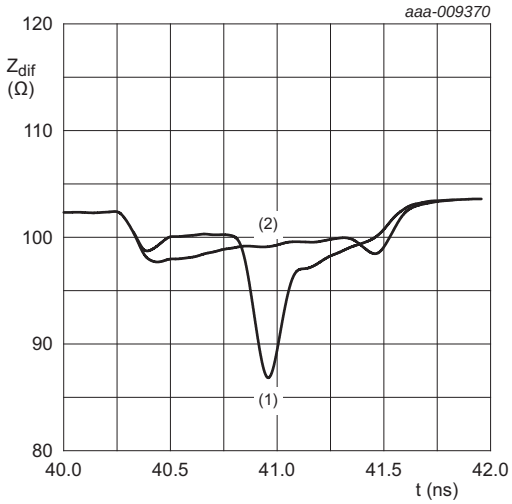
$$a = \frac{C_{line}}{C_{line(V_I = 0\ V)}}$$

Fig 2. Relative capacitance as a function of input voltage; typical values



Sdd21 normalized to 100 Ω;
differential pairs CH1/CH2 versus CH3/CH4

Fig 3. Crosstalk; typical values

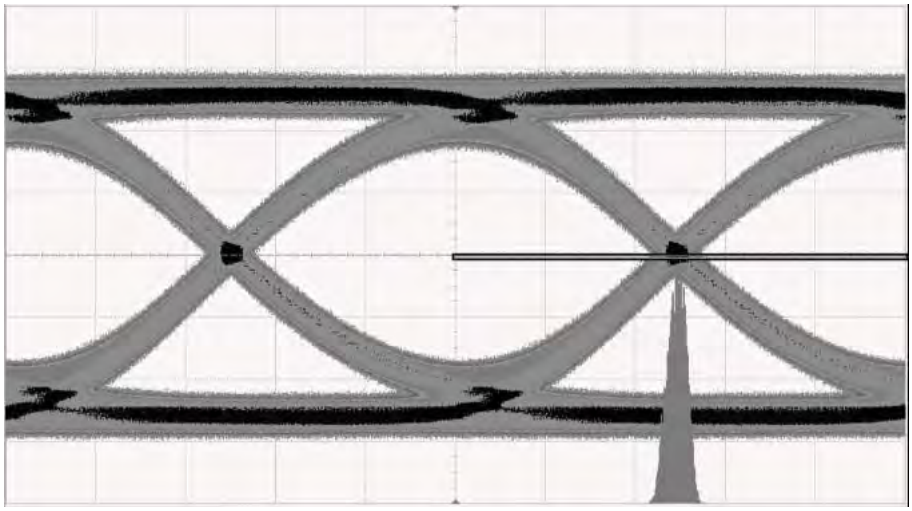


t_r = 200 ps; differential pair CH1 + CH2

(1) PHDMI2F4 on reference board

(2) Reference board without device under test (DUT)

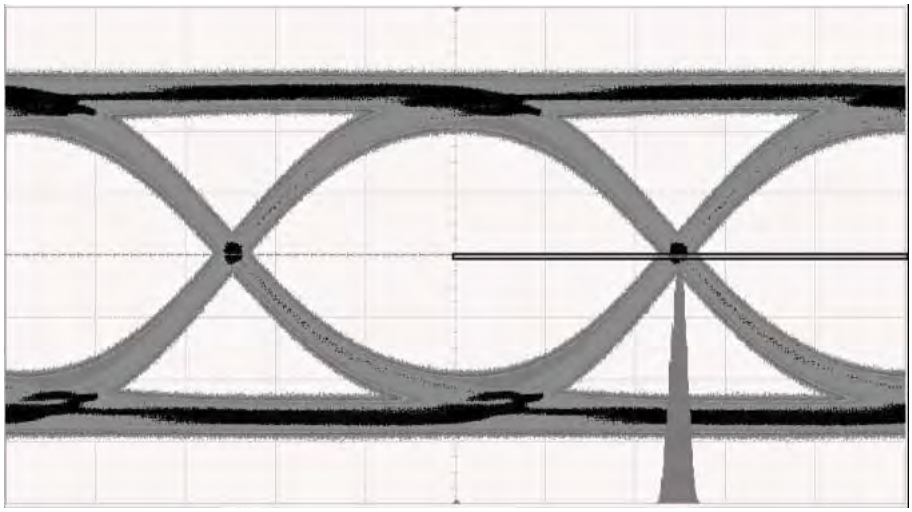
Fig 4. Differential Time Domain Reflectometer (TDR) plot; typical values



aaa-014159

Test frequency: 148.5 MHz
Differential swing voltage: 810 mV
Horizontal scale: 34 ps/div

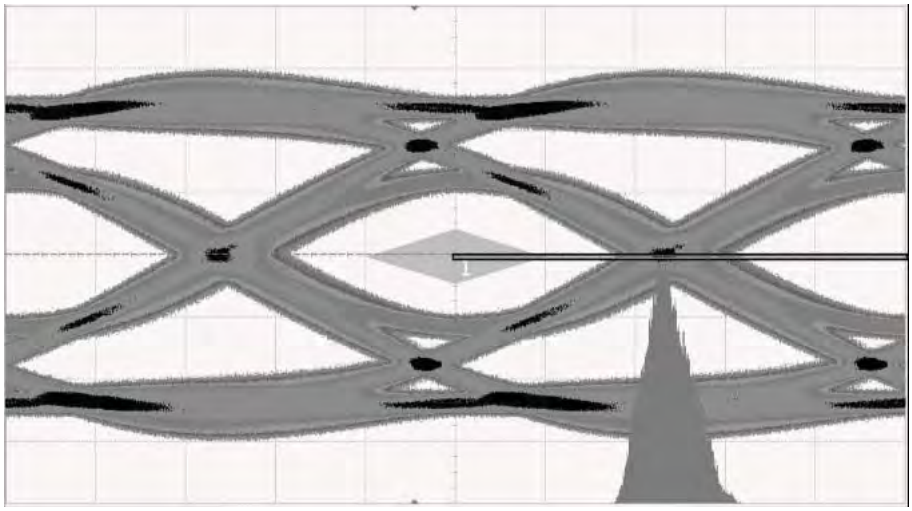
Fig 5. HDMI 2.0 TP1 eye diagram, PCB with PHDMI2F4 (2160p, 60 Hz)



aaa-014160

Test frequency: 148.5 MHz
Differential swing voltage: 800 mV
Horizontal scale: 34 ps/div

Fig 6. HDMI 2.0 TP1 eye diagram, PCB without PHDMI2F4 (2160p, 60 Hz, reference)



aaa-014161

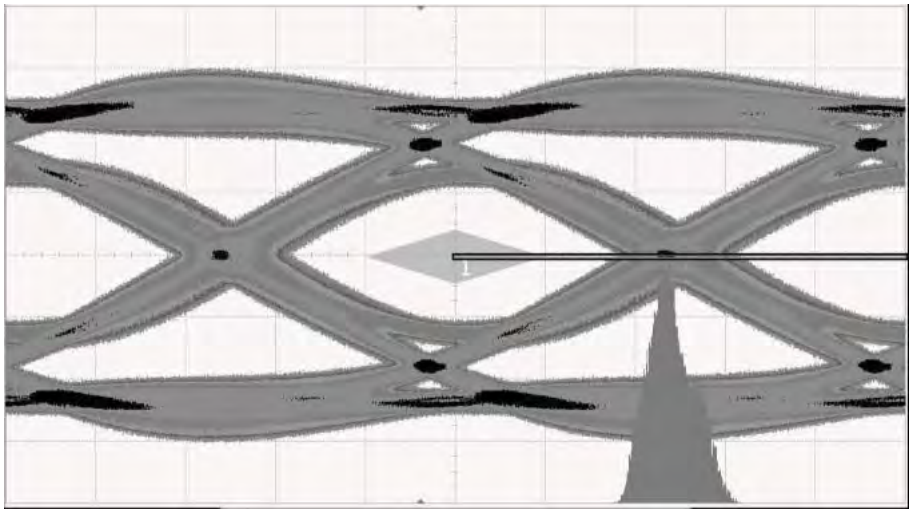
Test frequency: 148.5 MHz

Differential swing voltage: 809 mV

Horizontal scale: 34 ps/div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew.

Fig 7. HDMI 2.0 TP2 eye diagram, PCB with PHDMI2F4 (2160p, 60 Hz)



aaa-014162

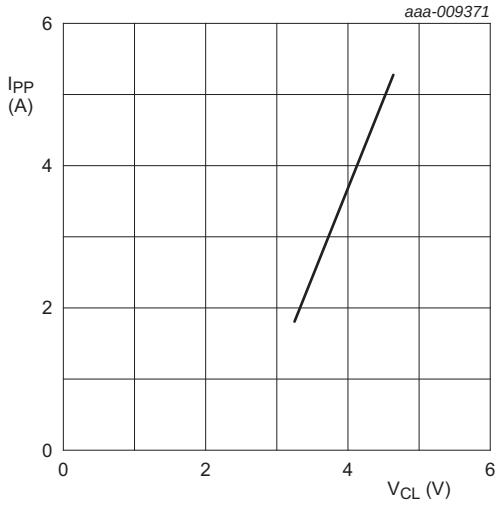
Test frequency: 148.5 MHz

Differential swing voltage: 820 mV

Horizontal scale: 34 ps/div

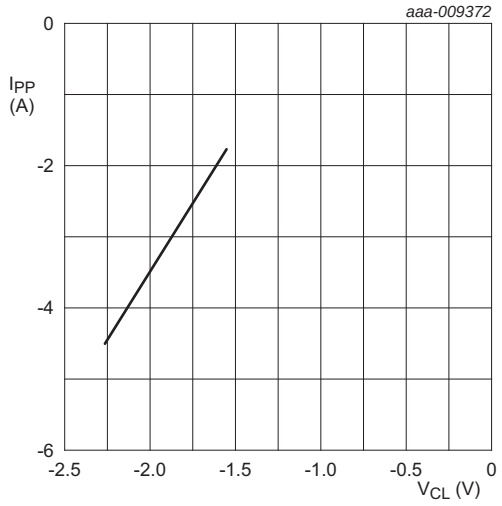
Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew.

Fig 8. HDMI 2.0 TP2 eye diagram, PCB without PHDMI2F4 (2160p, 60 Hz, reference)



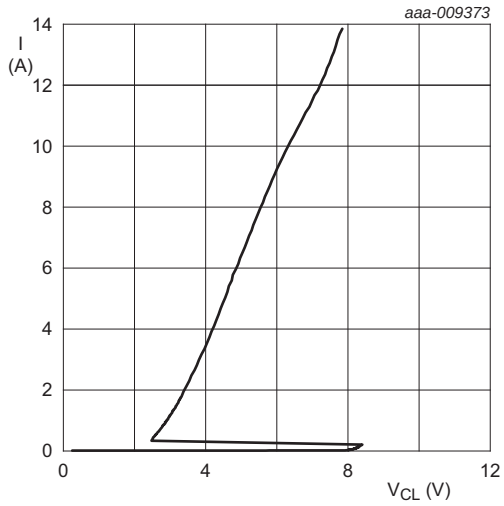
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 9. Dynamic resistance with positive clamping; typical values



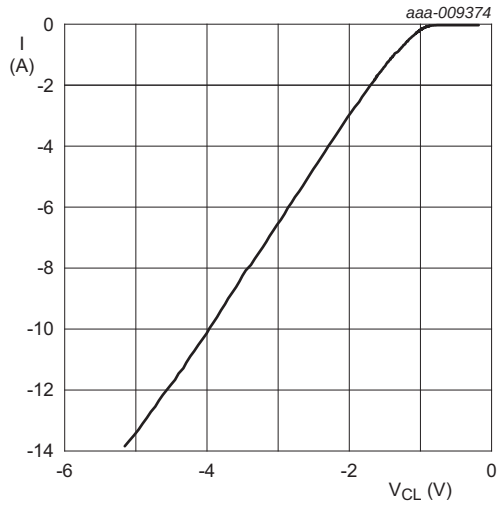
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 10. Dynamic resistance with negative clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 11. Dynamic resistance with positive clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 12. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI 2.0, DisplayPort and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

A basic application diagram for the ESD protection of an HDMI interface is shown in Figure 13.

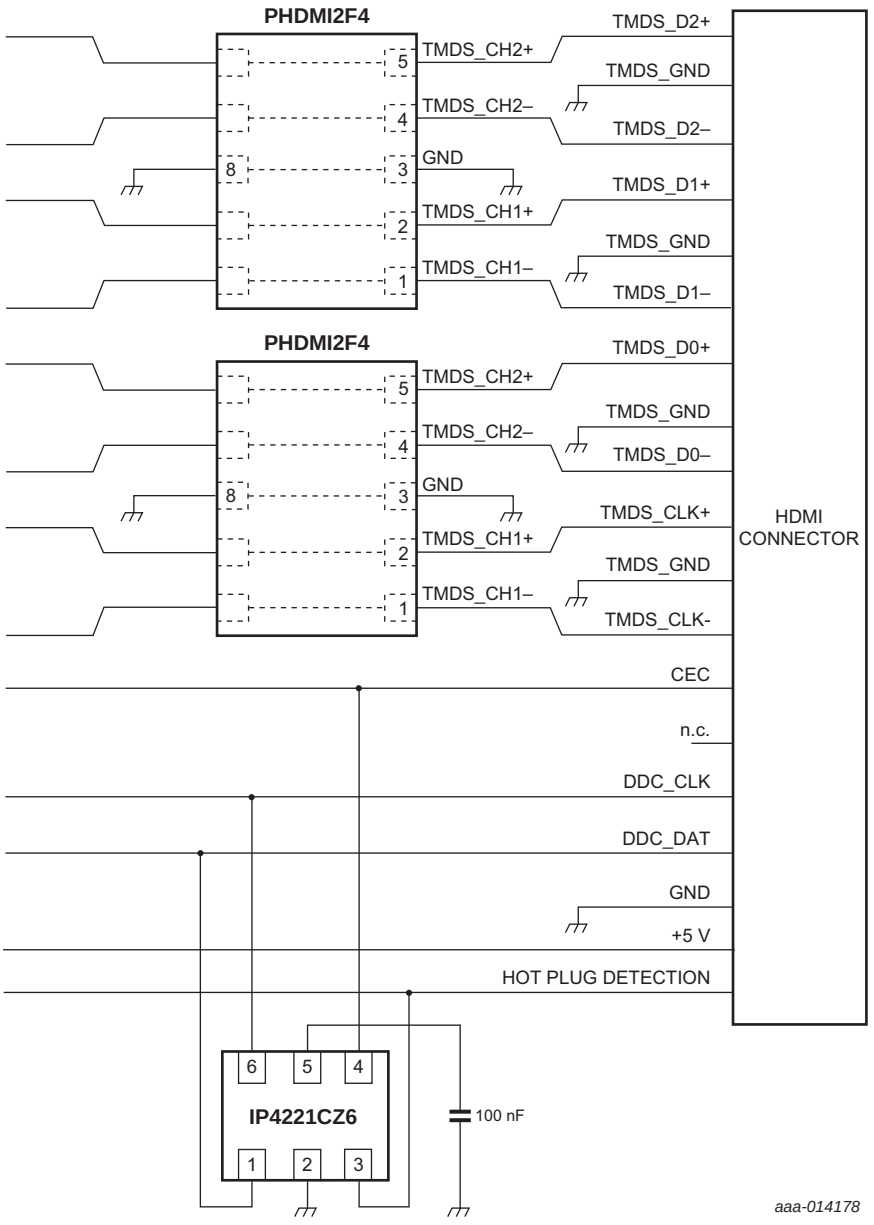


Fig 13. Application diagram of HDMI ESD protection using PHDMI2F4

8. Package outline

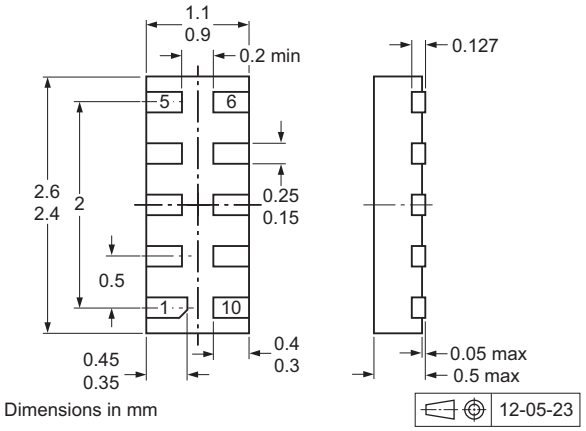
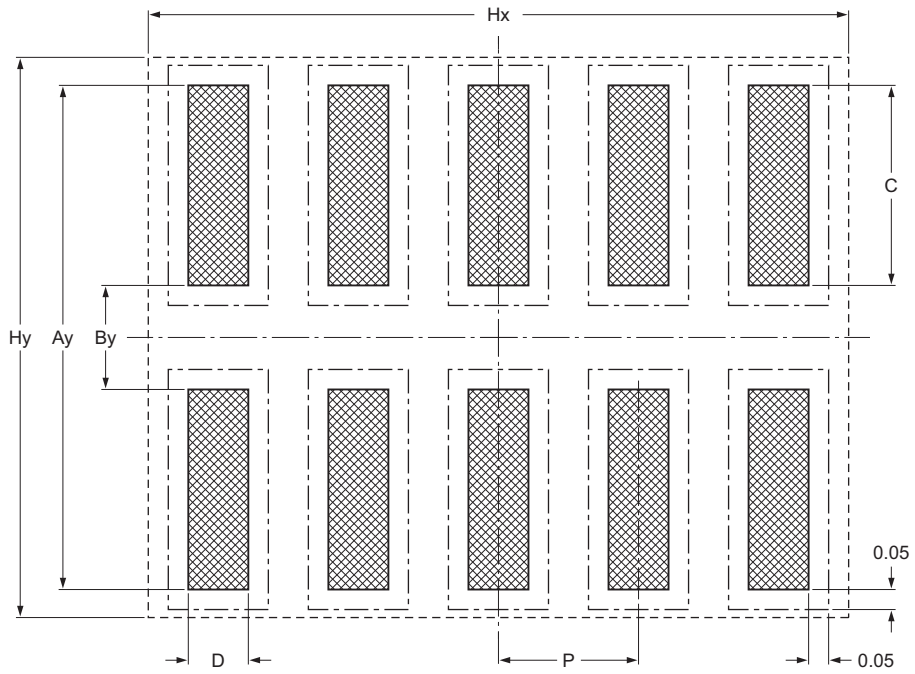


Fig 14. Package outline DFN2510A-10 (SOT1176-1)

9. Soldering

Footprint information for reflow soldering of DFN2510A-10 package **SOT1176-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

Dimensions in mm

P	Ay	By	C	D	Hx	Hy
0.5	1.25	0.3	0.475	0.2	2.45	1.5

Remark:
Stencil of 75 µm is recommended.
A stencil of 75 µm gives an aspect ratio of 0.77
With a stencil of 100 µm one will obtain an aspect ratio of 0.58

sot1176-1_fr

Fig 15. Reflow soldering footprint DFN2510A-10 (SOT1176-1)

10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHDMI2F4 v.1	20140731	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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