

Low capacitance unidirectional double ESD protection array

Rev. 1 — 21 February 2012

Product data sheet

1. Product profile

1.1 General description

Low capacitance unidirectional double ElectroStatic Discharge (ESD) protection array designed to protect up to two signal lines from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOT883B Surface-Mounted Device (SMD) plastic package.

1.2 Features and benefits

- ESD protection of up to two lines
- Low diode capacitance C_d = 16 pF
- Low clamping voltage V_{CL} = 10 V
- Ultra low leakage current I_{RM} = 5 nA
- ESD protection up to 15 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 2.5 A
- AEC-Q101 qualified

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Portable electronics
- SIM card protection
- Communication systems

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per diode	•					
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	$f = 1 MHz; V_R = 0 V$	-	16	19	pF



2. Pinning information

Table 2. Pinning

	9		
Pin	Description	Simplified outline	Graphic symbol
1	cathode		
2	cathode	1 3	3
3	common anode	2 Transparent top view	1 2 006aac923

3. Ordering information

Table 3. Ordering information

Type number	Package	Package					
	Name	Description	Version				
PESD5V0L2UMB	-	leadless ultra small plastic package; 3 solder lands; body 1.0 \times 0.6 \times 0.37 mm	SOT883B				

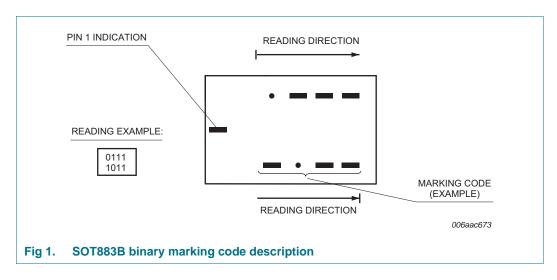
4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD5V0L2UMB	0001 1011

^[1] For SOT883B binary marking code description, see Figure 1.

4.1 Binary marking code description



PESD5V0L2UMB

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
I _{PPM}	rated peak pulse current	$t_p = 8/20 \ \mu s$	[1][2]	2.5	Α
Per device					
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	+150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] Device stressed with ten non-repetitive current pulses (8/20 μ s exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).

Table 6. ESD maximum ratings

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode	•				
LOD	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2]	15	kV
		machine model	[2] -	400	V
		MIL-STD-883 (human body model)	-	10	kV

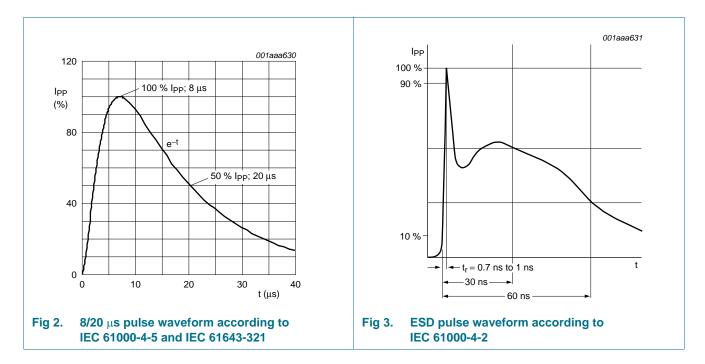
^[1] Device stressed with ten non-repetitive ESD pulses.

Table 7. ESD standards compliance

Conditions
> 15 kV (air); > 8 kV (contact)
> 8 kV

^[2] Measured from pin 1 or 2 to 3.

^[2] Measured from pin 1 or 2 to 3.



6. Characteristics

Table 8. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

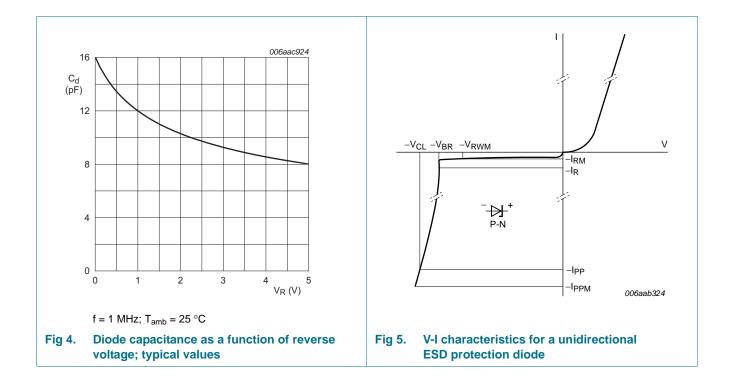
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per diod	е						
V_{RWM}	reverse standoff voltage			-	-	5	V
I _{RM}	reverse leakage current	$V_{RWM} = 5 V$		-	5	25	nA
V_{BR}	breakdown voltage	I _R = 1 mA		6.46	6.80	7.14	V
C _d	diode capacitance	$f = 1 MHz; V_R = 0 V$		-	16	19	pF
		f = 1 MHz; V _R = 5 V		-	8	11	pF
V_{CL}	clamping voltage	I _{PP} = 1 A	[1][2]	-	-	10	V
			[1][3]	-	-	11	V
		I _{PPM} = 2.5 A	[1][2]	-	-	13	V
			[1][3]	-	-	15	V
r _{dyn}	dynamic resistance	I _R = 10 A	<u>[4]</u>	-	0.9	-	Ω

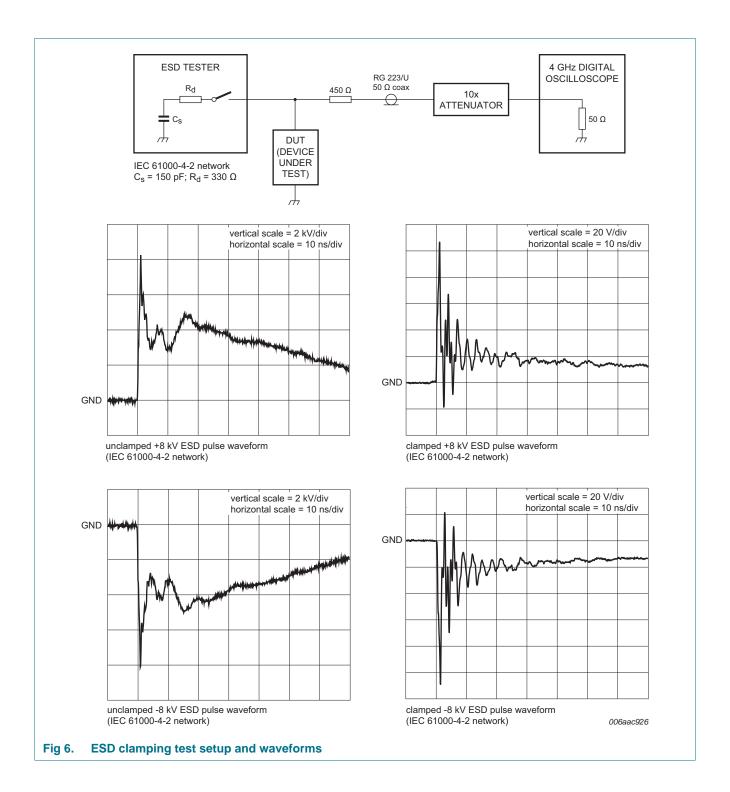
^[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.

^[2] Measured from pin 1 or 2 to 3.

^[3] Measured from pin 1 to 2.

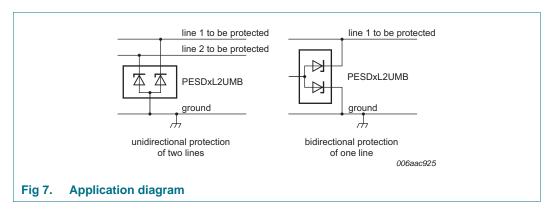
^[4] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANS/IESD STM5-1-2008.





7. Application information

The device is designed for the protection of up to two unidirectional data or signal lines from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are either positive or negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

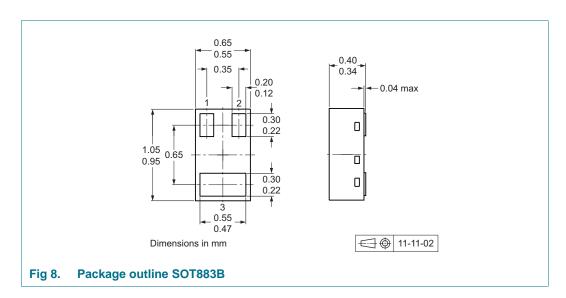
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101* - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

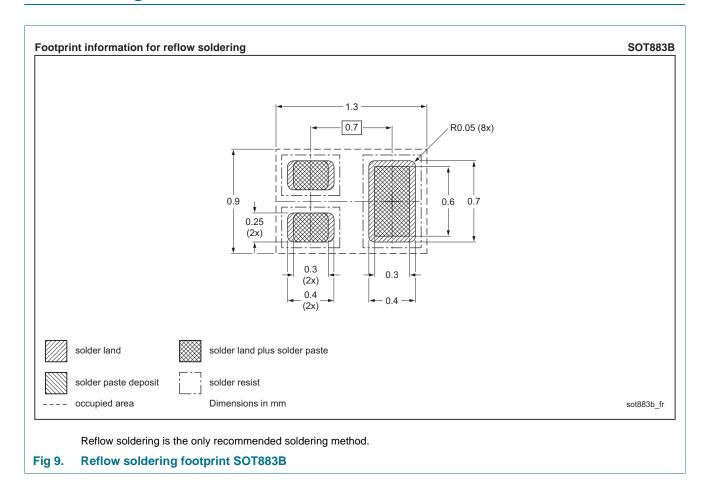
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity
			10000
PESD5V0L2UMB	SOT883B	2 mm pitch, 8 mm tape and reel	-315

^[1] For further information and the availability of packing methods, see Section 14.

11. Soldering



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12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0L2UMB v.1	20120221	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
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