



PESD3V3L1ULS

Unidirectional ESD protection diode

27 April 2021

Product data sheet

1. General description

Unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a leadless ultra small DFN1006BD-2 (SOD882BD) Surface-Mounted Device (SMD) plastic package with side-wettable flanks (SWF).

2. Features and benefits

- Ultra small SMD plastic package
- ESD protection of one line
- Side-wettable flanks
- Low clamping voltage: $V_{CL} = 20\text{ V}$
- Ultra low leakage current: $I_{RM} < 400\text{ nA}$
- ESD protection up to 30 kV
- IEC 61000-4-2 (ESD): level 4
- IEC 61000-4-5 (surge): I_{PPM} up to 14 A

3. Applications

- Computers and peripherals
- Audio and video equipment
- Parallel ports
- Communication systems



4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	3.3	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	-	105	160	pF

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode ^[1]	 <p>Transparent top view</p> <p>DFN1006BD-2 (SOD882BD)</p>	 <p>1 2</p> <p><i>sym035</i></p>
2	A	anode		

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3L1ULS	DFN1006BD-2	Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body	SOD882BD

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3L1ULS	8N

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-	14	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[2]	-	30	kV

- [1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5.
[2] Device stressed with ten non-repetitive ESD pulses.

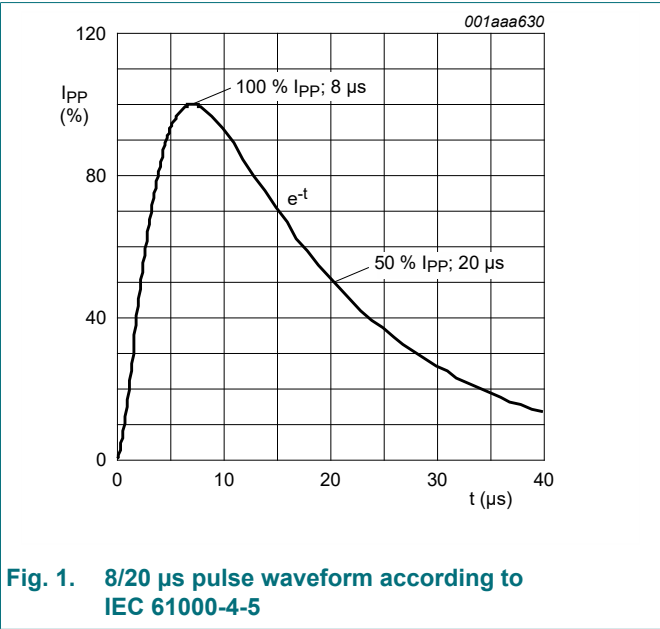


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

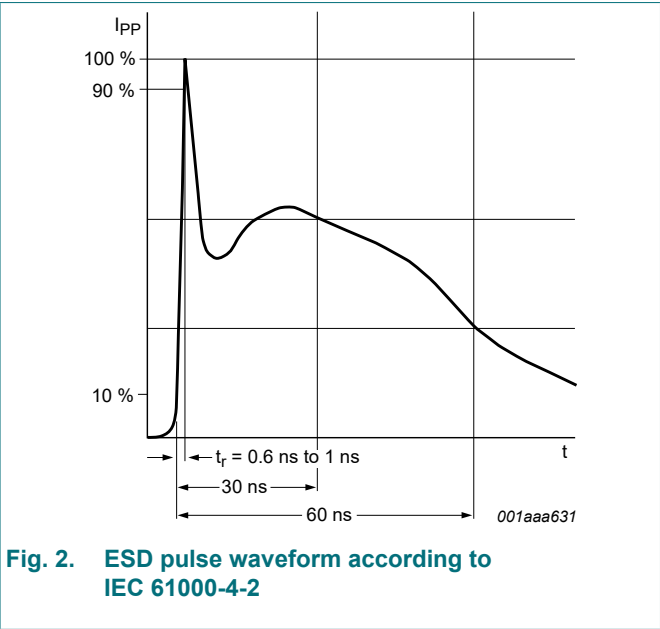


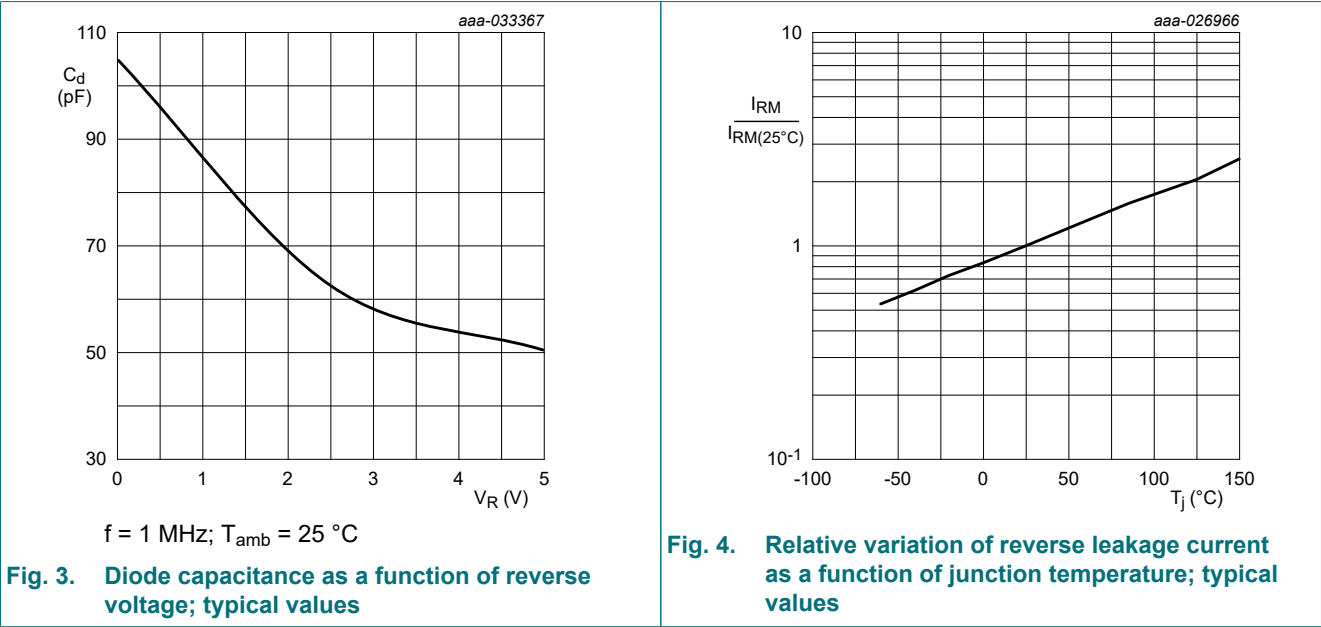
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

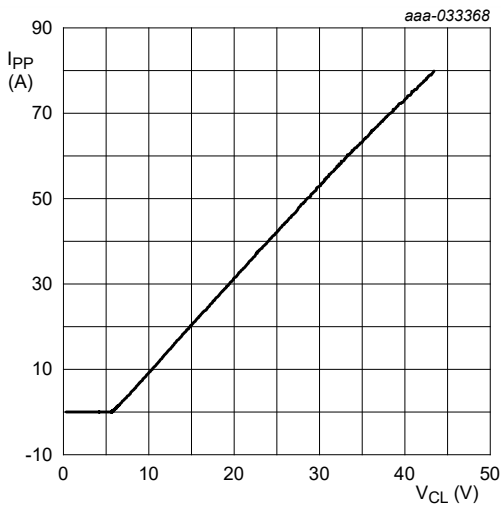
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	3.3	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C	[1]	5.2	5.6	6	V
I _{RM}	reverse leakage current	V _{RWM} = 3.3 V; T _{amb} = 25 °C		-	0.4	2	µA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	105	160	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _{amb} = 25 °C	[2]	-	-	7.5	V
		I _{PPM} = 14 A; T _{amb} = 25 °C	[2]	-	-	17.5	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[3]	-	0.46	-	Ω

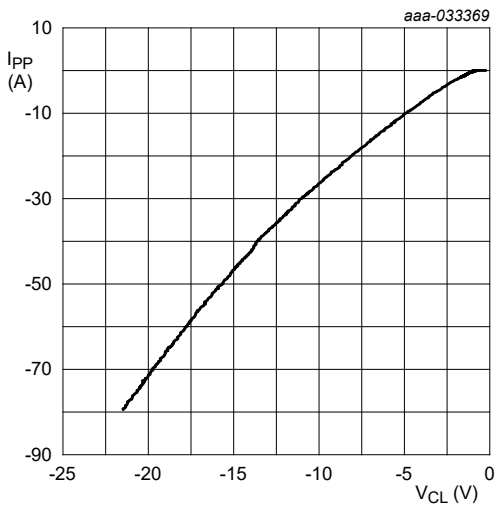
- [1] Pulse test: t_p ≤ 300 µs; duty cycle ≤ 0.02.
- [2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.





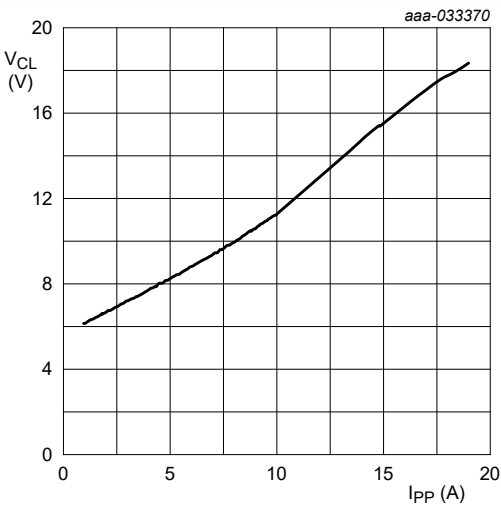
Transmission Line Pulse (TLP);
 $t_p = 100\text{ ns}$; $t_r = 1\text{ ns}$

Fig. 5. Dynamic resistance with positive clamping; typical values



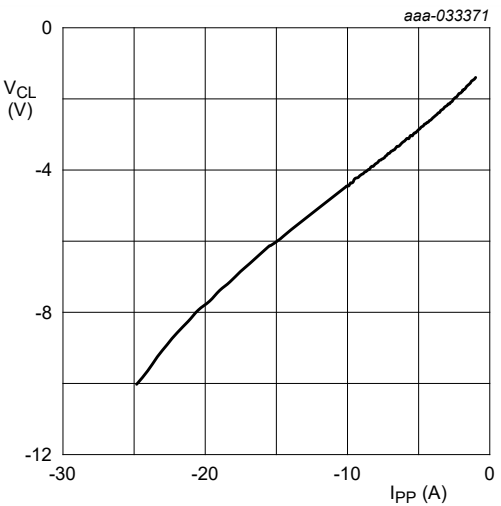
Transmission Line Pulse (TLP);
 $t_p = 100\text{ ns}$; $t_r = 1\text{ ns}$

Fig. 6. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5; $t_p = 8/20\text{ }\mu\text{s}$; positive pulse

Fig. 7. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20\text{ }\mu\text{s}$; negative pulse

Fig. 8. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one unidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.

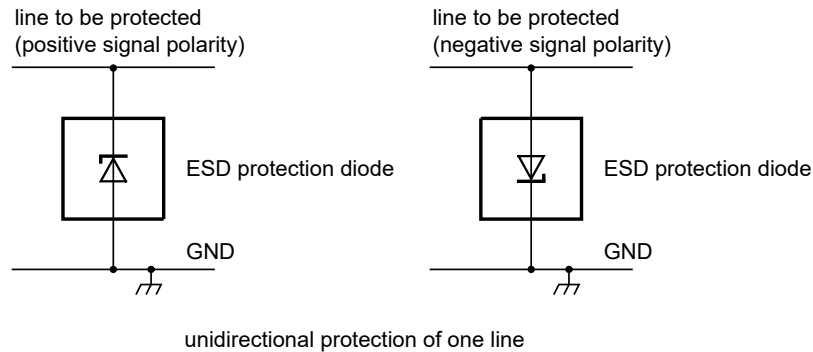


Fig. 9. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

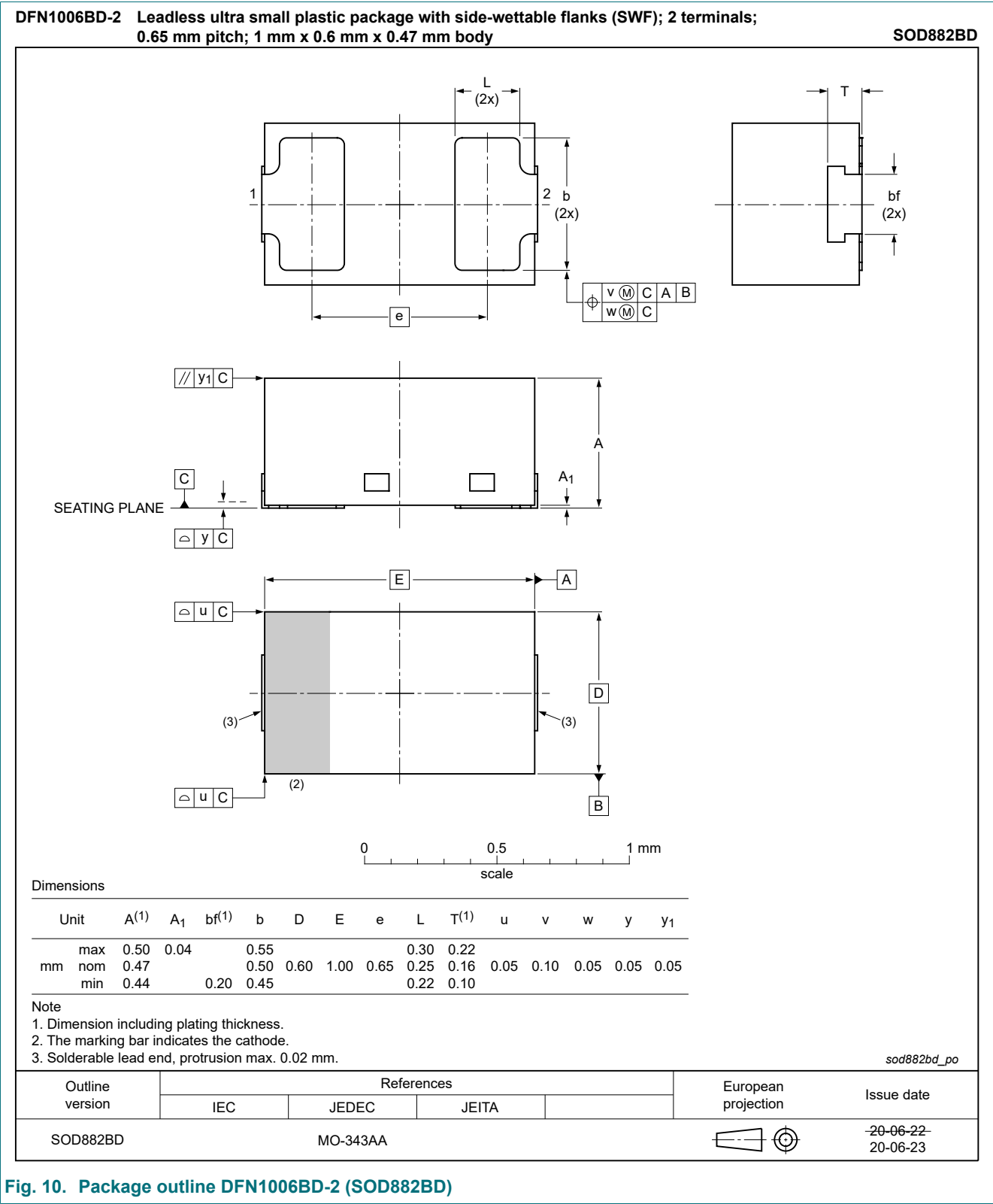
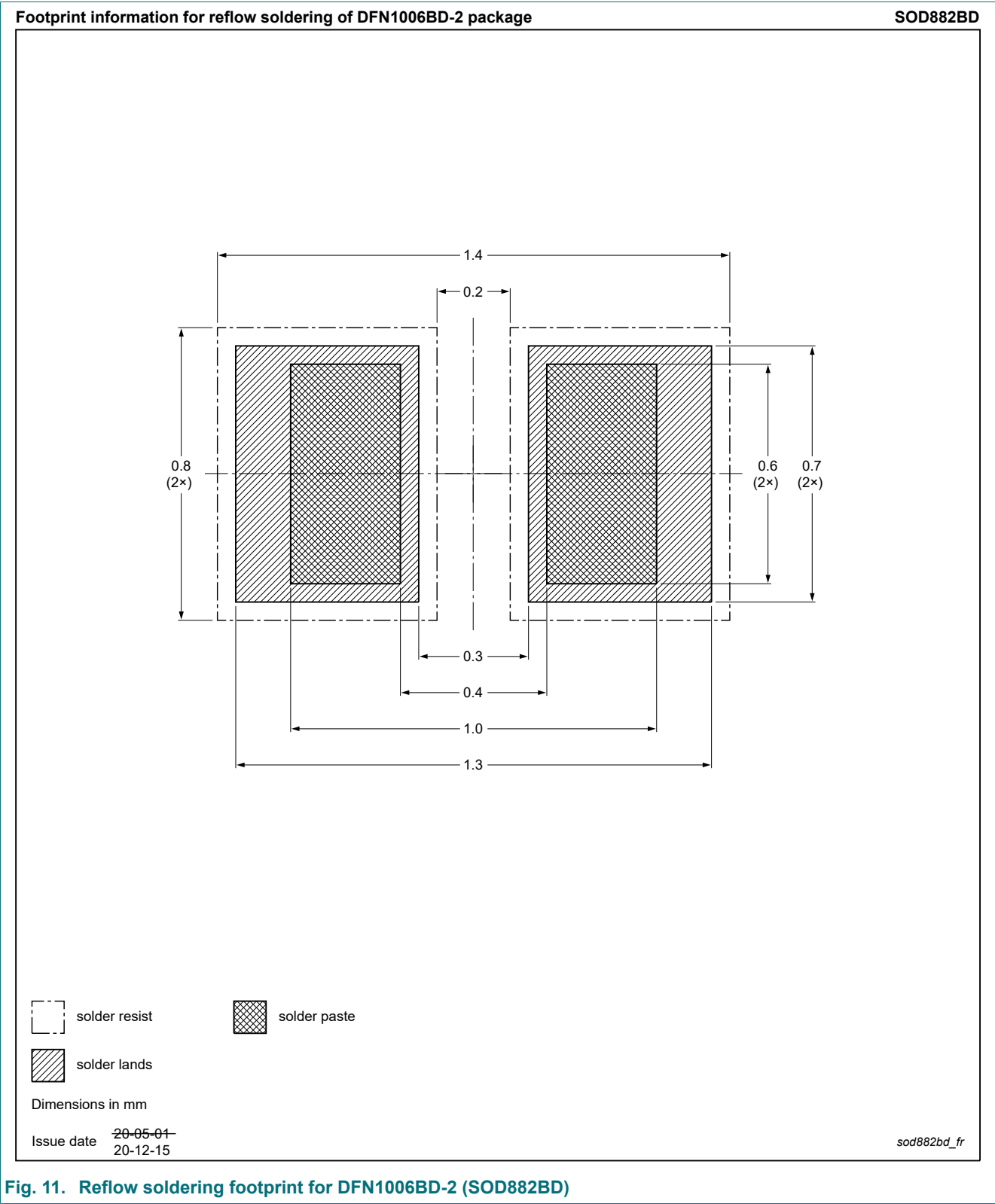


Fig. 10. Package outline DFN1006BD-2 (SOD882BD)

12. Soldering



13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3L1ULS v.1	20210427	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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