1. General description

Extremely low clamping low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, which is part of the TrEOS protection family. The device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from damage caused by ESD and other transients.

2. Features and benefits

- · Bidirectional ESD protection of one line
- Extremely high surge robustness of 11 A for a 8/20 µs pulse
- Low diode capacitance C_d = 0.8 pF
- · Extremely low inductance protection path to ground
- ESD protection up to ±18 kV according to IEC 61000-4-2
- · Ultra small SMD package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- · Communication systems
- · Computers and peripherals

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage		-3.3	-	3.3	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	0.8	1	pF



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode		
2	K2	cathode	Transparent top view DSN0603-2 (SOD962-2)	K1 K2 sym045

6. Ordering information

Table 3. Ordering information

Type number Package				
	Name	Description	Version	
PESD3V3HS2-SF	DSN0603-2	silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body	SOD962-2	

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3HS2-SF	D9

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-3.3	3.3	V
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1]	-11	11	Α
T _{amb}	ambient temperature			-40	125	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum	ratings					
V _{ESD}	voltago	IEC 61000-4-2; contact discharge	[2]	-18	18	kV
		IEC 61000-4-2; air discharge	[2]	-18	18	kV

- [1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC61000-4-5.
- [2] Device stressed with ten non-repetitive ESD pulses.

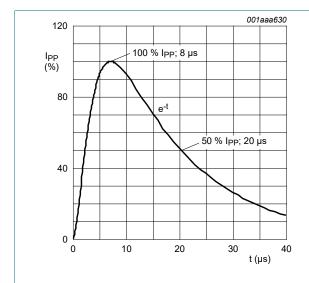


Fig. 1. $8/20~\mu s$ pulse waveform according to IEC 61000-4-5

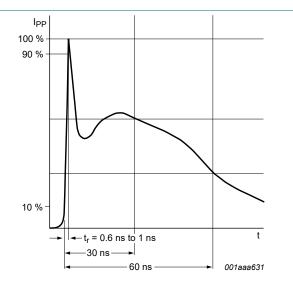


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C		-	6.6	-	V
I _{RM}	reverse leakage current	V _{RWM} = 3.3 V; T _{amb} = 25 °C		-	5	100	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.8	1	pF
V _{CL}	clamping voltage	I _{PPM} = 11 A; 8/20 μs; T _{amb} = 25 °C	[1]	-	-	4	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[2]	-	0.1	-	Ω
		I _R = -10 A; T _{amb} = 25 °C	[2]	-	0.1	-	Ω

- [1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; pulser at 70 ns to 90 ns; ANSI / ESD STM5.5.1-2008.

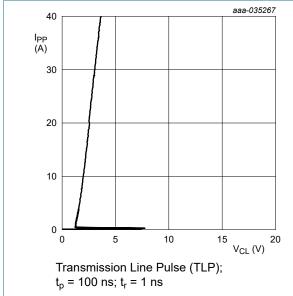


Fig. 3. Dynamic resistance with positive clamping; typical values

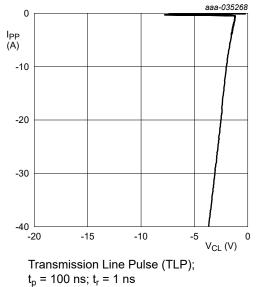
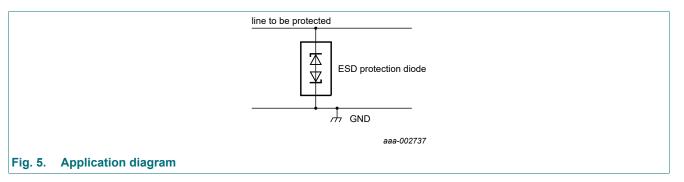


Fig. 4. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

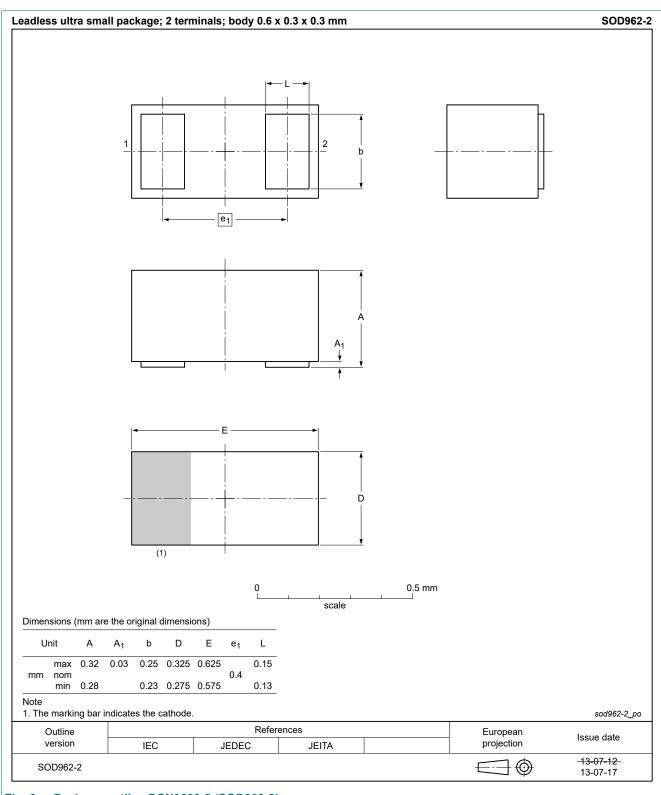


Fig. 6. Package outline DSN0603-2 (SOD962-2)

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12. Soldering

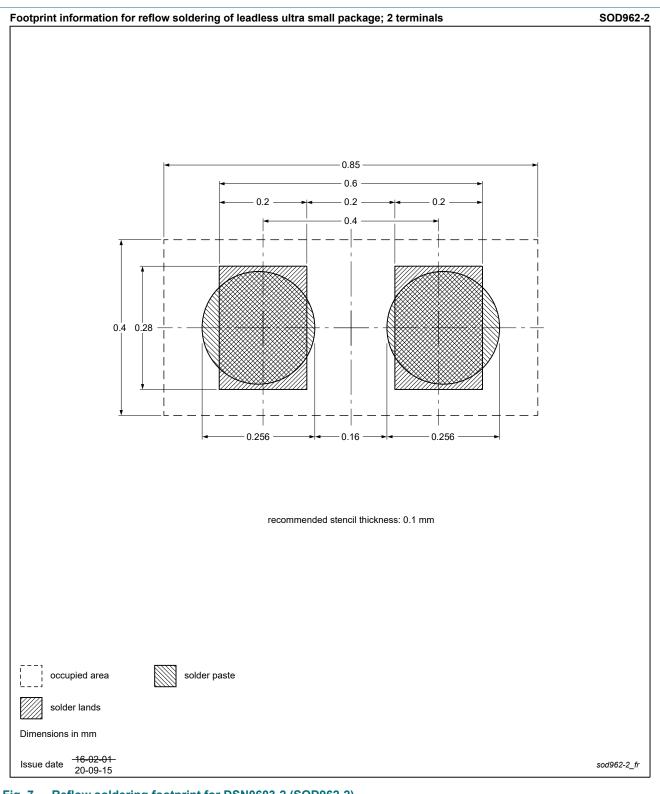


Fig. 7. Reflow soldering footprint for DSN0603-2 (SOD962-2)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3HS2-SF v.1	20220811	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Very low clamping bidirectional ESD protection diode

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