

PDTA143X/123J/143Z/114Y/124XQC

Series 50 V, 100 mA PNP resistor-equipped transistors Rev. 1 — 30 September 2021 Pro-

Product data sheet

1. General description

100 mA PNP Resistor-Equipped Transistor (RET) family in an ultra small DFN1412D-3 (SOT8009) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks.

Table 1. Product overview

Type number	R1	R2	Package		NPN complement:
	kΩ	kΩ	Nexperia	JEDEC	
PDTA143XQC	4.7	10	SOT8009	MO-340CA	PDTC143XQC
PDTA123JQC	2.2	47			PDTC123JQC
PDTA143ZQC	4.7	47			PDTC143ZQC
PDTA114YQC	10	47			PDTC114YQC
PDTA124XQC	22	47			PDTC124XQC

2. Features and benefits

- 100 mA output current capability
- **Built-in resistors**
- Simplifies circuit design •
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint

3. Applications

- **Digital applications**
- Cost saving alternative for BC857 series in digital applications
- Controlling IC inputs
- Switching loads •

4. Quick reference data

Table 2. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
lo	output current		-	-	-100	mA

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5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)		
2	GND	GND (emitter)	3	
3	0	output (collector)		
				GND
			Transparent top view	aaa-019606

6. Ordering information

Table 4. Ordering information

Type number	Package						
	Name	Description	Version				
PDTA143XQC	-	plastic leadless ultra small outline package with side-	SOT8009				
PDTA123JQC		wettable flanks (SWF); 3 terminals; 0.8 mm pitch; body: 1.4 x 1.2 x 0.48 mm					
PDTA143ZQC]						
PDTA114YQC							
PDTA124XQC	1						

7. Marking

Type number	Marking code
PDTA143XQC	8F
PDTA123JQC	8C
PDTA143ZQC	8G
PDTA114YQC	8B
PDTA124XQC	6F

8. Limiting values

Table 6. Limiting values

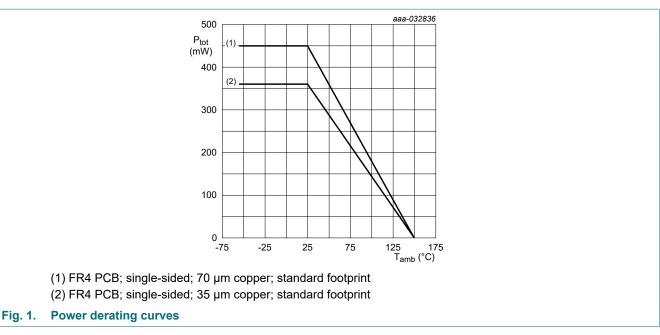
In accordance with the Absolute Maximum Rating System (IEC 60134).

$T_{amb} = 25$	5 °C unless	otherwise	specified.
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Symbol	Parameter	Conditions		Min	Max	Unit			
V _{CBO}	collector-base voltage	open emitter		-	-50	V			
V _{CEO}	collector-emitter voltage	open base		-	-50	V			
V _{EBO}	emitter-base voltage				_				
	PDTA143XQC	open collector		-	-7	V			
	PDTA123JQC			-	-5	V			
	PDTA143ZQC			-	-5	V			
	PDTA114YQC			-	-6	V			
	PDTA124XQC			-	-7	V			
VI	input voltage								
	PDTA143XQC			-30	+7	V			
	PDTA123JQC			-12	+5	V			
	PDTA143ZQC			-30	+5	V			
	PDTA114YQC			-40	+6	V			
	PDTA124XQC			-40	+7	V			
I _O	output current			-	-100	mA			
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	360	mW			
			[2]	-	450	mW			
Tj	junction temperature			-	150	°C			
T _{amb}	ambient temperature			-55	150	°C			
T _{stg}	storage temperature			-65	150	°C			

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided; 35 µm copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.



9. Thermal characteristics

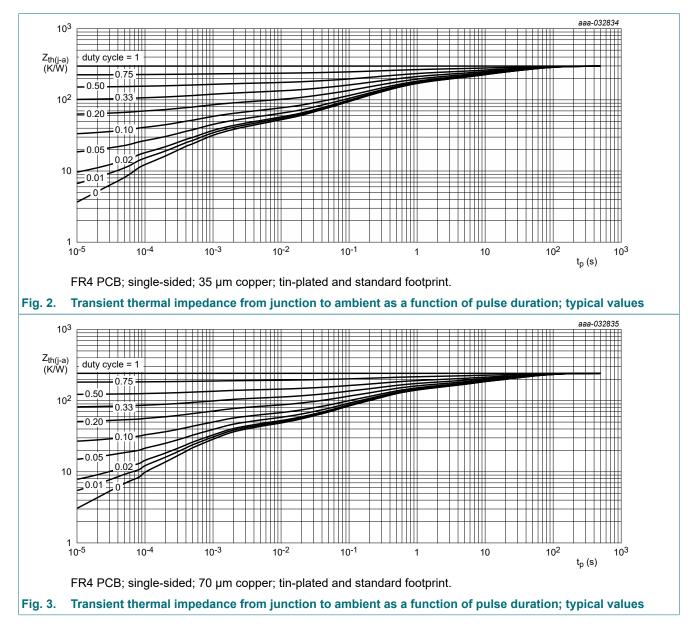
Table 7. Thermal characteristics

 T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	348	K/W
			[2]	-	-	278	K/W

[1] Device mounted on an FR4 PCB; single-sided; 35 µm copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.



10. Characteristics

Table 8. Characteristics

 T_{amb} = 25 °C unless otherwise specified.

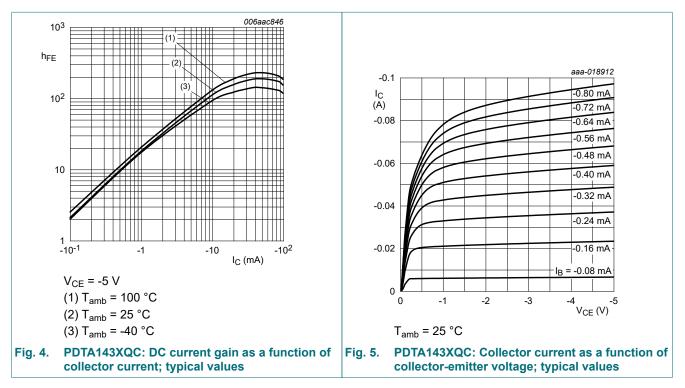
Symbol	Parameter	Conditions		Тур	Max	Unit			
V _{(BR)CBO}	collector-base breakdown voltage	I _C = -100 μA; I _E = 0 A	-50	-	-	V			
V _{(BR)CEO}	collector-emitter breakdown voltage	I _C = -2 mA; I _B = 0 A	-50	-	-	V			
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A	-	-	-100	nA			
CEO	collector-emitter cut-off	V _{CE} = -30 V; I _B = 0 A	-	-	-100	nA			
	current	V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	-	-	-5	μA			
I _{EBO}	emitter-base cut-off curr	ent				_			
	PDTA143XQC $V_{EB} = -5 \text{ V}; \text{ I}_{C} = 0 \text{ A}$		-	-	-600	μA			
	PDTA123JQC		-	-	-180	μA			
	PDTA143ZQC		-	-	-170	μA			
	PDTA114YQC				-150	μA			
	PDTA124XQC				-120	μA			
h _{FE}	DC current gain								
	PDTA143XQC	V _{CE} = -5 V; I _C = -10 mA	50	-	-				
	PDTA123JQC		100	-	-				
	PDTA143ZQC		100	-	-				
	PDTA114YQC	V _{CE} = -5 V; I _C = -5 mA	100	-	-				
	PDTA124XQC		80	-	-				
V _{CEsat}	collector-emitter saturation voltage								
	PDTA143XQC	I _C = -10 mA; I _B = -0.5 mA	-	-	-100	mV			
	PDTA123JQC	I _C = -5 mA; I _B = -0.25 mA	-	-	-100	mV			
	PDTA143ZQC	1	-	-	-100	mV			
	PDTA114YQC		-	-	-100	mV			
	PDTA124XQC	I _C = -10 mA; I _B = -0.5 mA	-	-	-100	mV			
V _{I(off)}	off-state input voltage	1							
	PDTA143XQC	V _{CE} = -5 V ; I _C = -100 μA	-	-0.9	-0.3	V			
	PDTA123JQC		-	-0.6	-0.5	V			
	PDTA143ZQC		-	-0.6	-0.5	V			
	PDTA114YQC	1	-	-0.7	-0.5	V			
	PDTA124XQC	1	-	-0.8	-0.5	V			
V _{I(on)}	on-state input voltage		I						
	PDTA143XQC	V _{CE} = -0.3 V ; I _C = -20 mA	-2.5	-1.5	-	V			
	PDTA123JQC	V _{CE} = -0.3 V ; I _C = -5 mA	-1.1	-0.75	-	V			
	PDTA143ZQC	V _{CE} = -0.3 V ; I _C = -5 mA	-1.3	-0.9	-	V			
	PDTA114YQC	V _{CE} = -0.3 V ; I _C = -1 mA	-1.4	-0.8	-	V			
	PDTA124XQC	V _{CE} = -0.3 V ; I _C = -2 mA	-2	-1.1	-	V			

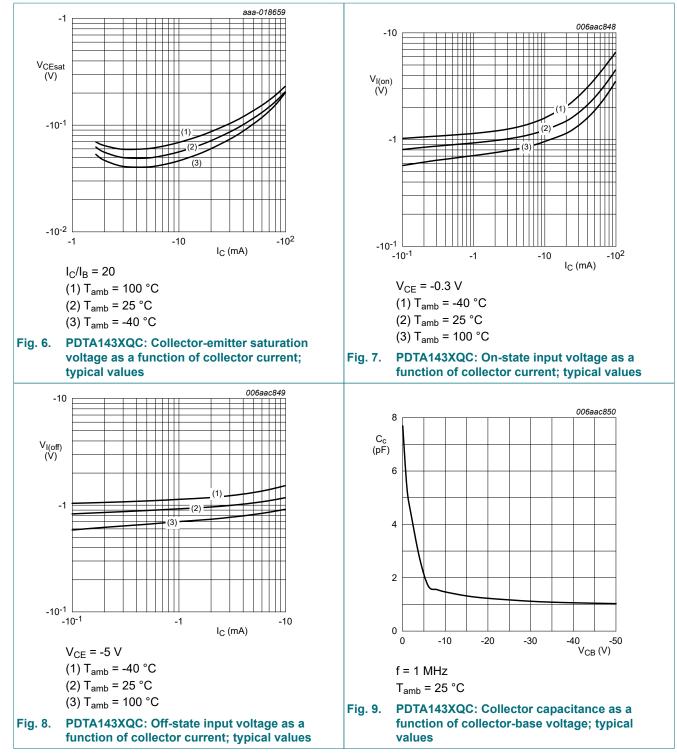
50 V, 100 mA PNP resistor-equipped transistors

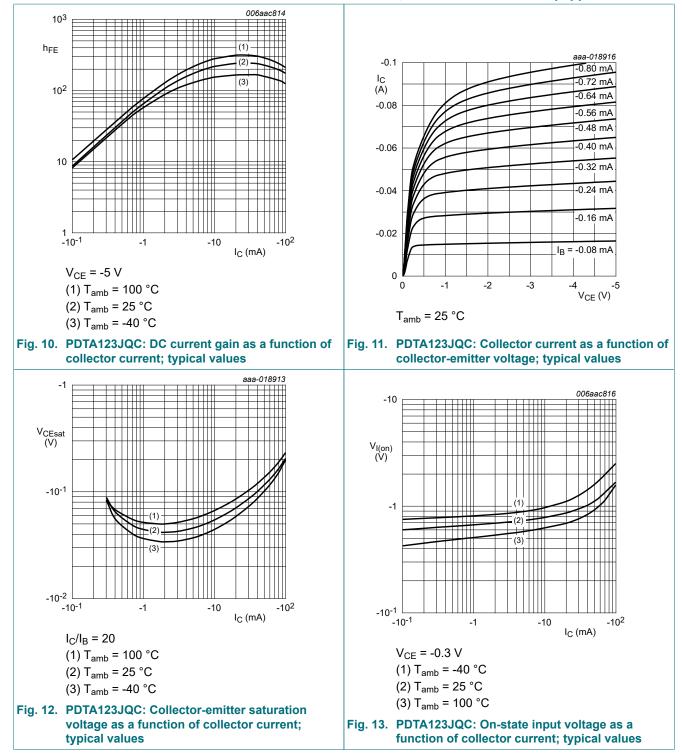
Symbol	Parameter	Conditions		Min	Тур	Max	Unit			
R1	bias resistor 1 (input)	bias resistor 1 (input)								
	PDTA143XQC		[1]	3.3	4.7	6.1	kΩ			
	PDTA123JQC			1.54	2.2	2.86	kΩ			
	PDTA143ZQC	_		3.3	4.7	6.1	kΩ			
	PDTA114YQC			7	10	13	kΩ			
	PDTA124XQC	_		15.4	22	28.6	kΩ			
R2/R1	bias resistor ratio									
	PDTA143XQC		[1]	1.7	2.13	2.6				
	PDTA123JQC			17	21	26				
	PDTA143ZQC			8	10	12				
	PDTA114YQC			3.7	4.7	5.7				
	PDTA124XQC			1.7	2.13	2.6				
f _T	transition frequency	V _{CE} = -5 V; I _C = -10 mA; f = 100 MHz	[2]	-	180	-	MHz			
C _c	collector capacitance	V _{CB} = -10 V; I _E = i _e = 0 A; f = 1 MHz		-	-	3	pF			

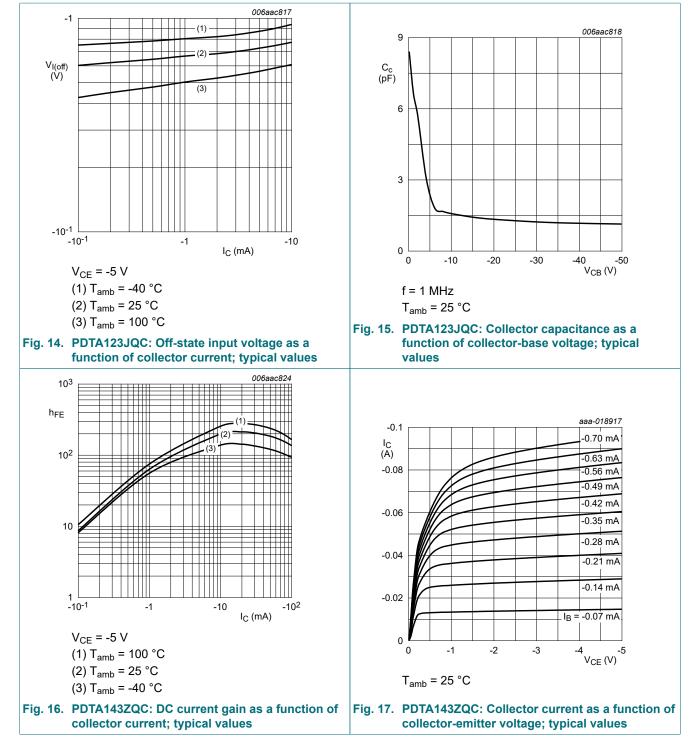
[1] See "Section 11: Test information" for resistor calculation and test conditions

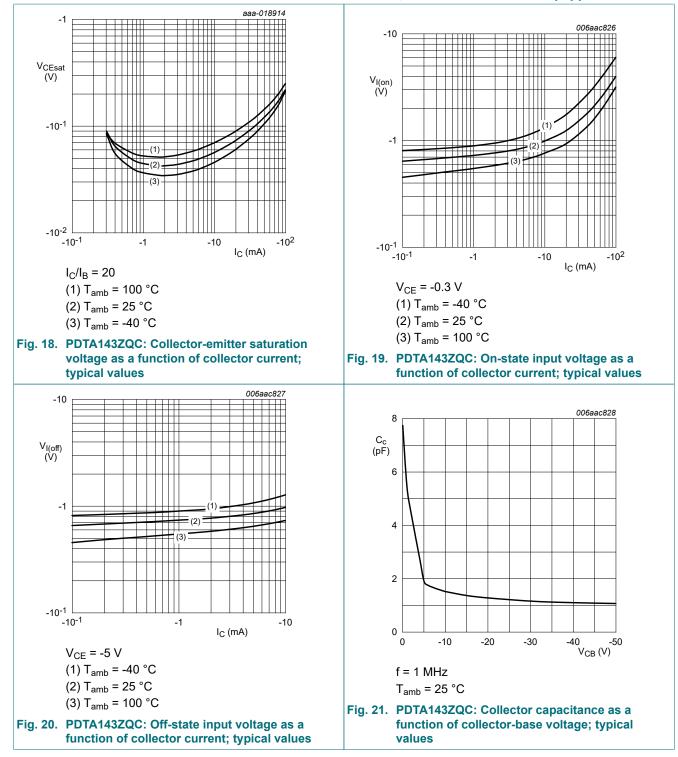
[2] Characteristics of built-in transistor

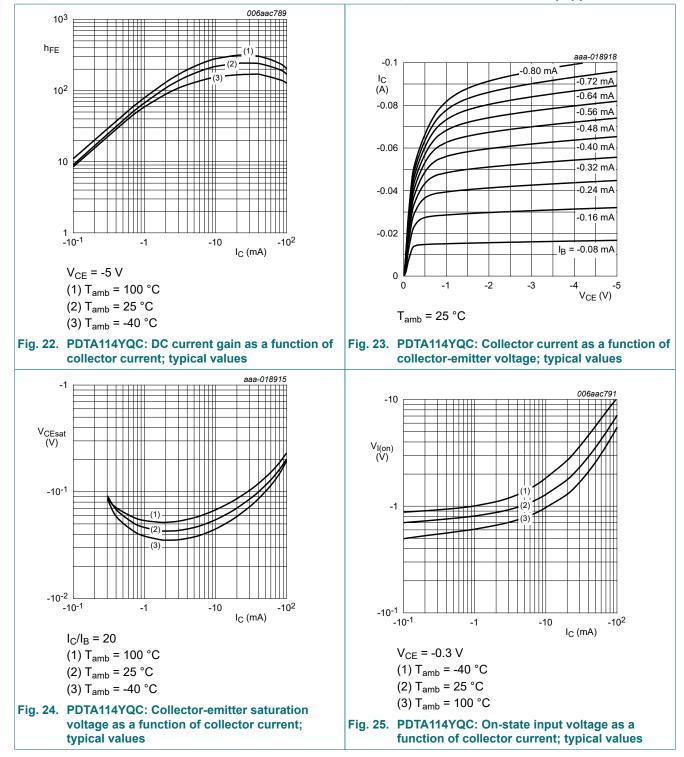


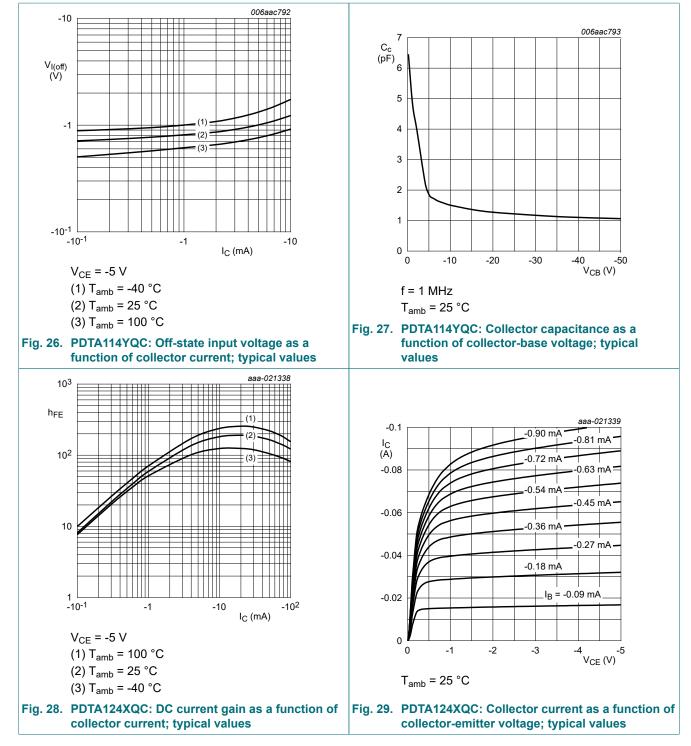


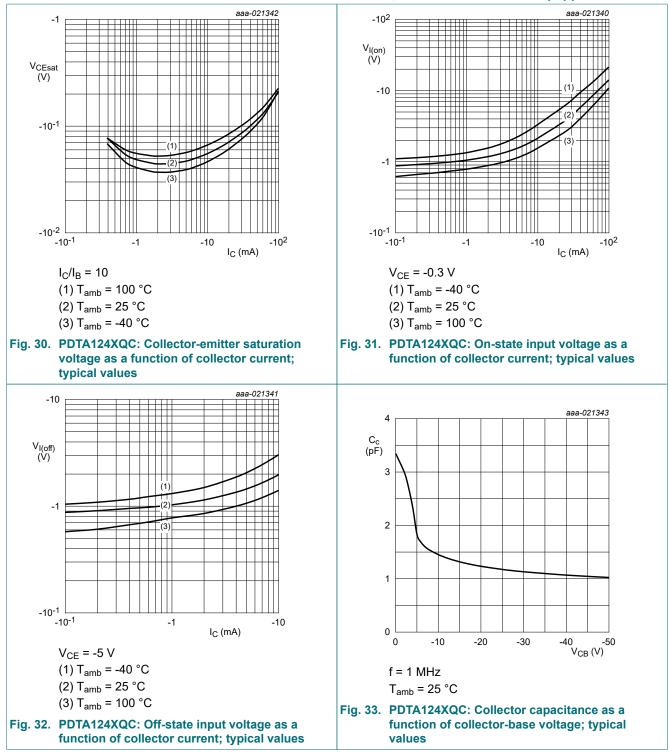






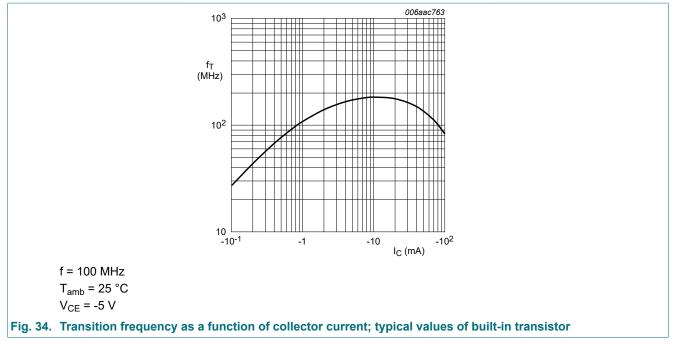






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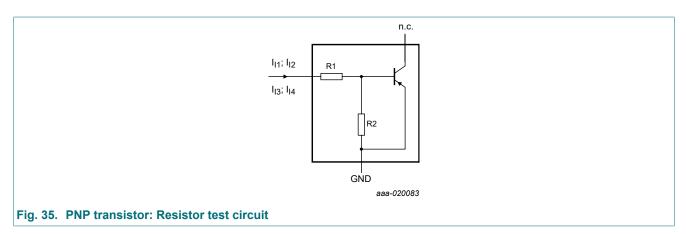


PDTA143X_TO_124XQC_SER

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1) $RI = \frac{V(I_{12}) - V(I_{11})}{I_{12} - I_{11}}$
- Calculation of bias resistor ratio (R2/R1) $\frac{R2}{R1} = \frac{V(I_{14}) - V(I_{13})}{R1 \cdot (I_{14} - I_{13})} - 1$

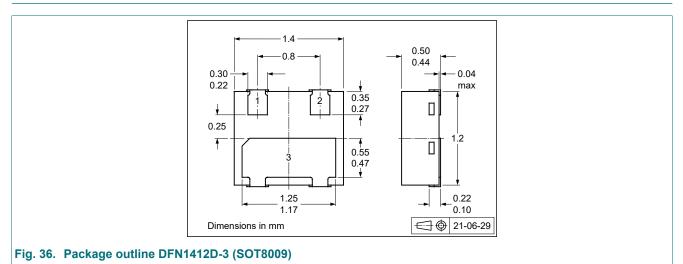


Resistor test conditions

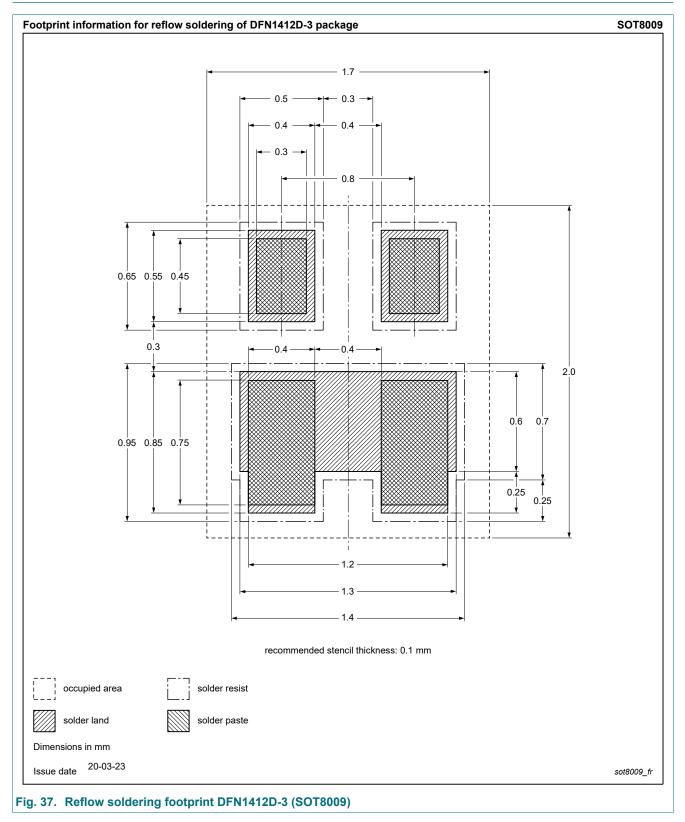
Table 9. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I _{I1}	I ₁₂	I ₁₃	I ₁₄
PDTA143XQC	4.7	10	-350 µA	-450 µA	350 µA	450 µA
PDTA123JQC	2.2	47	-90 µA	-140 µA	55 µA	105 µA
PDTA143ZQC	4.7	47	-90 µA	-140 µA	55 µA	105 µA
PDTA114YQC	10	47	-90 µA	-140 µA	55 µA	105 µA
PDTA124XQC	22	47	-55 μA	-105 µA	55 µA	105 µA

12. Package outline



13. Soldering



14. Revision history

Table 10. Revision history							
Data sheet ID	Release date		Change notice	Supersedes			
PDTA143X_TO_ 124XQC_SER v.1	20210930	Product data sheet	-	-			

PDTA143X_TO_124XQC_SER

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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