

# PCMFxUSB3B/C series

Common-mode EMI filter for differential channels with integrated bidirectional ESD protection

Rev. 2 — 29 January 2019

Product data sheet

## 1. General description

Common-mode ElectroMagnetic Interference (EMI) filters with integrated bidirectional ElectroStatic Discharge (ESD) protection for one, two and three differential channels. The devices are designed to provide low insertion loss for differential high-speed signals on each channel while unwanted common-mode signals are attenuated.

Each differential channel incorporates two signal lines that are coupled by integrated coils. Diodes provide protection to downstream components from ESD voltages up to  $\pm 20$  kV on each signal line.

**Table 1. Product overview**

Type number	Number of channels	Package Name
PCMF1USB3B/C	1	WLCSP5
PCMF2USB3B/C	2	WLCSP10
PCMF3USB3B/C	3	WLCSP15

## 2. Features and benefits

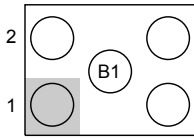
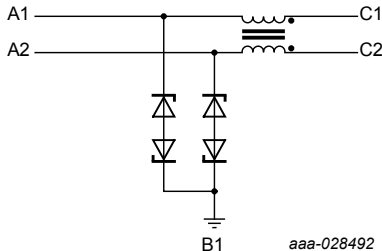
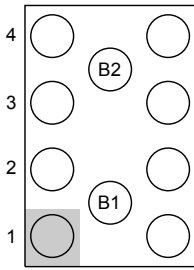
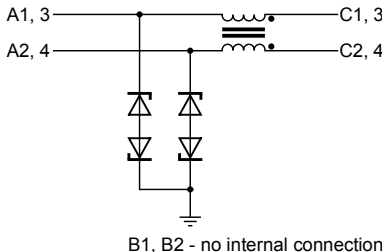
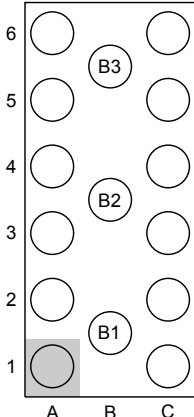
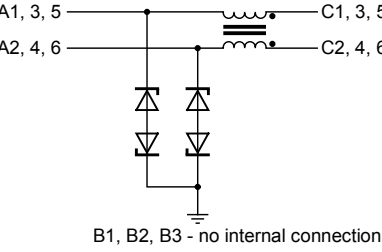
- One, two and three differential channels common-mode EMI filters with integrated ESD protection
- ESD protection up to  $\pm 20$  kV contact discharge according to IEC 61000-4-2
- Superior common-mode suppression over a wide frequency range
- Superior RF performance compared to other integrated filters or discrete filters with external ESD protection
- Extremely high symmetry between line pairs
- Industry-standard Wafer-Level Chip-Scale Packages: WLCSP5, 10 and 15 for smaller footprint

## 3. Applications

- Smartphone, cellular and cordless phone
- USB 3.2, USB 2.0, HDMI 2.0, HDMI 1.4
- General-purpose downstream ESD protection for differential data lines
- Tablet PC and Mobile Internet Device (MID)
- MIPI M-PHY and D-PHY as used in Camera Serial Interface (CSI) and Display Serial Interface (DSI)

## 4. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
PCMF1USB3B/C (WLCSP5_2-1-2)				
A1	CH1_IN+	channel 1+, external	 <p>Transparent top view <b>WLCSP5_2-1-2</b></p>	 <p>aaa-028492</p>
A2	CH1_IN-	channel 1-, external		
B1	GND_CH1	ground channel 1		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
PCMF2USB3B/C (WLCSP10_4-2-4)				
A1	CH1_IN+	channel 1+, external	 <p>Transparent top view <b>WLCSP10_4-2-4</b></p>	 <p>B1, B2 - no internal connection aaa-028493</p>
A2	CH1_IN-	channel 1-, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN-	channel 2-, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT-	channel 2-, internal		
PCMF3USB3B/C (WLCSP15_6-3-6)				
A1	CH1_IN+	channel 1+, external	 <p>Transparent top view <b>WLCSP15_6-3-6</b></p>	 <p>B1, B2, B3 - no internal connection aaa-028494</p>
A2	CH1_IN-	channel 1-, external		
A3	CH2_IN+	channel 2+, external		
A4	CH2_IN-	channel 2-, external		
A5	CH3_IN+	channel 3+, external		
A6	CH3_IN-	channel 3-, external		
B1	GND_CH1	ground channel 1		
B2	GND_CH2	ground channel 2		
B3	GND_CH3	ground channel 3		
C1	CH1_OUT+	channel 1+, internal		
C2	CH1_OUT-	channel 1-, internal		
C3	CH2_OUT+	channel 2+, internal		
C4	CH2_OUT-	channel 2-, internal		
C5	CH3_OUT+	channel 3+, internal		
C6	CH3_OUT-	channel 3-, internal		

## 5. Ordering information

**Table 3. Ordering information**

Type number	Package	
	Name	Description
PCMF1USB3B/C	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)
PCMF2USB3B/C	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)
PCMF3USB3B/C	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)

## 6. Marking

**Table 4. Marking codes**

Type number	Marking code
PCMF1USB3B/C	PF1B
PCMF2USB3B/C	PF2B
PCMF3USB3B/C	PF3B

## 7. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-4	4	V
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2, level 4; all input pins to ground			
		• contact discharge	-20	20	kV
		• air discharge	-20	20	kV
		IEC 61000-4-2, level 4; all output pins to ground			
		• contact discharge	-2	2	kV
		• air discharge	-2	2	kV
$I_{PPM}$	rated peak-pulse current	$t_p = 8/20 \mu s$	-9.5	9.5	A
$T_{stg}$	storage temperature		-40	+125	°C
$T_{amb}$	ambient temperature		-40	+125	°C

## 8. Characteristics

### 8.1. Channel characteristics

**Table 6. Channel characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	parameter	Conditions		Min	Typ	Max	Unit
$R_{S(ch)}$	channel series resistance	single line; input to output	-	-	2.6	-	$\Omega$
$C_d$	diode capacitance	$f = 1\text{ MHz}$ ; $V_I = 2.5\text{ V}$	[1]	-	0.3	-	pF
$I_{RM}$	reverse leakage current	per line; $V_I = 4\text{ V}$		-	1	100	nA
$V_{BR}$	breakdown voltage	$I_R = 1\text{ mA}$		6	9	-	V
$R_{dyn}$	dynamic resistance	TLP; positive transient	[2]	-	0.22	-	$\Omega$
		TLP; negative transient	[2]	-	0.22	-	$\Omega$

[1] This parameter is guaranteed by design

[2] 100 ns Transmission Line Pulse (TLP); 50  $\Omega$ ; pulser at 70 ns to 90 ns.

### 8.2. Frequency characteristics

**Table 7. Frequency characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Differential mode: <math>S_{dd21}</math></b>							
$f_{-3dB}$	cut-off frequency		[1]	-	8.1	-	GHz

[1] Normalized to attenuation at 1 MHz.

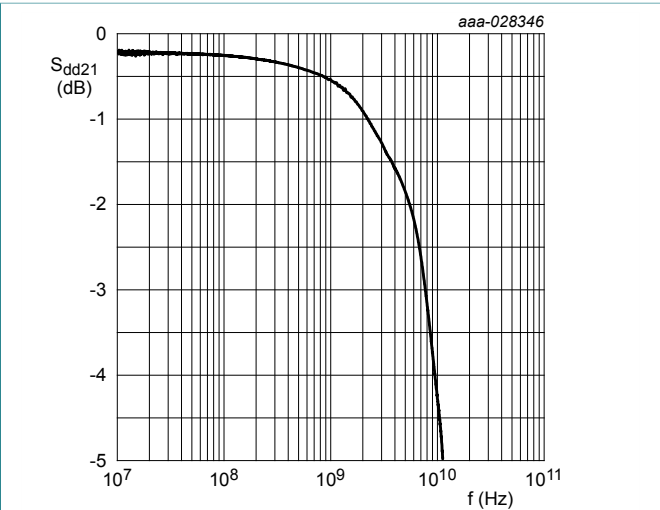


Fig. 1. Differential mode insertion loss; typical values

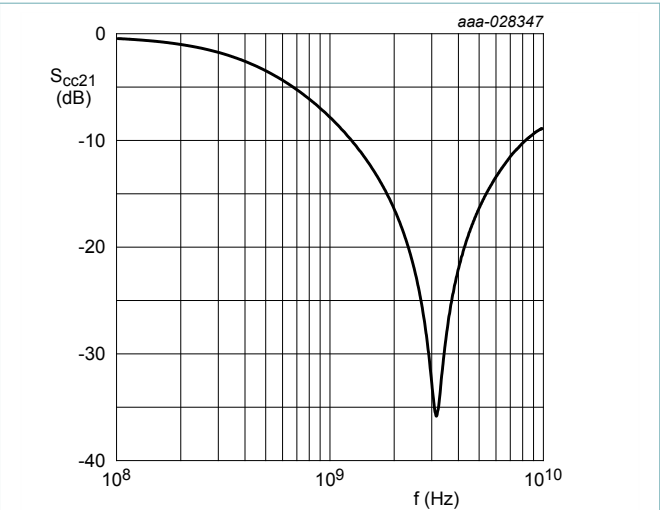
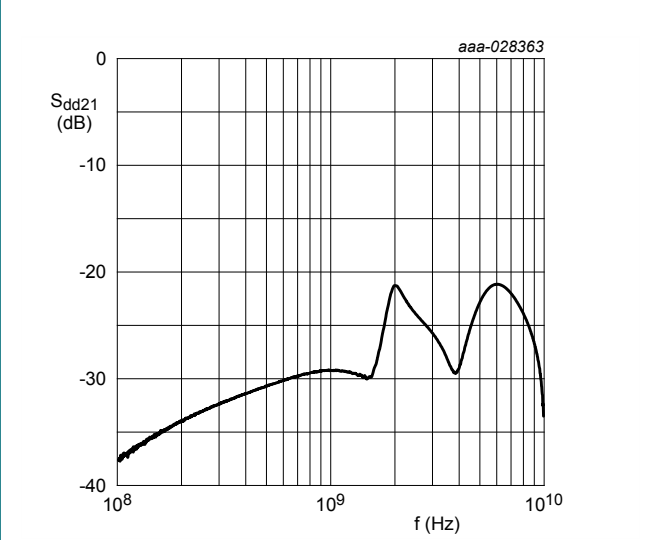
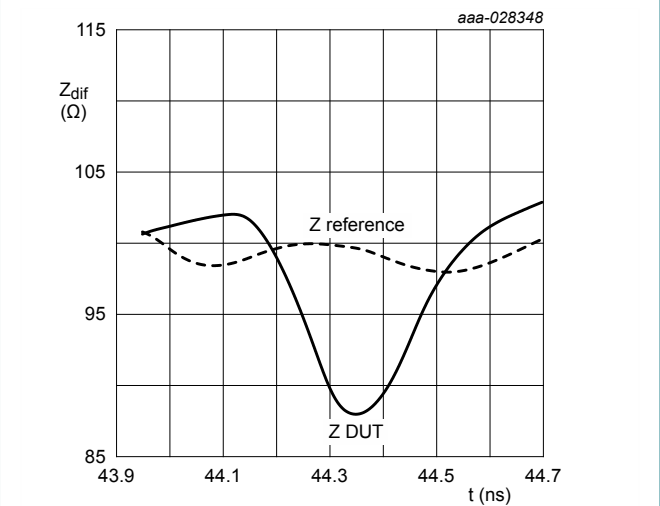


Fig. 2. Common-mode insertion loss; typical values



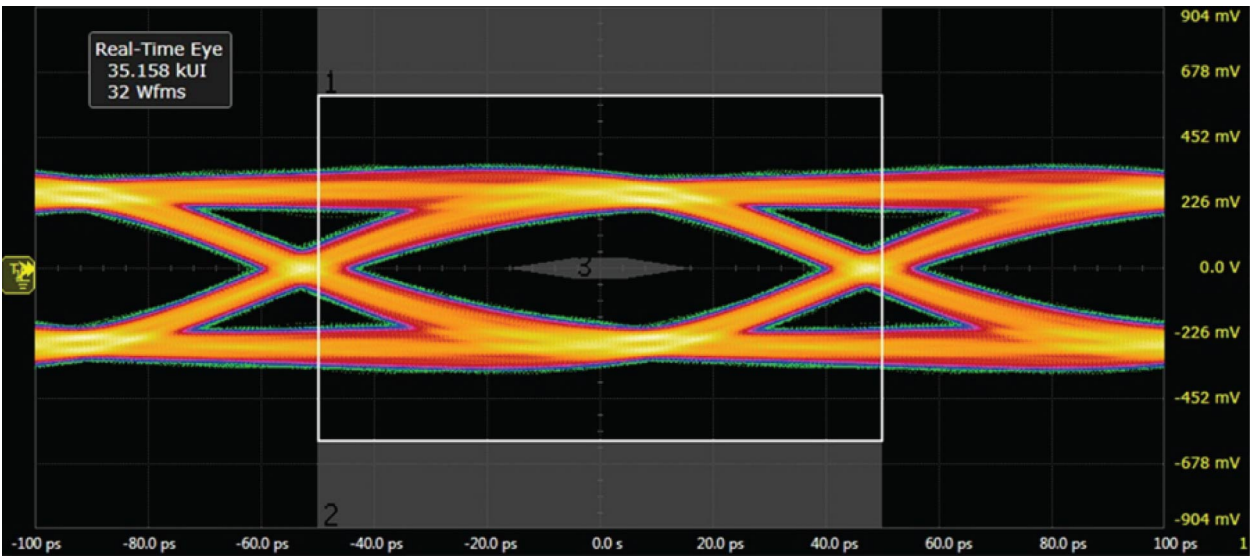
CH1 to CH2

Fig. 3. Differential crosstalk; typical values



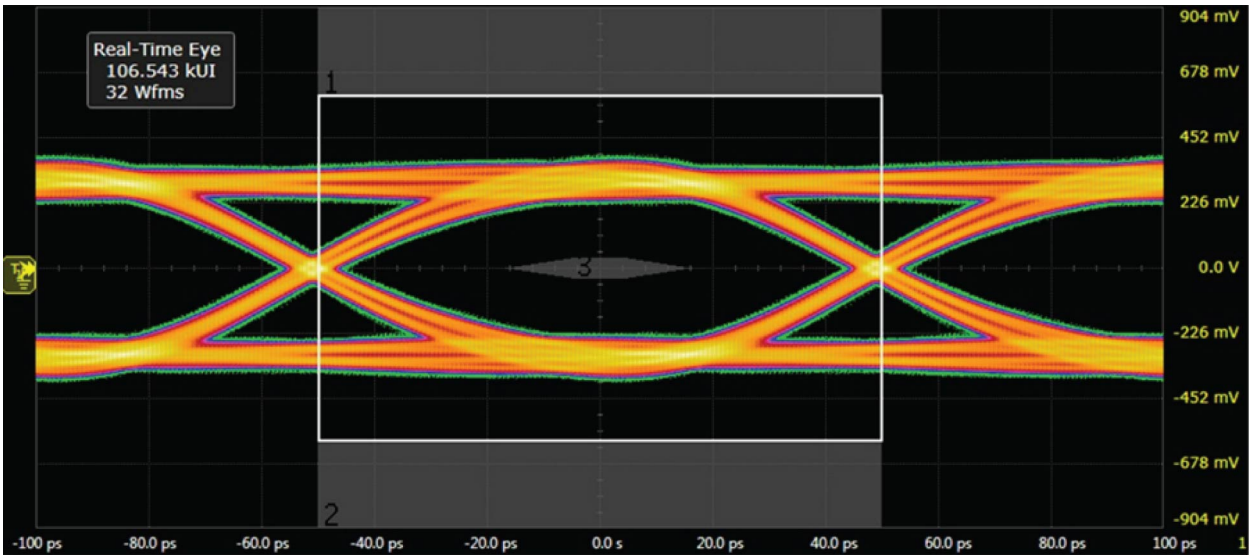
$t_r = 200$  ps

Fig. 4. Differential Time Domain Reflectometer (TDR) plot; typical values



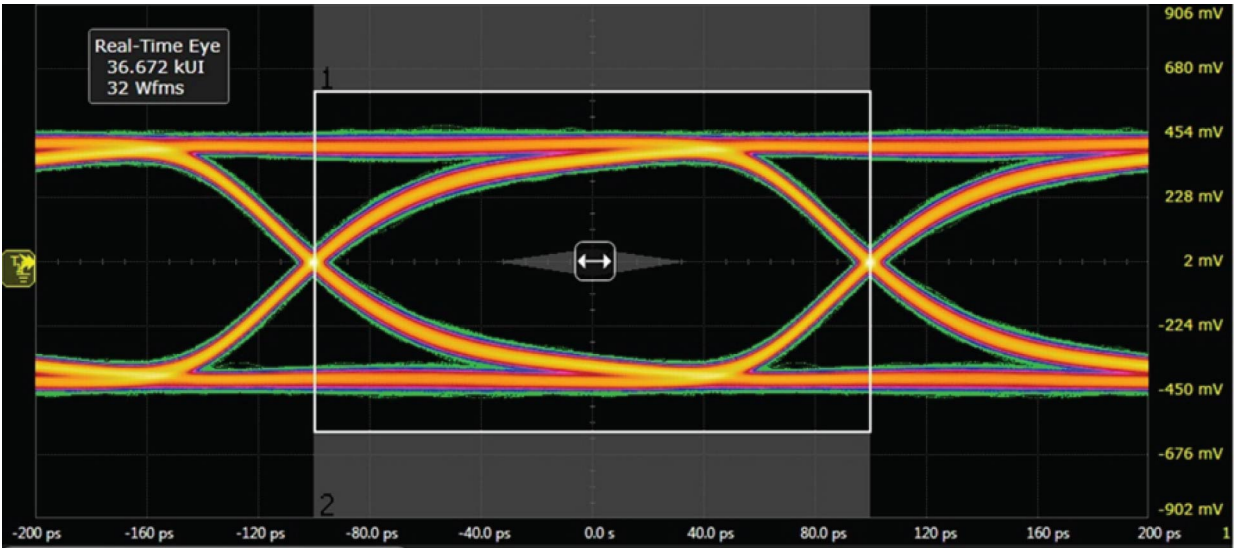
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Fig. 5. USB 3.2 eye diagram 10 Gbps, test board with PCMFxUSB3B/C; typical values



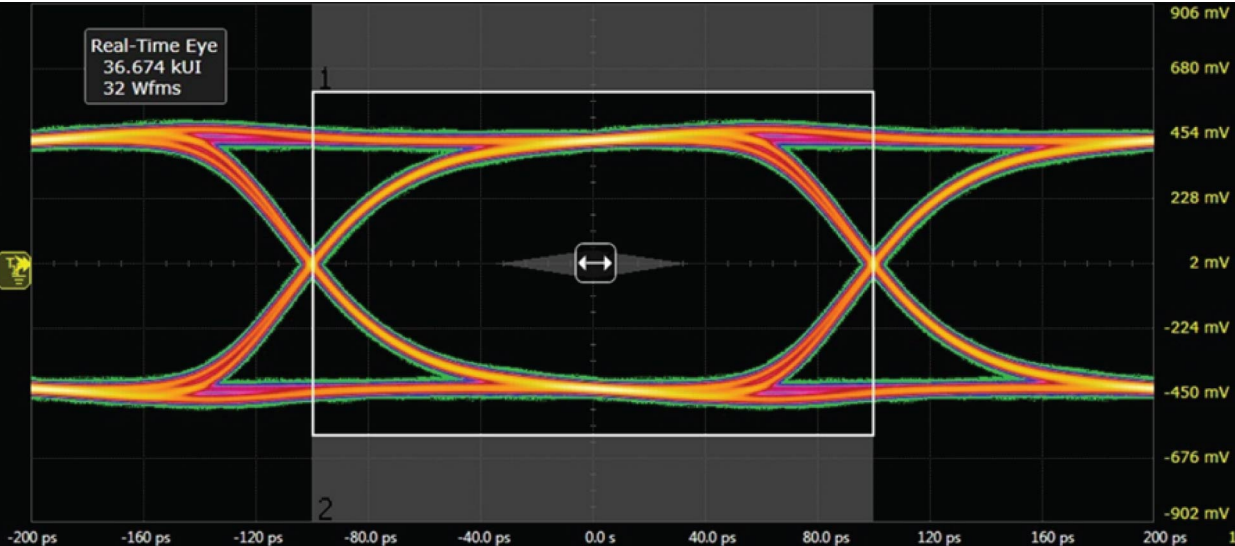
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Fig. 6. USB 3.2 eye diagram 10 Gbps, test board without device; typical values



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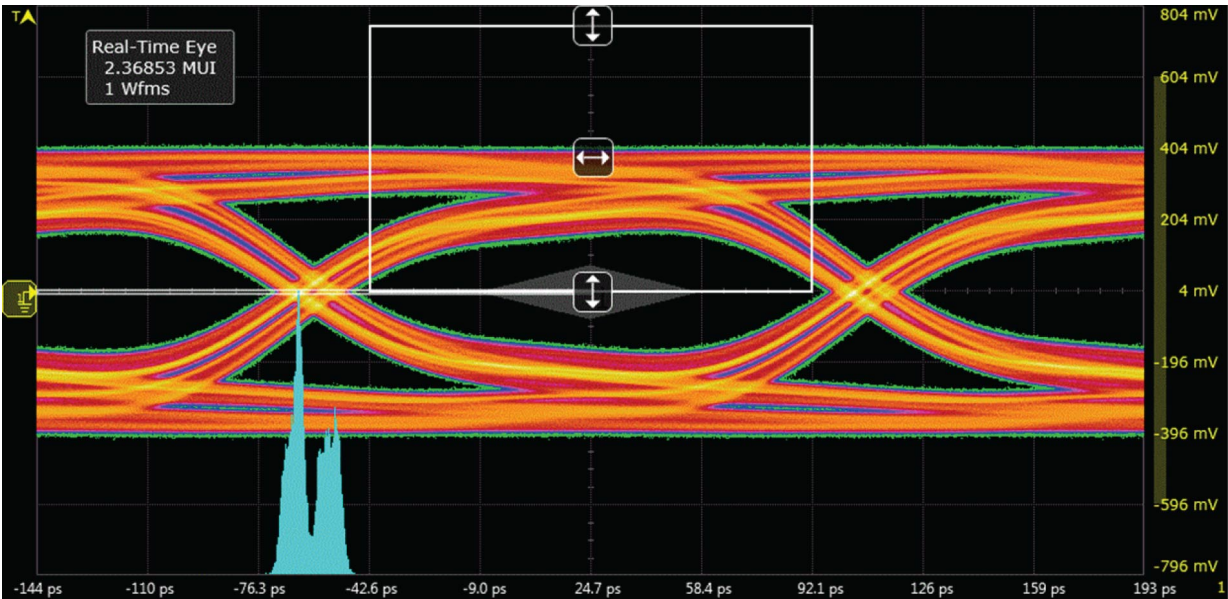
Fig. 7. USB 3.2 eye diagram 5 Gbps, test board with PCMFxUSB3B/C; typical values



aaa-028352

Fig. 8. USB 3.2 eye diagram 5 Gbps, test board without device; typical values

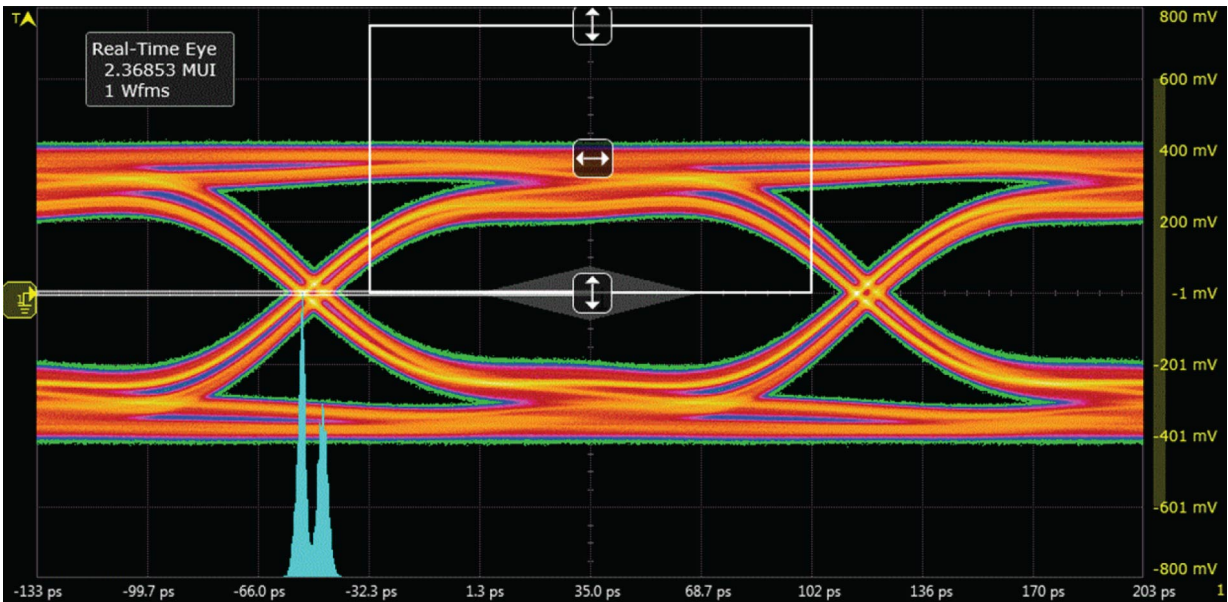




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1080p, 6 Gbps

Fig. 9. HDMI 2.0 eye diagram TP1, test board with PCMFxUSB3B/C; typical values

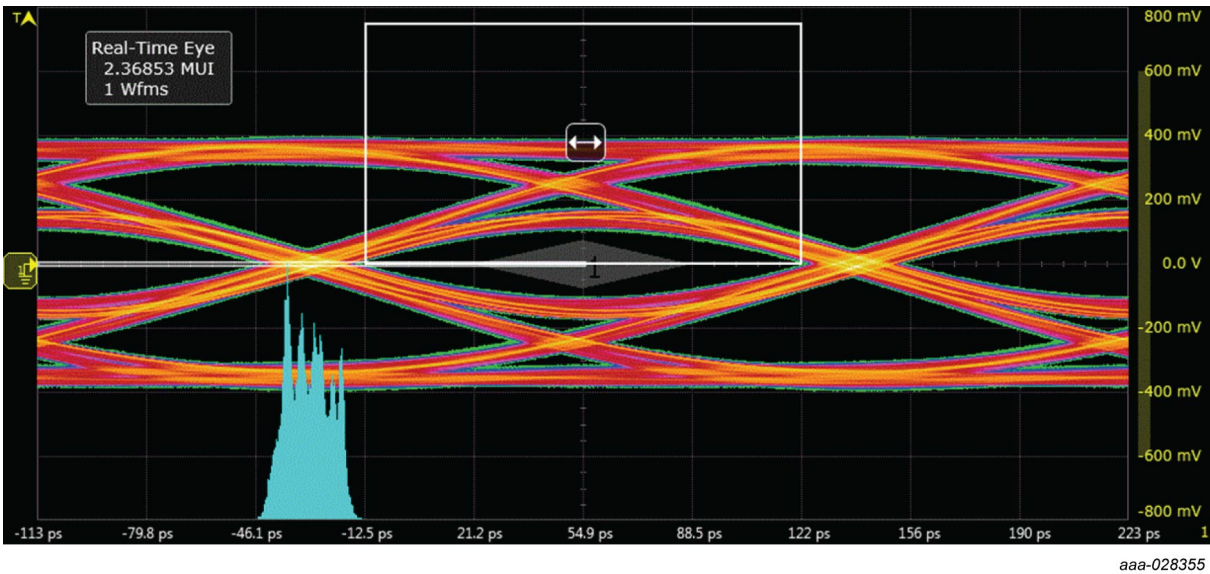


aaa-028354

1080p, 6 Gbps

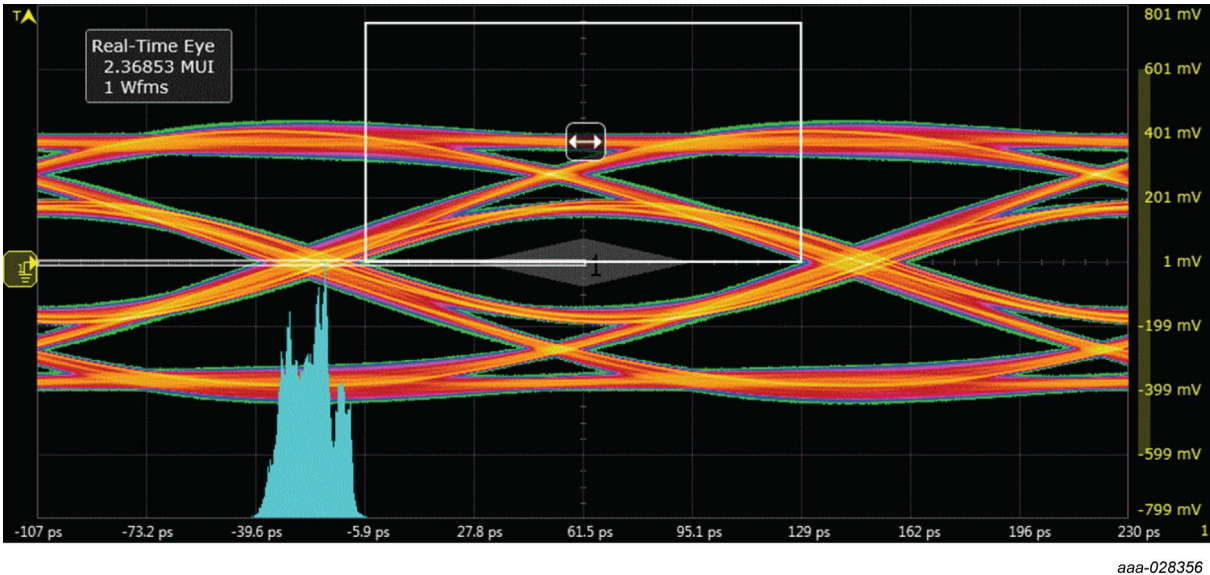
Fig. 10. HDMI 2.0 eye diagram TP1, test board without device; typical values





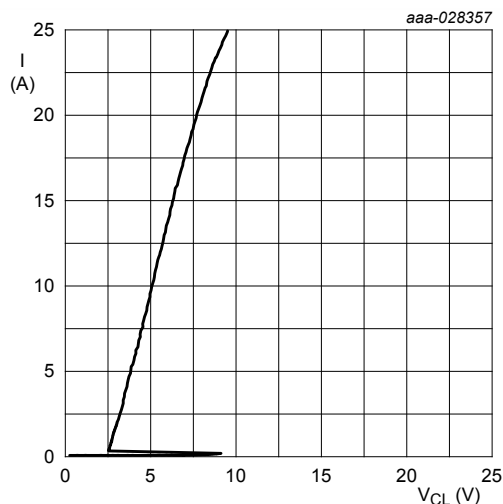
1080p, 6 Gbps

Fig. 11. HDMI 2.0 eye diagram TP2, test board with PCMFxUSB3B/C; typical values



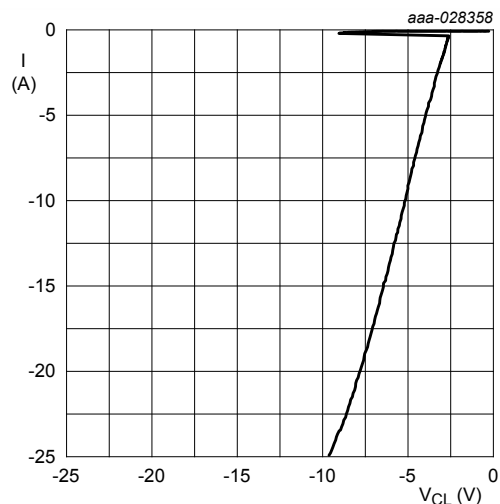
1080p, 6 Gbps

Fig. 12. HDMI 2.0 eye diagram TP2, test board without device; typical values



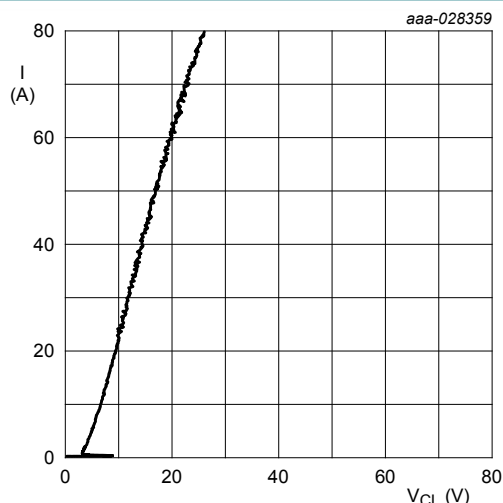
Transmission Line Pulse (TLP) = 100 ns;  
measured CH\_IN to GND

**Fig. 13. Dynamic resistance with positive clamping; typical values**



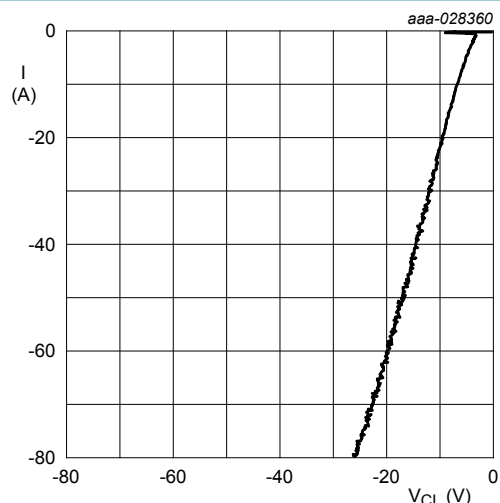
Transmission Line Pulse (TLP) = 100 ns;  
measured CH\_IN to GND

**Fig. 14. Dynamic resistance with negative clamping; typical values**



Very-Fast Transmission Line Pulse  
(VF-TLP) = 5 ns;  
measured CH\_IN to GND

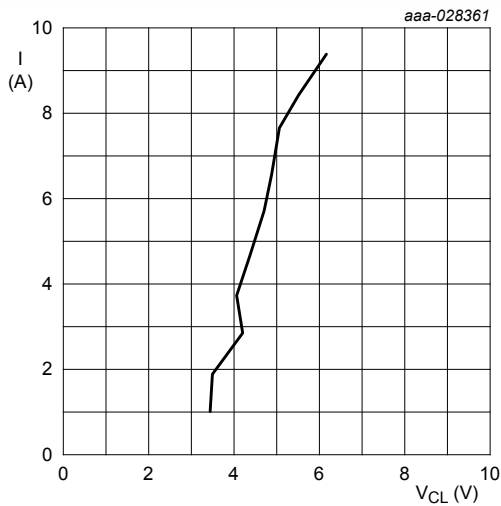
**Fig. 15. Dynamic resistance with positive clamping; typical values**



Very-Fast Transmission Line Pulse  
(VF-TLP) = 5 ns;  
measured CH\_IN to GND

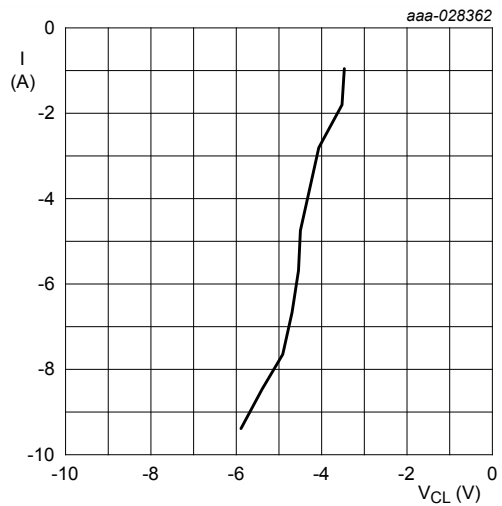
**Fig. 16. Dynamic resistance with negative clamping; typical values**

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



IEC61000-4-5;  $t_p = 8/20 \mu s$ ; positive pulse

Fig. 17. Dynamic resistance with positive clamping; typical values



IEC61000-4-5;  $t_p = 8/20 \mu s$ ; negative pulse

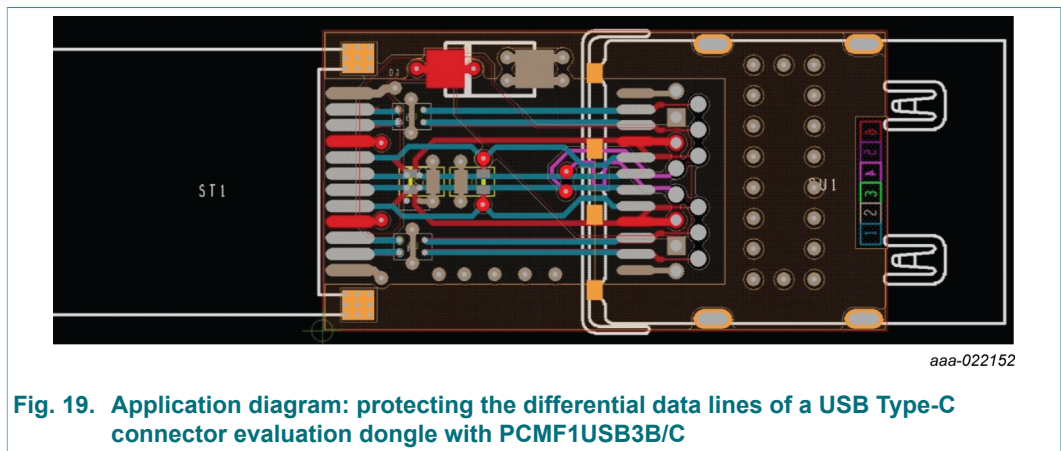
Fig. 18. Dynamic resistance with negative clamping; typical values

## 9. Application information

The device is designed to provide high-level ESD protection for differential high-speed data line pairs such as:

- USB 3.2
- HDMI 2.0
- Transition-Minimized Differential Signaling (TMDS)
- DisplayPort
- external Serial Advanced Technology Attachment (eSATA)
- Low Voltage Differential Signaling (LVDS)

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the protected signal lines to unlimited current sources like, for example, a battery.



Since the SuperSpeed TX/RX lines are separated by GND or VBUS from the Hi-Speed lines, PCMF1USB3B/C makes it easy to achieve same signal lengths, straight routing, and optimal positioning for ESD protection directly at the connector.

10. Package outline

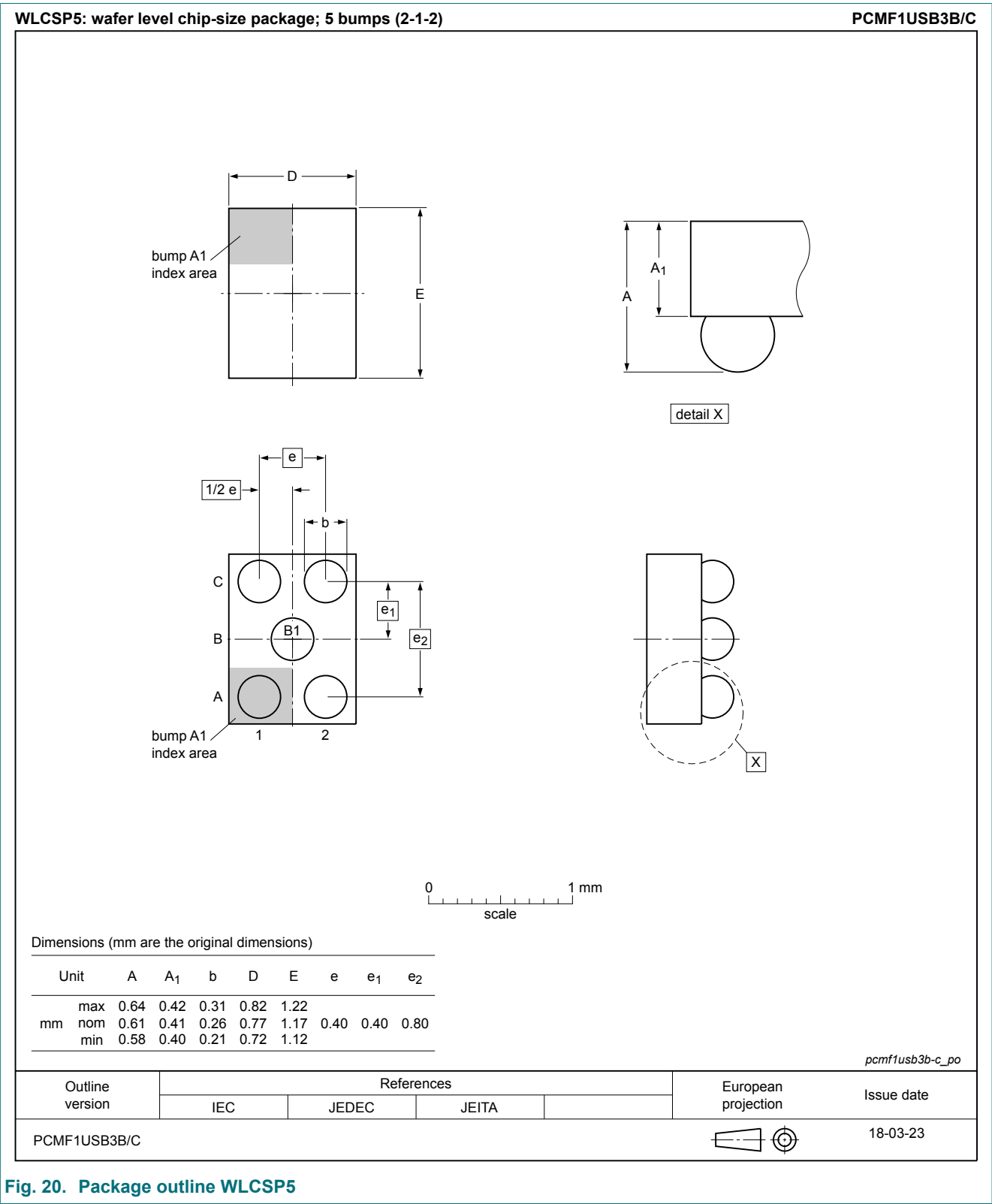


Fig. 20. Package outline WLCSP5

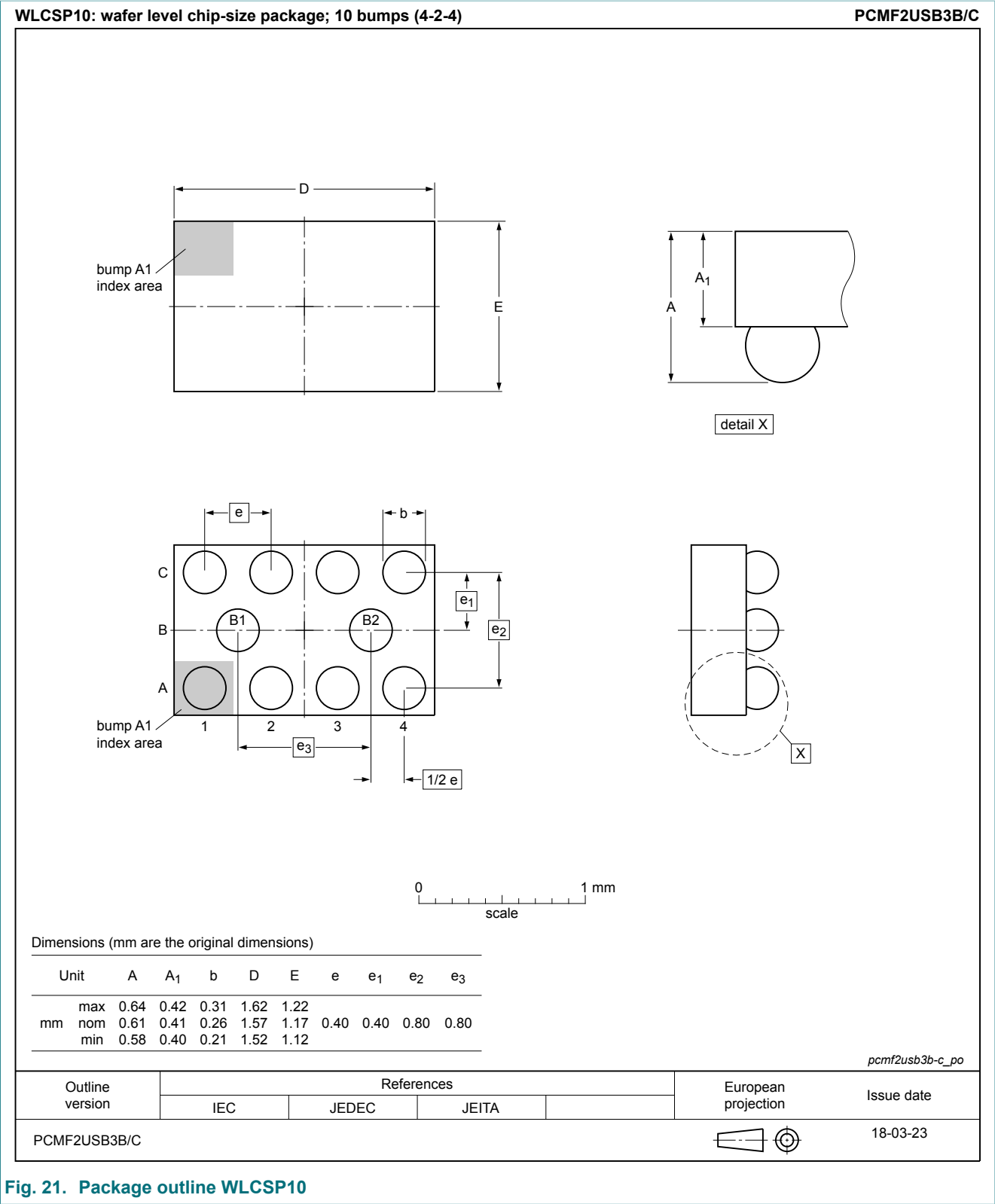


Fig. 21. Package outline WLCSP10



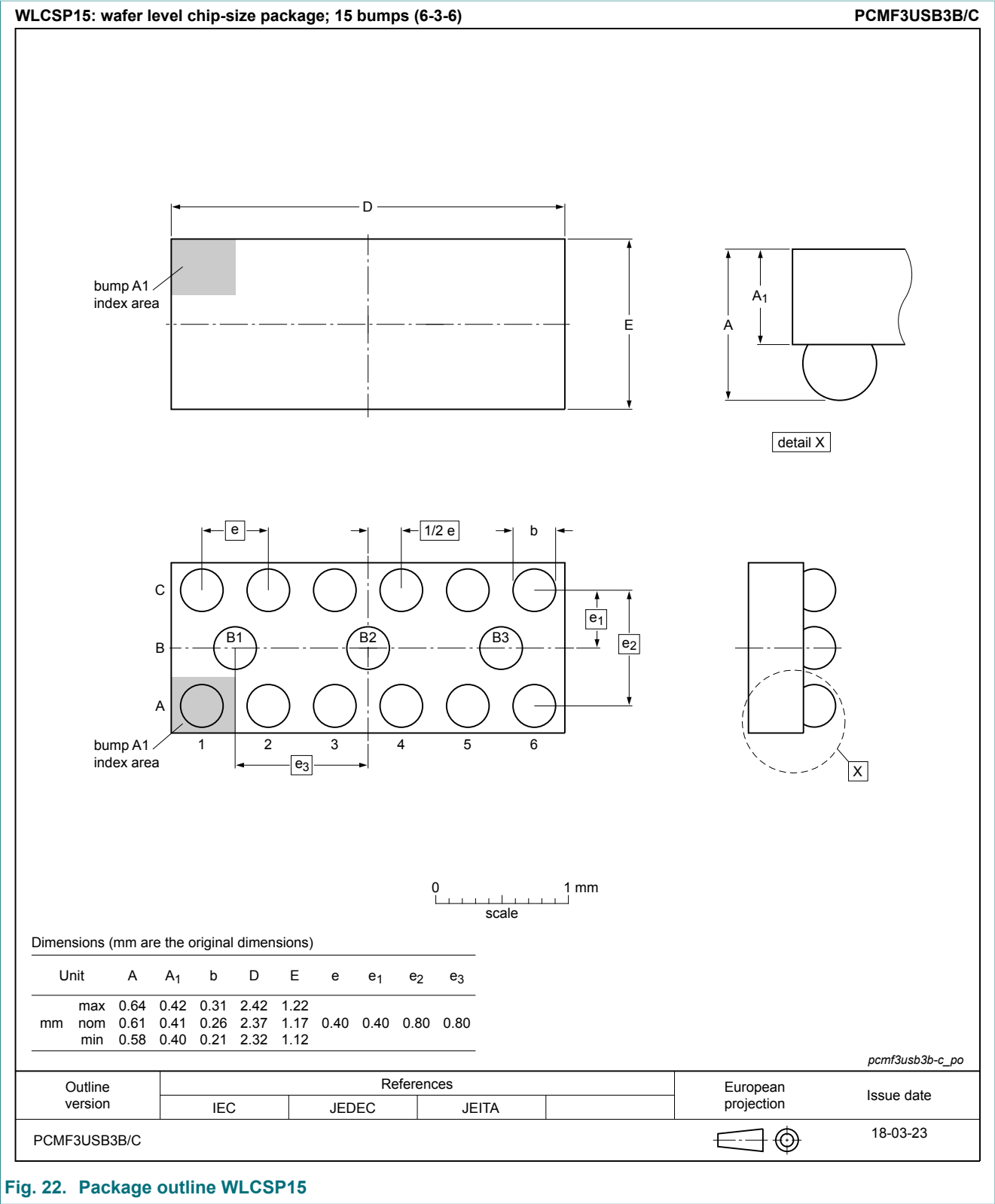
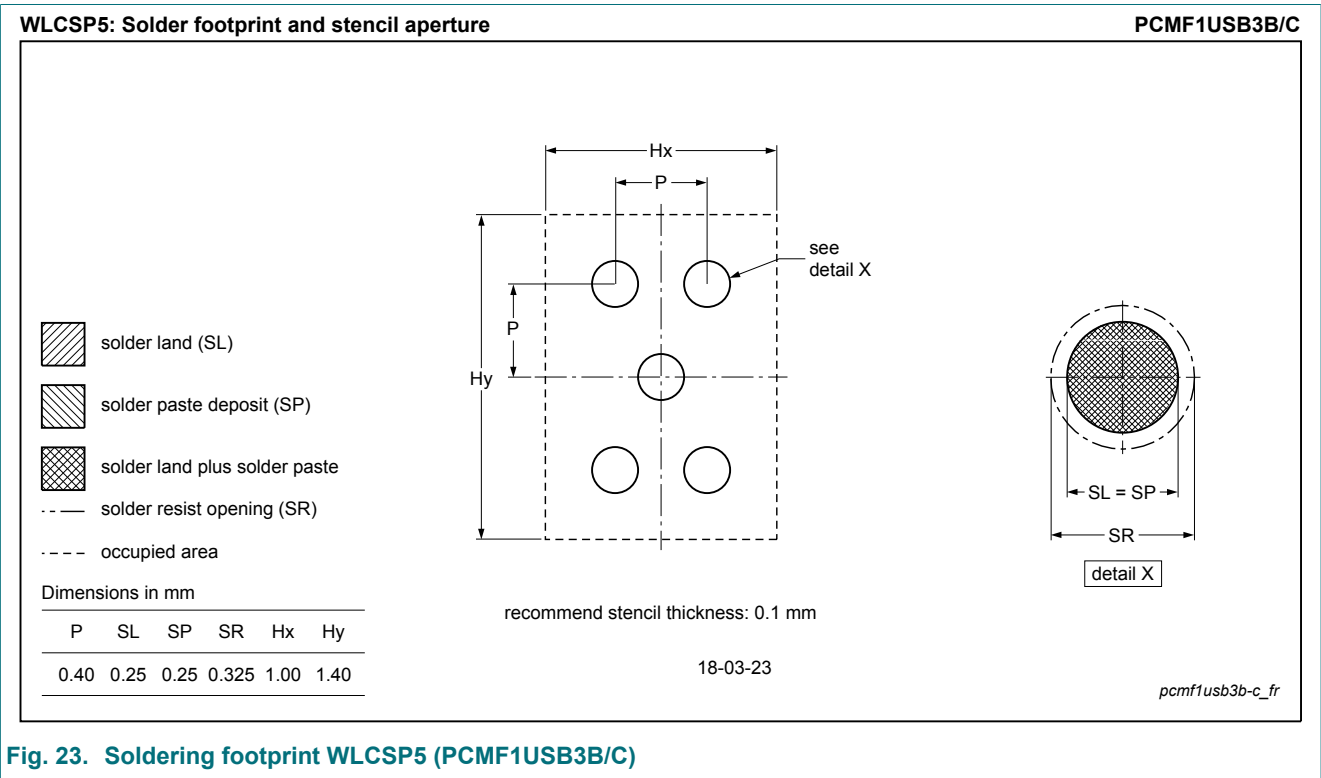
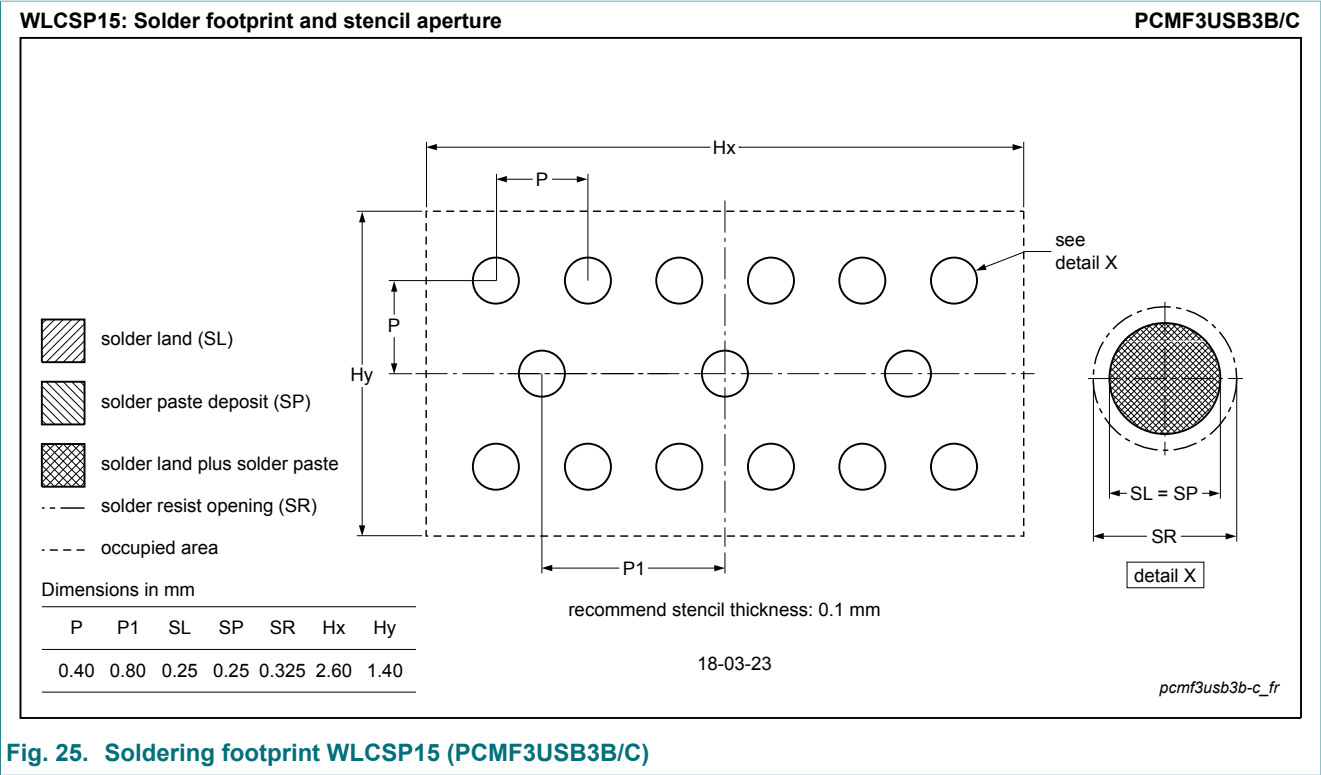


Fig. 22. Package outline WLCSP15

11. Soldering





## 12. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCMFxUSB3B_C_SER v.2	20190129	Product data sheet	-	PCMFxUSB3B_C_SER v.1
Modifications:	<ul style="list-style-type: none"><li>Limiting values: <math>T_{amb}</math> updated.</li><li>Channel characteristics: Sentence inserted; <math>R_{S(ch)}</math> inserted.</li><li>Frequency characteristics: Sentence inserted; Fig 2 updated.</li></ul>			
PCMFxUSB3B_C_SER v.1	20180507	Product data sheet	-	-

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 29 January 2019



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