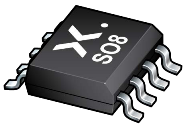

PBSS4032SP

30 V, 4.8 A PNP/PNP low V_{CEsat} (BISS) transistor

Rev. 2 — 13 October 2010 Product data sheet

1. Product profile

1.1 General description

PNP/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT96-1 (SO8) medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/NPN complement	NPN/PNP complement
	Nexperia	Name		
PBSS4032SP	SOT96-1	SO8	PBSS4032SN	PBSS4032SPN

1.2 Features and benefits

- Low collector-emitter saturation voltage V_{CEsat}
- Optimized switching time
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- Battery-driven devices
- Power management
- Charging circuits

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	–30	V
I_C	collector current		-	-	–4.8	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	–10	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = –4$ A; $I_B = –0.4$ A [1]	-	65	98	mΩ

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.

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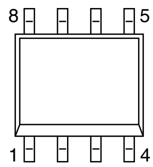
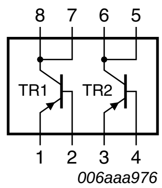
2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4032SP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4032SP	4032SP

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{CBO}	collector-base voltage	open emitter		-	–30	V
V_{CEO}	collector-emitter voltage	open base		-	–30	V
V_{EBO}	emitter-base voltage	open collector		-	–5	V
I_C	collector current			-	–4.8	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	–10	A
I_B	base current			-	–1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.73	W
			[2]	-	1	W
			[3]	-	1.7	W

Table 6. Limiting values *...continued*

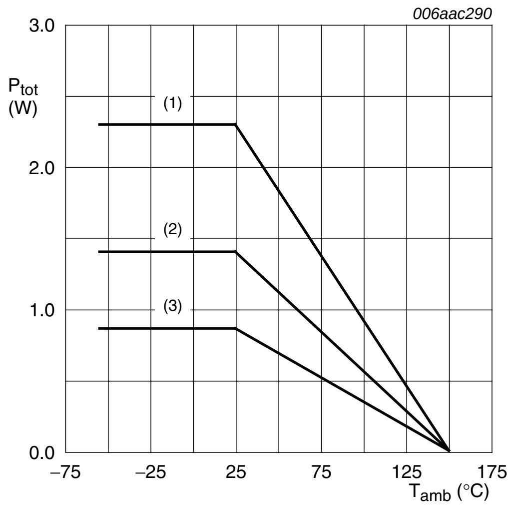
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.86	W
			[2]	-	1.4	W
			[3]	-	2.3	W
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			–55	+150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



(1) Ceramic PCB, Al_2O_3, standard footprint

(2) FR4 PCB, mounting pad for collector 1 cm^2

(3) FR4 PCB, standard footprint

Fig 1. Per device: Power derating curves

6. Thermal characteristics

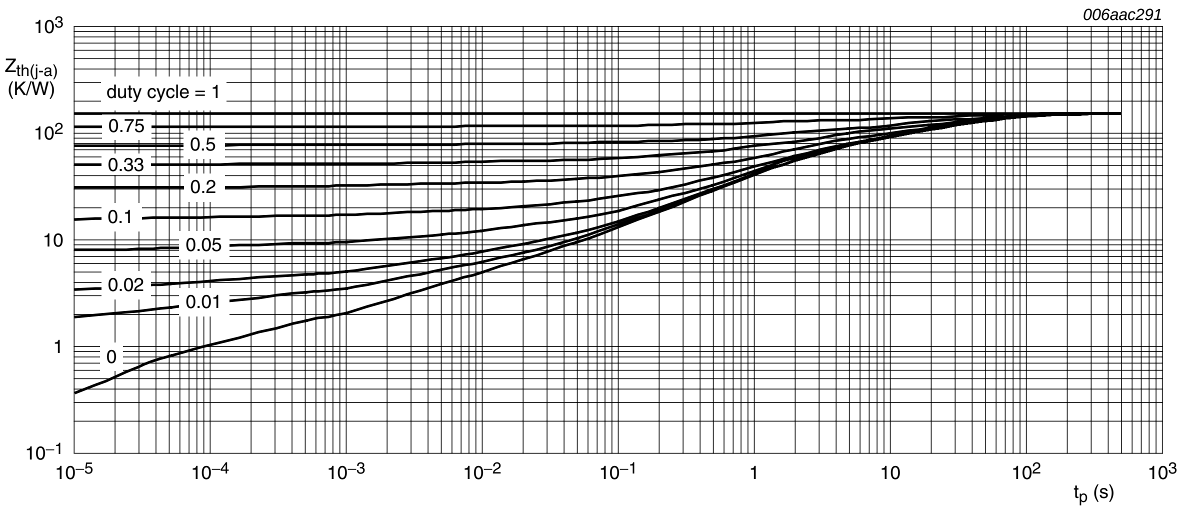
Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	170	K/W
			[2]	-	-	125	K/W
			[3]	-	-	75	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	40	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	145	K/W
			[2]	-	-	90	K/W
			[3]	-	-	55	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

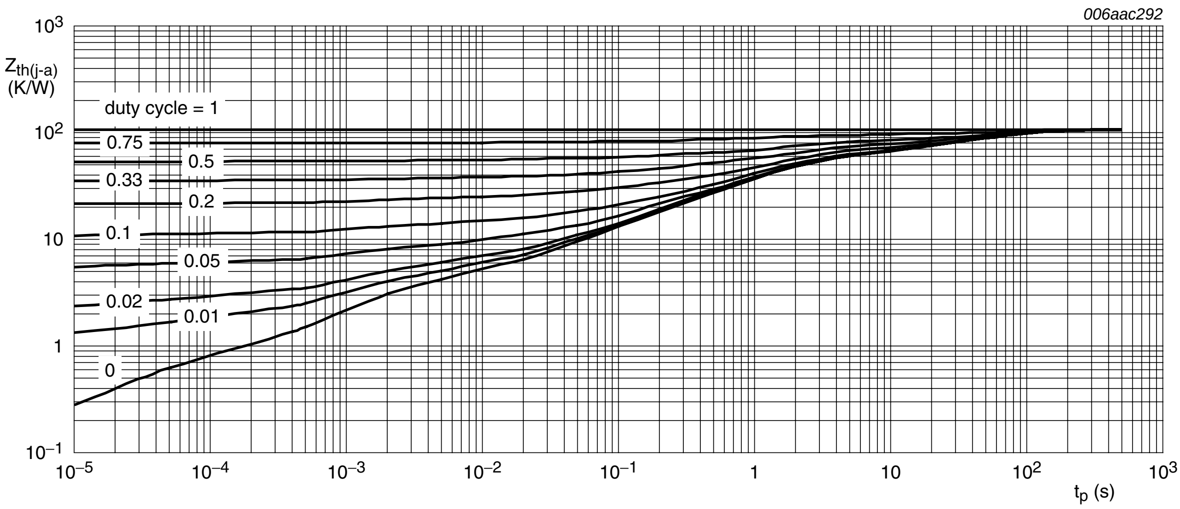
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on a ceramic PCB, Al_2O_3, standard footprint.



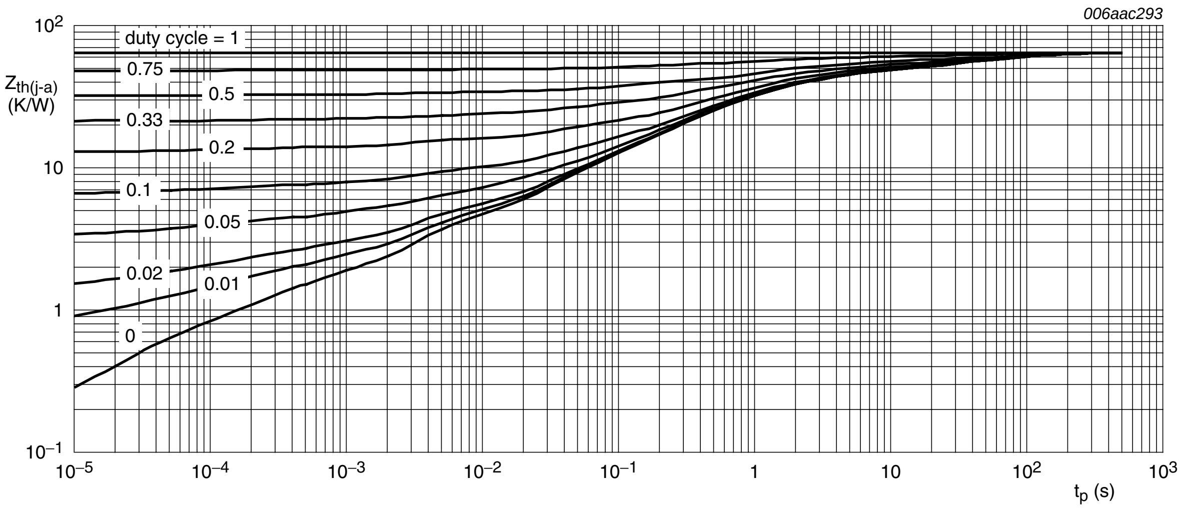
FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm^2

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al_2O_3, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

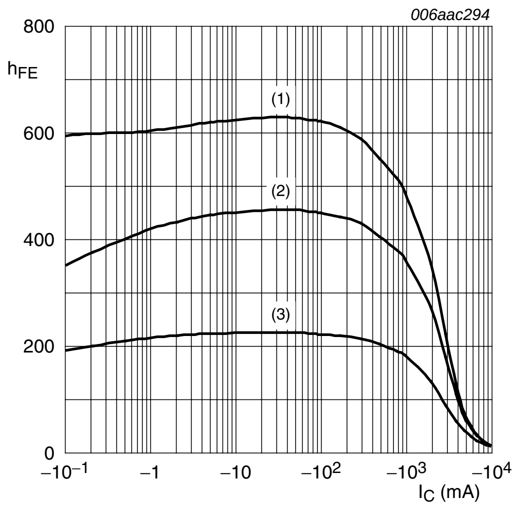
7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
I_{CBO}	collector-base cut-off current	V_{CB} = −30 V; I_E = 0 A		-	-	−100	nA
		V_{CB} = −30 V; I_E = 0 A; T_j = 150 °C		-	-	−50	μA
I_{CES}	collector-emitter cut-off current	V_{CE} = −24 V; V_{BE} = 0 V		-	-	−100	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = −5 V; I_C = 0 A		-	-	−100	nA
h_{FE}	DC current gain	V_{CE} = −2 V	[1]				
		I_C = −500 mA		200	380	-	
		I_C = −1 A		200	330	-	
		I_C = −2 A		150	250	-	
		I_C = −4 A		60	100	-	
		I_C = −5 A		40	60	-	
V_{CEsat}	collector-emitter saturation voltage		[1]				
		I_C = −1 A; I_B = −50 mA		-	−115	−165	mV
		I_C = −1 A; I_B = −10 mA		-	−170	−240	mV
		I_C = −2 A; I_B = −40 mA		-	−210	−300	mV
		I_C = −4 A; I_B = −400 mA		-	−260	−390	mV
		I_C = −4 A; I_B = −200 mA		-	−300	−450	mV
		I_C = −5 A; I_B = −250 mA		-	−340	−510	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = −4 A; I_B = −400 mA	[1]	-	65	98	mΩ
V_{BEsat}	base-emitter saturation voltage		[1]				
		I_C = −1 A; I_B = −100 mA		-	−0.8	−0.9	V
		I_C = −4 A; I_B = −400 mA		-	−0.99	−1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = −2 V; I_C = −2 A	[1]	-	−0.81	−0.9	V
t_d	delay time	V_{CC} = −12.5 V; I_C = −1 A; I_{Bon} = −0.05 A; I_{Boff} = 0.05 A		-	30	-	ns
t_r	rise time			-	60	-	ns
t_{on}	turn-on time			-	90	-	ns
t_s	storage time			-	140	-	ns
t_f	fall time			-	80	-	ns
t_{off}	turn-off time			-	220	-	ns
f_T	transition frequency	V_{CE} = −10 V; I_C = −100 mA; f = 100 MHz		-	115	-	MHz
C_c	collector capacitance	V_{CB} = −10 V; I_E = i_e = 0 A; f = 1 MHz		-	85	-	pF

[1] Pulse test: $t_p \leq 300$ μs; $\delta \leq 0.02$.



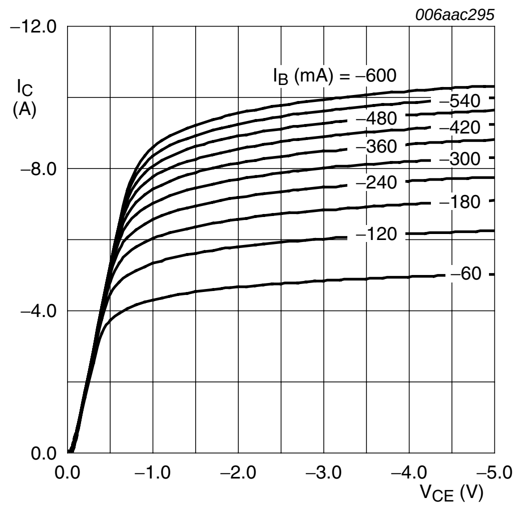
V_{CE} = −2 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

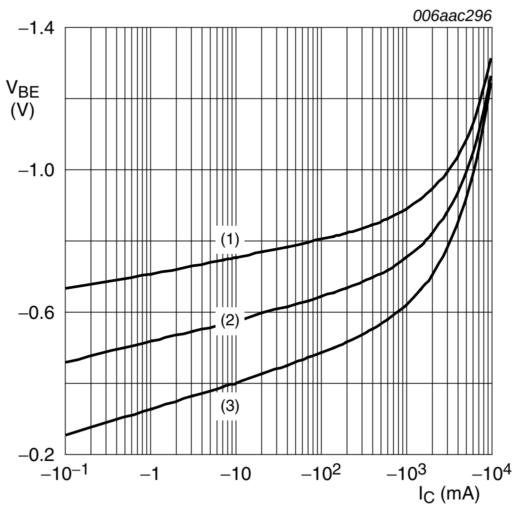
(3) T_{amb} = −55 °C

Fig 5. DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig 6. Collector current as a function of collector-emitter voltage; typical values



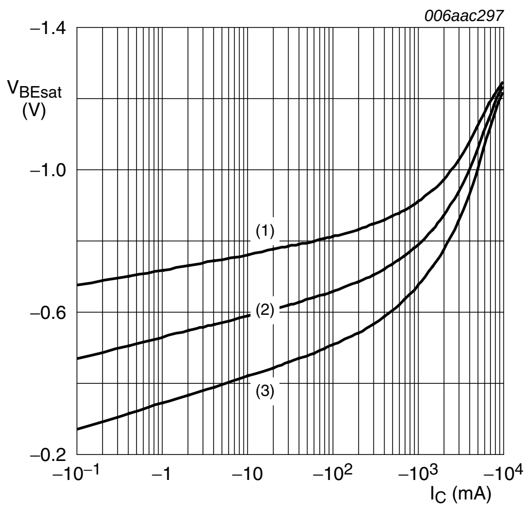
V_{CE} = −2 V

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 7. Base-emitter voltage as a function of collector current; typical values



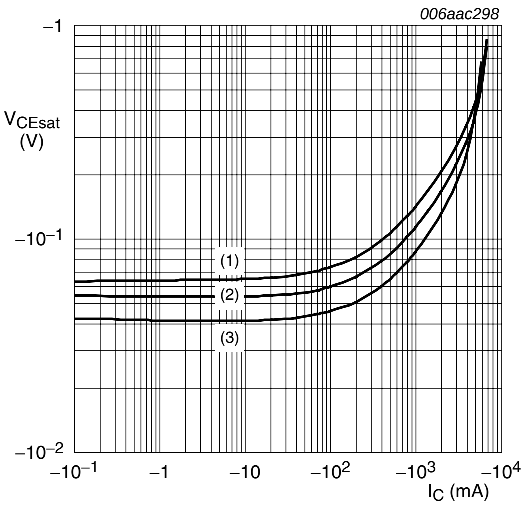
I_C/I_B = 20

(1) T_{amb} = −55 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



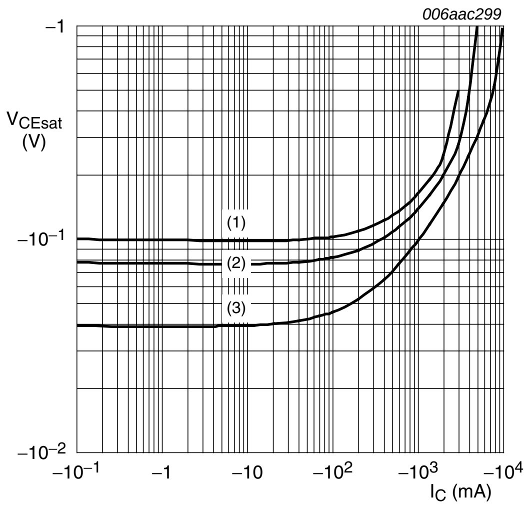
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



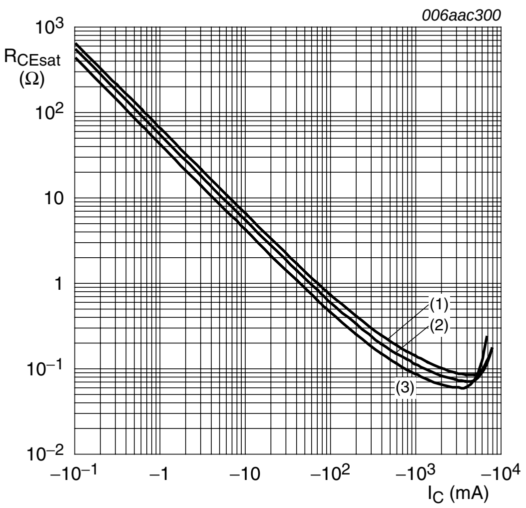
T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



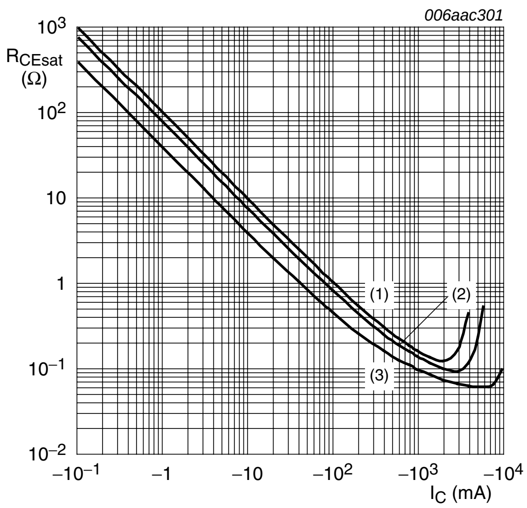
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

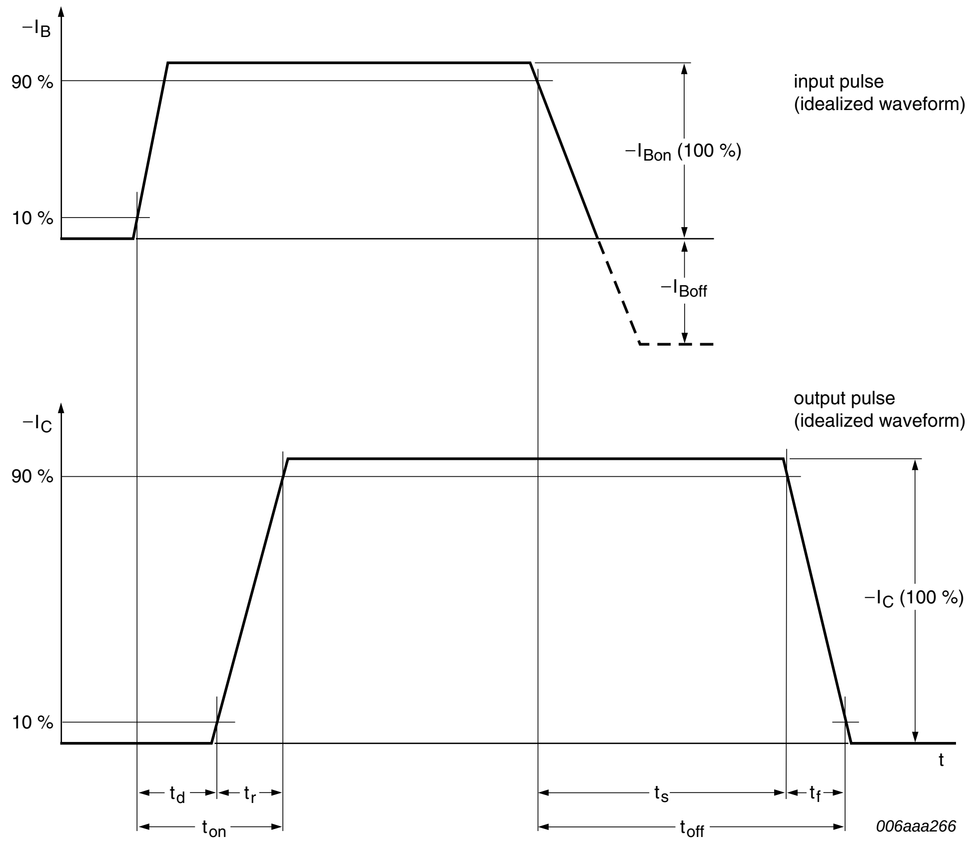
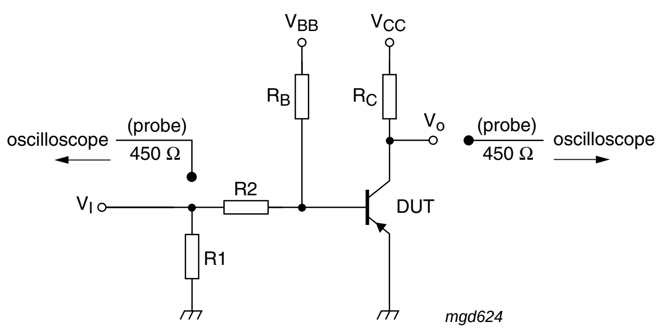


Fig 13. BISS transistor switching time definition



V_{CC} = −12.5 V; I_C = −1 A; I_{Bon} = −0.05 A; I_{Boff} = 0.05 A

Fig 14. Test circuit for switching times

9. Package outline

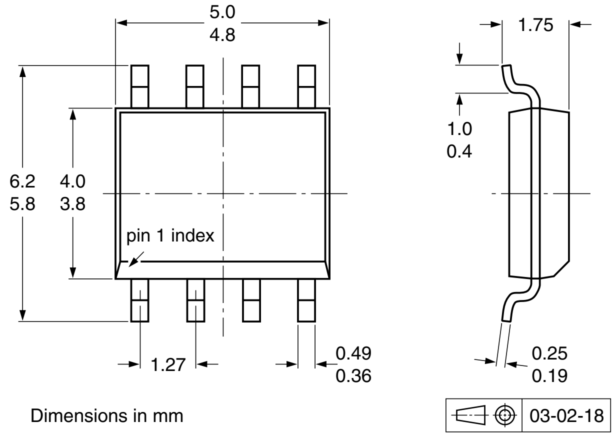


Fig 15. Package outline SOT96-1 (SO8)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			1000	**2500**
PBSS4032SP	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see Section 14.

11. Soldering

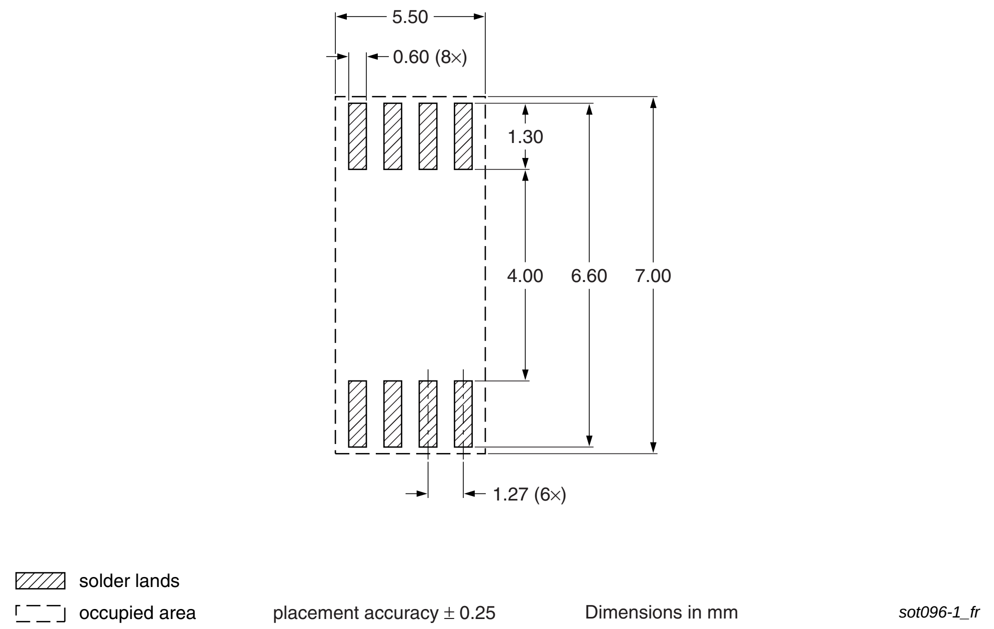


Fig 16. Reflow soldering footprint SOT96-1 (SO8)

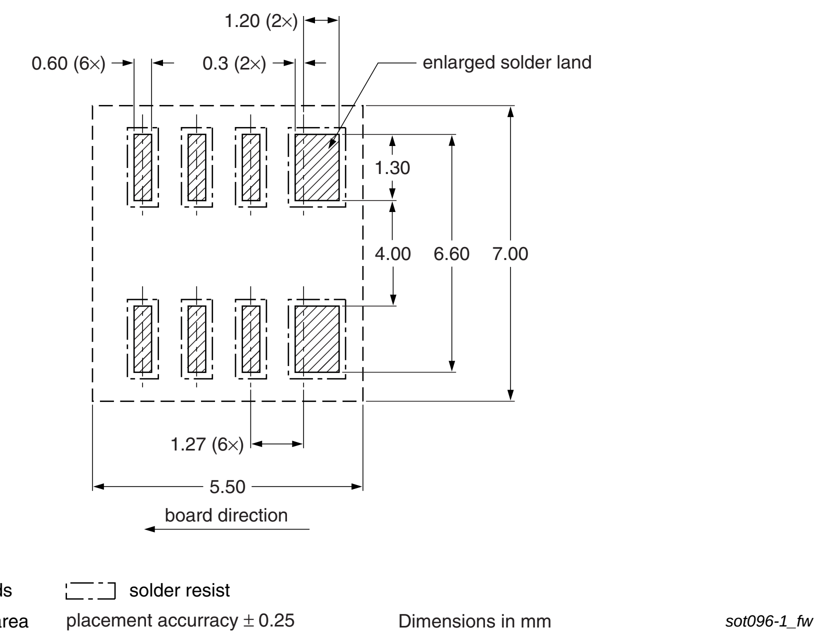


Fig 17. Wave soldering footprint SOT96-1 (SO8)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4032SP v.2	20101013	Product data sheet	-	PBSS4032SP v.1
Modifications:	• Figure 1 "Per device: Power derating curves": updated.			
PBSS4032SP v.1	20100714	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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14. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

15. Contents

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Date of release: 13 October 2010