



NX7002BKS

60 V, dual N-channel Trench MOSFET

12 May 2015

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

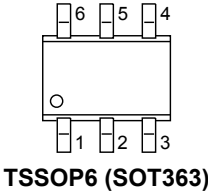
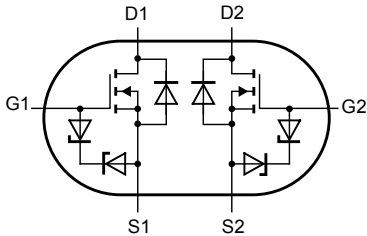
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	60	V
V _{GS}	gate-source voltage			-20	-	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C		-	-	330	mA
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	-	240	mA
Static characteristics (per transistor)							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 200 mA; T _j = 25 °C		-	2.2	2.8	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 TSSOP6 (SOT363)	 017aaa256
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX7002BKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code
NX7002BKS	LT%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{DS}	drain-source voltage	T _j = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{sp} = 25 °C		-	330	mA
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	240	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	150	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	0.8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	285	mW
			[1]	-	320	mW
		T _{sp} = 25 °C		-	870	mW
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	200	mA
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

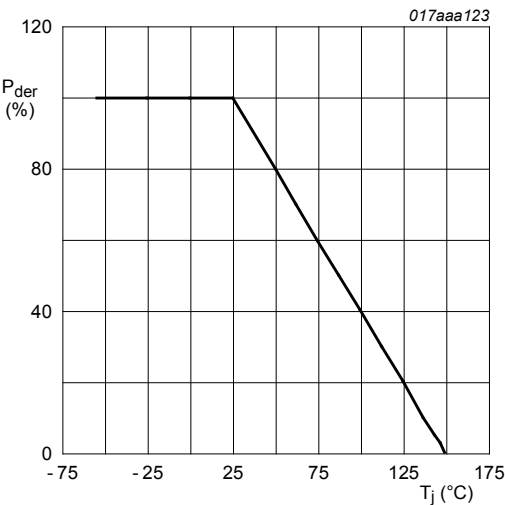


Fig. 1. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

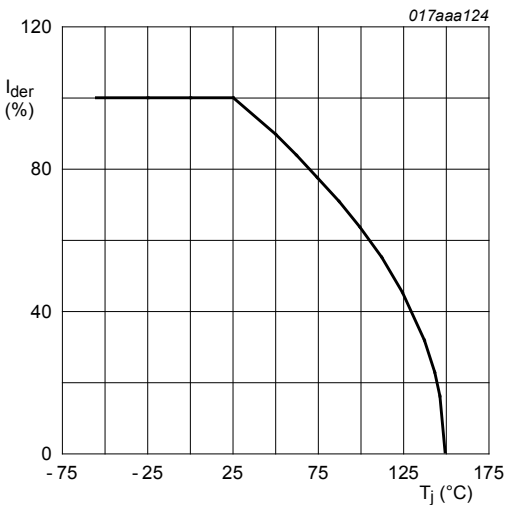


Fig. 2. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

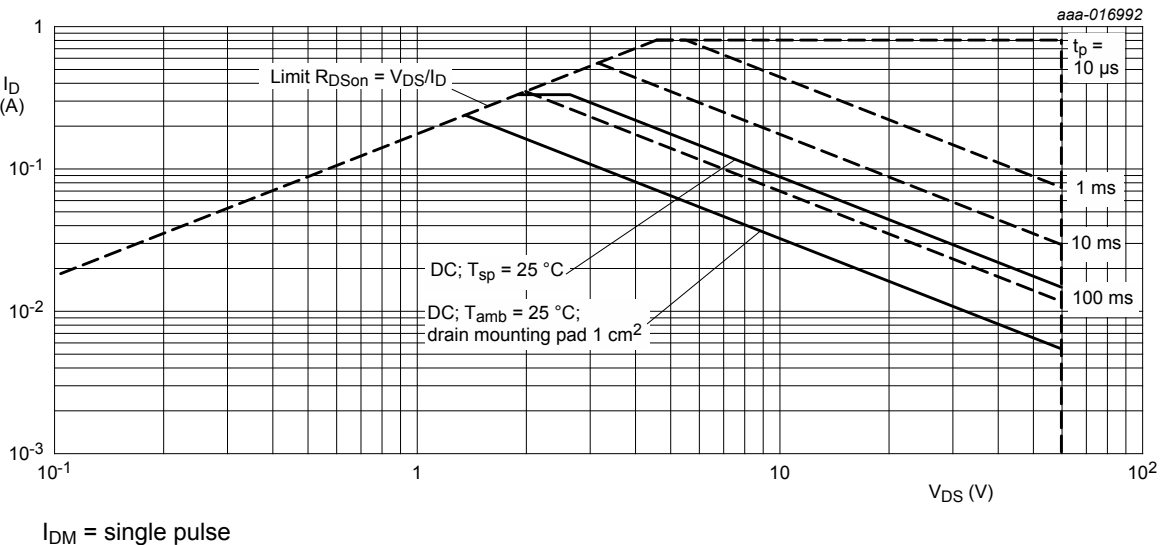


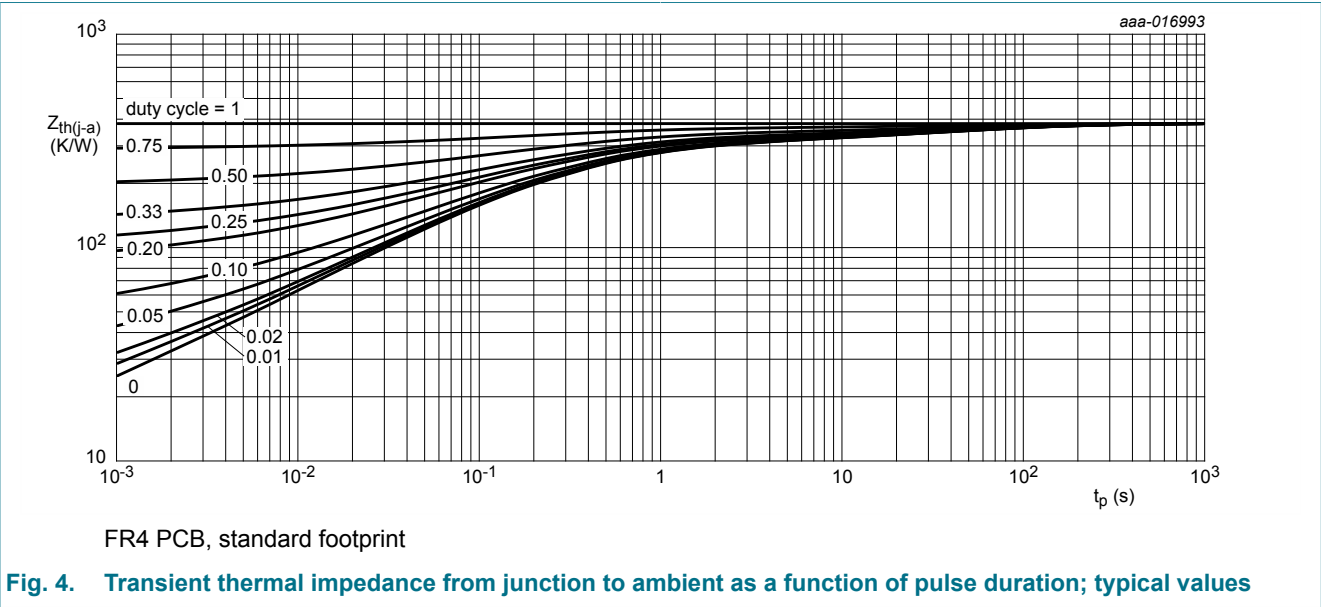
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

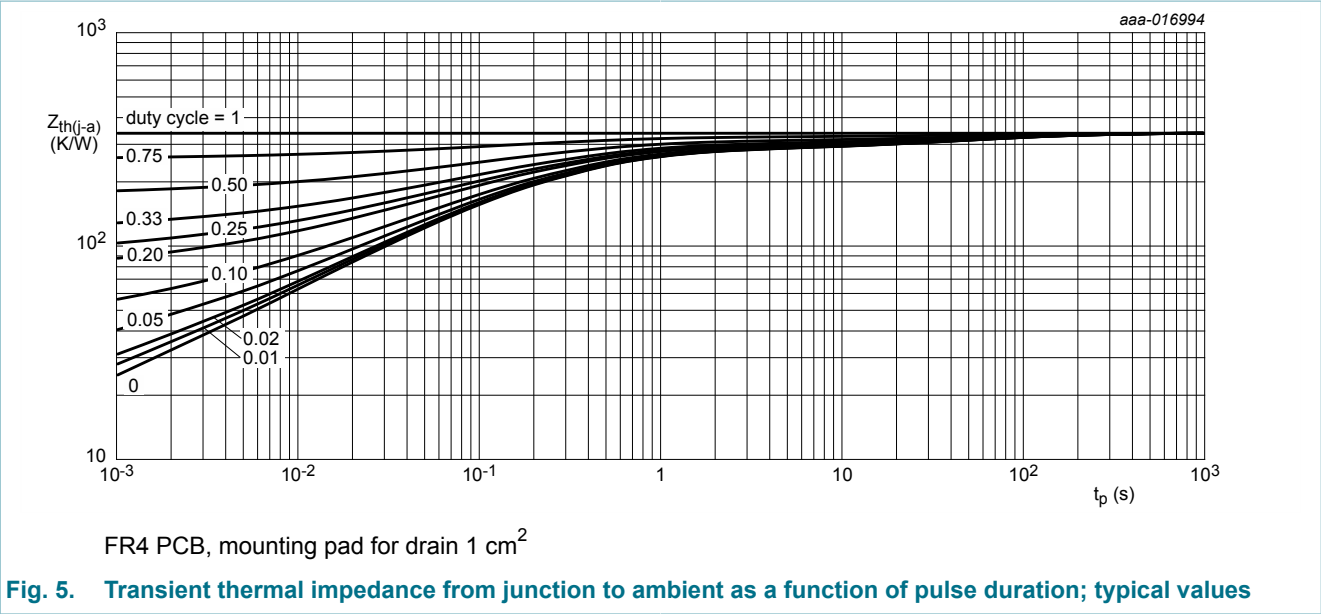
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	380	440	K/W
			[2]	-	340	390	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	125	145	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		1.1	1.6	2.1	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	0.3	μA
		V _{GS} = -5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-0.3	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 200 mA; T _j = 25 °C		-	2.2	2.8	Ω
		V _{GS} = 10 V; I _D = 200 mA; T _j = 150 °C		-	4.5	5.7	Ω
		V _{GS} = 5 V; I _D = 200 mA; T _j = 25 °C		-	2.5	3.2	Ω
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 200 mA; T _j = 25 °C		-	600	-	mS
R _G	gate resistance	f = 1 MHz		-	2.5	-	Ω
Dynamic characteristics (per transistor)							
Q _{G(tot)}	total gate charge	V _{DS} = 30 V; I _D = 200 mA; V _{GS} = 10 V; T _j = 25 °C		-	1	-	nC
Q _{GS}	gate-source charge			-	0.12	-	nC
Q _{GD}	gate-drain charge			-	0.18	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	23.6	-	pF
C _{oss}	output capacitance			-	4.6	-	pF
C _{rss}	reverse transfer capacitance			-	3	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; I _D = 200 mA; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	4.7	-	ns
t _r	rise time			-	4.3	-	ns
t _{d(off)}	turn-off delay time			-	6.9	-	ns
t _f	fall time			-	2.9	-	ns
Source-drain diode (per transistor)							
V _{SD}	source-drain voltage	I _S = 50 mA; V _{GS} = 0 V; T _j = 25 °C		-	0.87	1.2	V

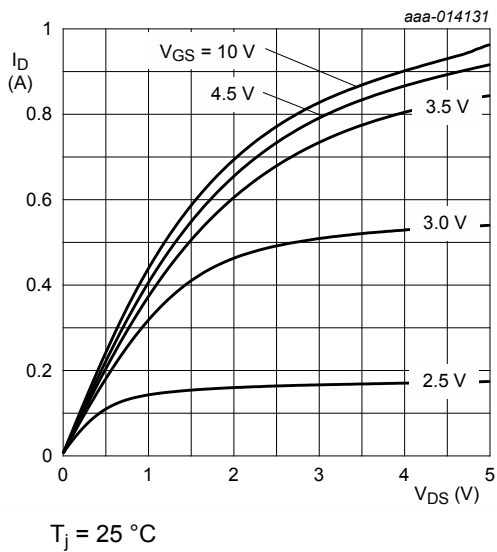


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

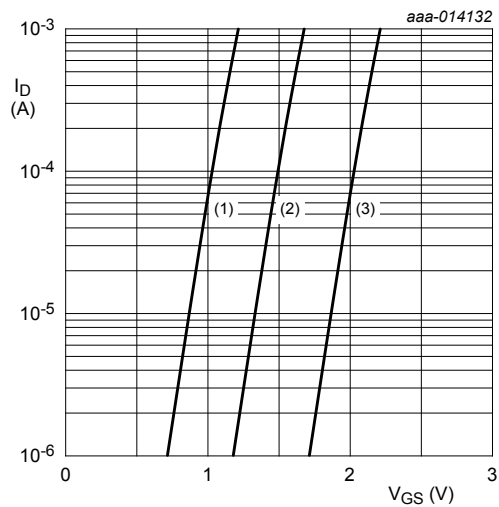


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

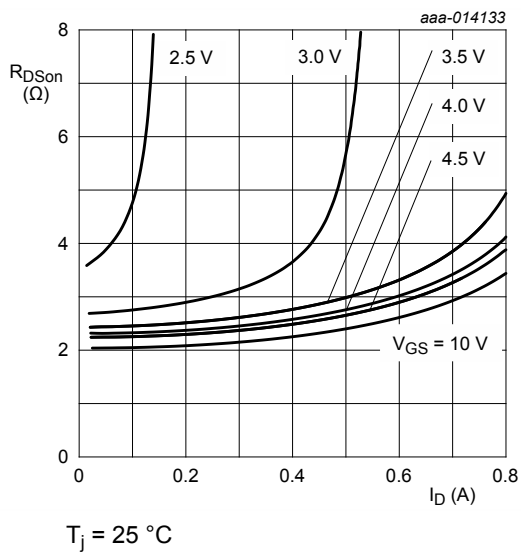


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

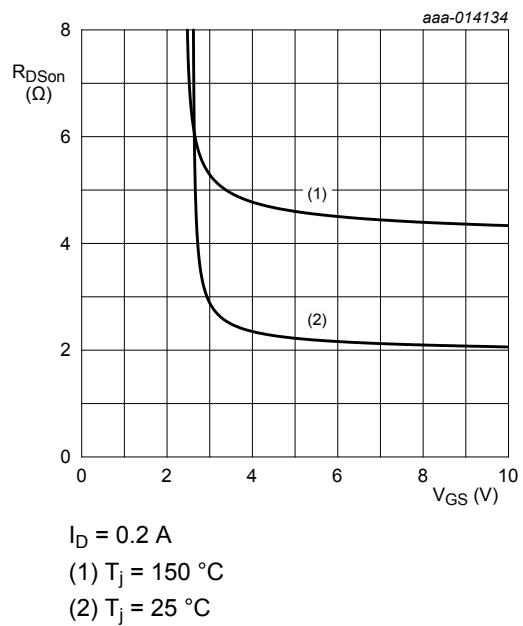
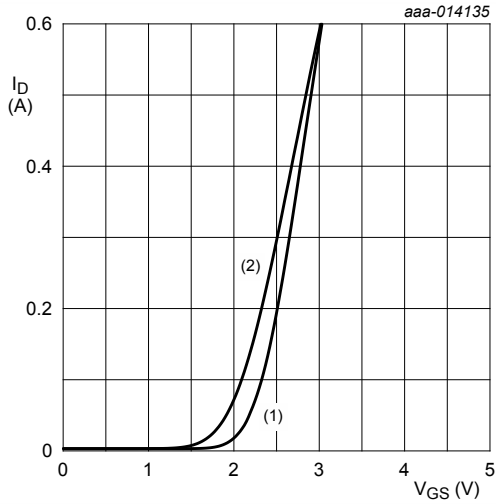


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DS(on)}$$

(1) $T_j = 25\text{ }^{\circ}\text{C}$

(2) $T_j = 150\text{ }^{\circ}\text{C}$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

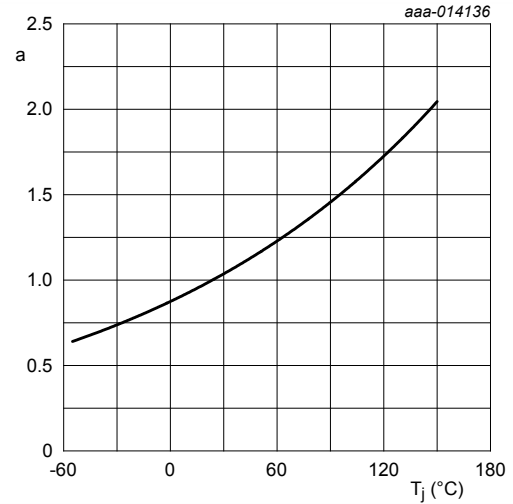
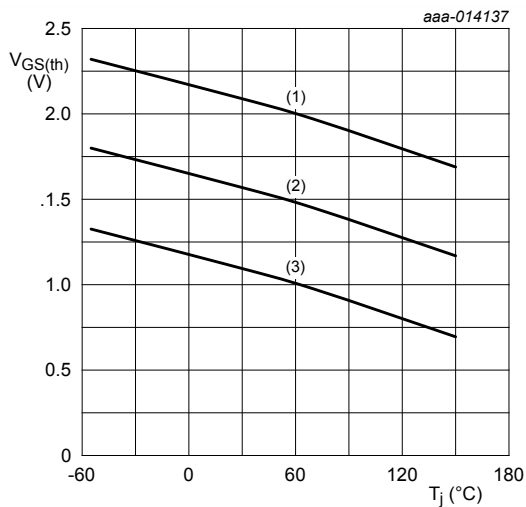


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$



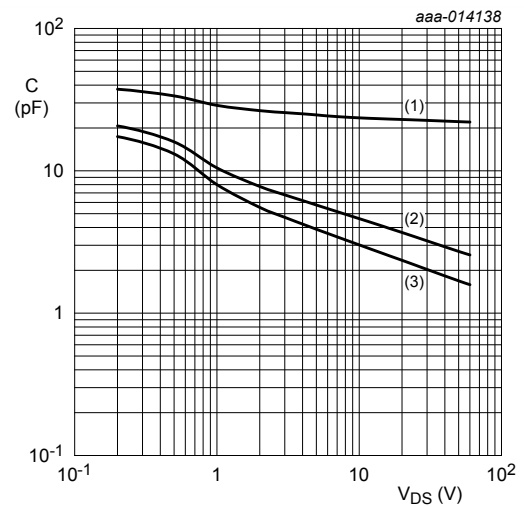
$$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$$

(1) maximum values

(2) typical values

(3) minimum values

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$$

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

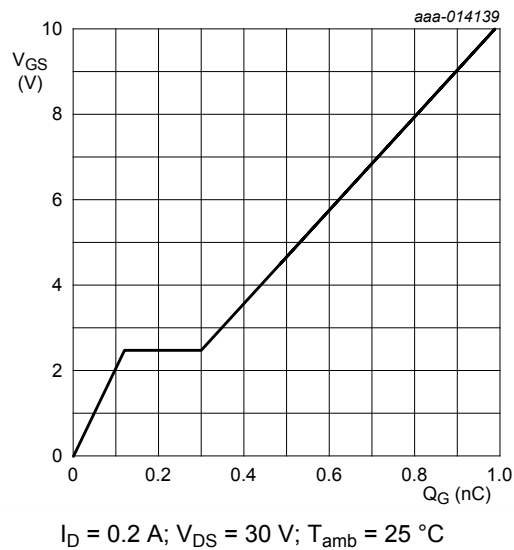


Fig. 14. Gate-source voltage as a function of gate charge; typical values

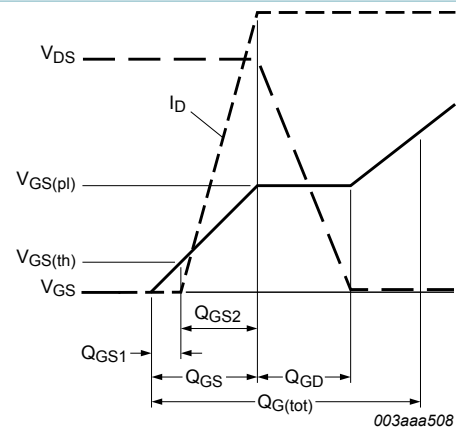
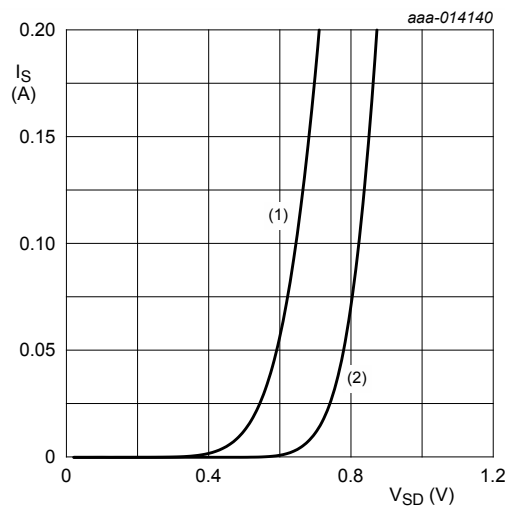


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0\text{ V}$
(1) $T_j = 150\text{ }^{\circ}\text{C}$
(2) $T_j = 25\text{ }^{\circ}\text{C}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

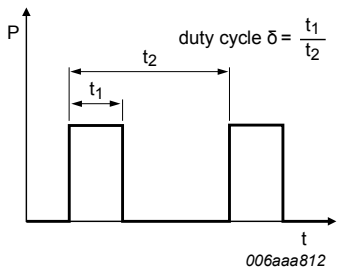


Fig. 17. Duty cycle definition

12. Package outline

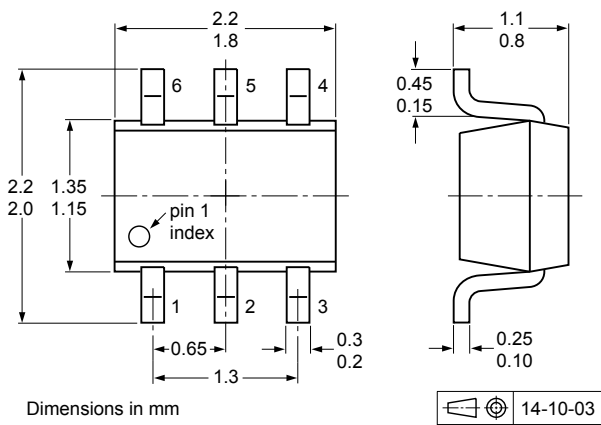


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

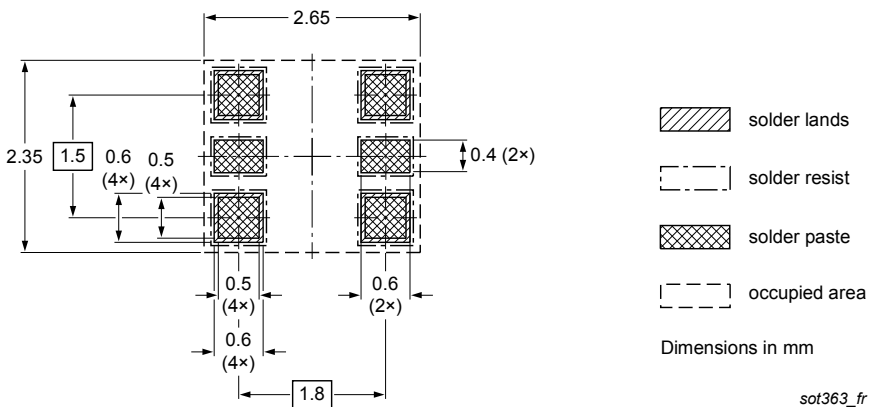
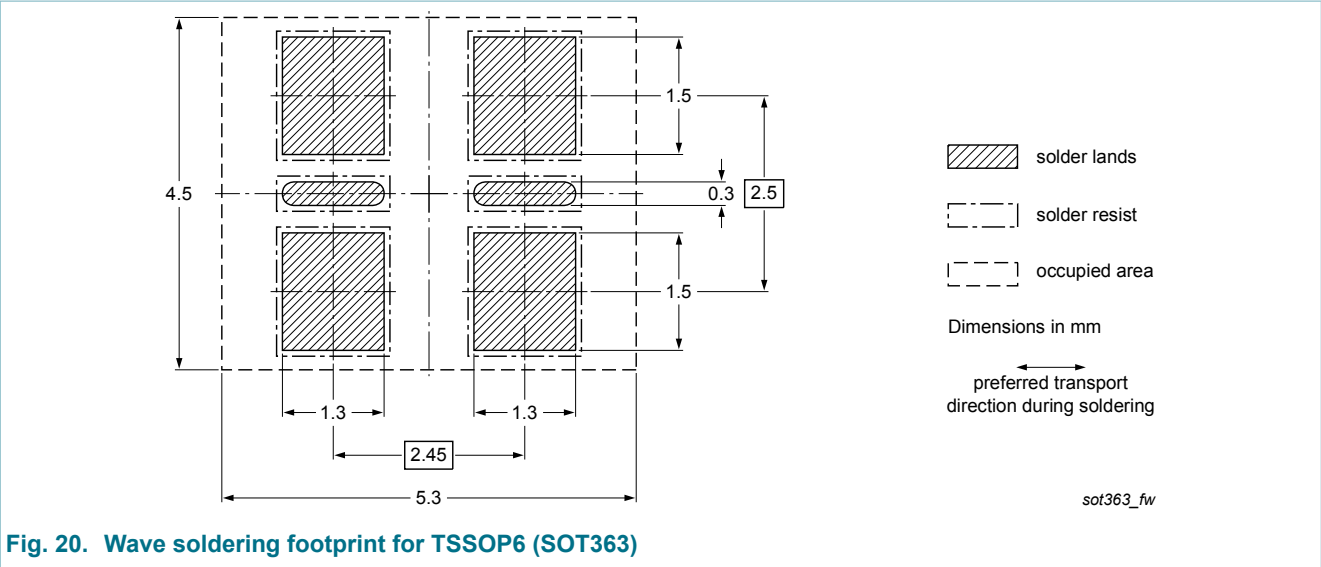


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX7002BKS v.1	20150512	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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