

# HEF4557B

## 1-to-64 bit variable length shift register

Rev. 7 — 1 April 2016

Product data sheet

### 1. General description

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the DA or DB data inputs with the A/ $\overline{B}$  select input. This feature is useful for recirculation purposes. Information on DA or DB is shifted into the first register position and all the data in the register is shifted one position to the right on the  $\overline{\text{LOW}}$  to HIGH transition of CP0 while  $\overline{\text{CP1}}$  is LOW or on the HIGH to LOW transition of  $\overline{\text{CP1}}$  while CP0 is HIGH. A HIGH on master reset (MR) resets the register and forces Q to LOW and  $\overline{Q}$  to HIGH, independent of the other inputs.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

**Table 1.** Ordering information

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Type number	Package		
	Name	Description	Version
HEF4557BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

#### 4. Functional diagram

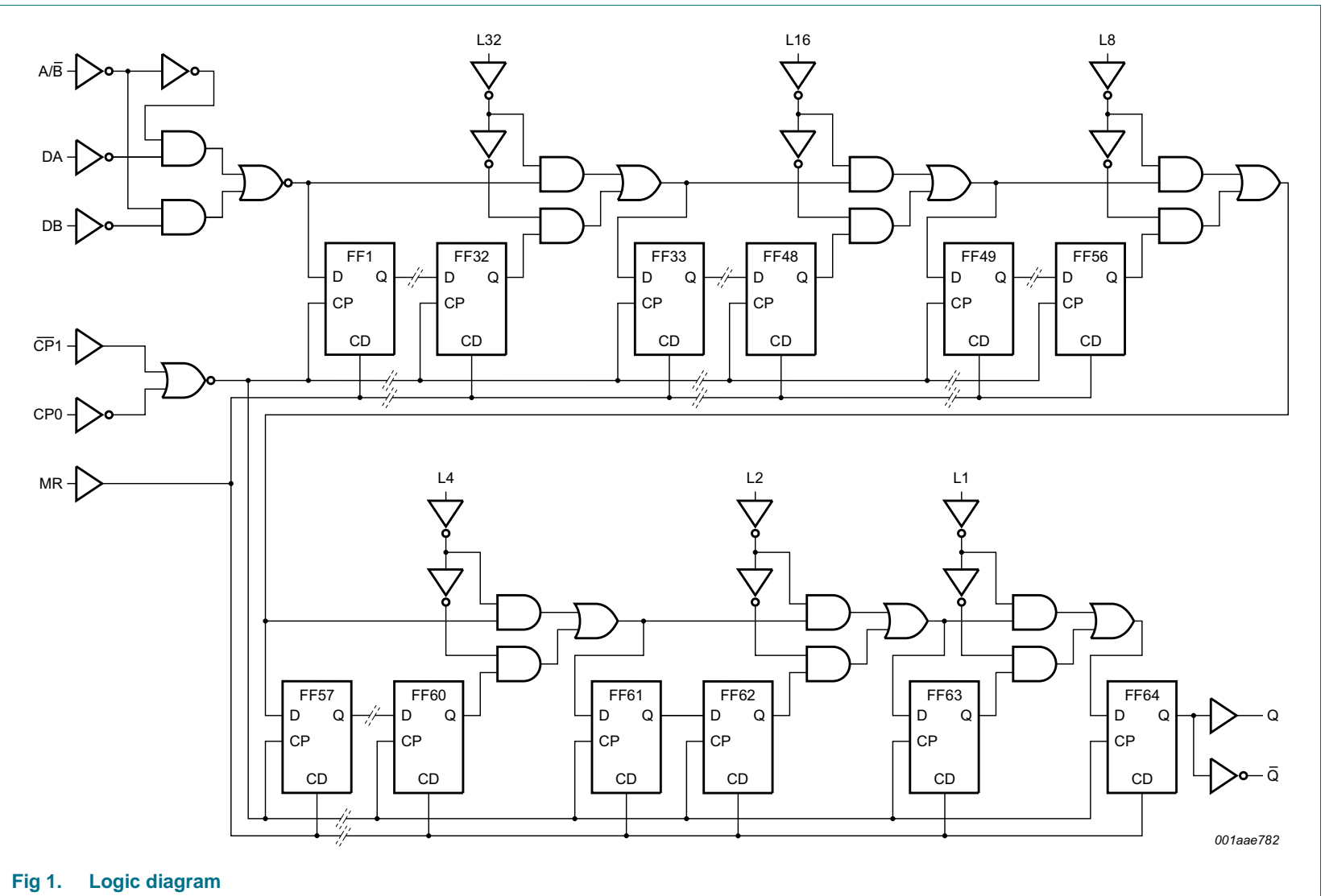


Fig 1. Logic diagram

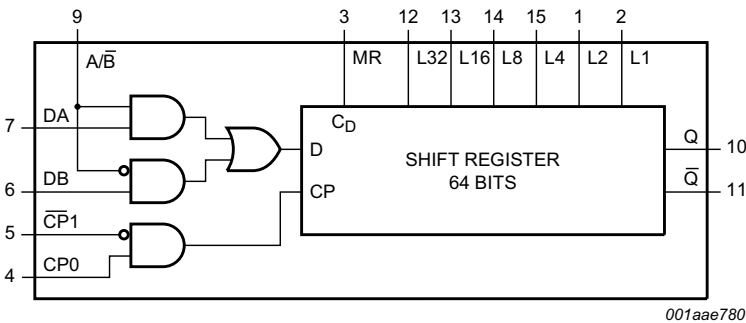


Fig 2. Functional diagram

## 5. Pinning information

### 5.1 Pinning

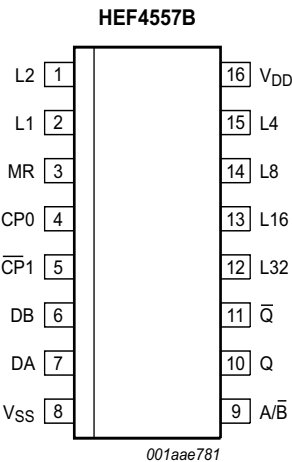


Fig 3. Pin configuration

### 5.2 Pin description

Table 2. Pin description table

Symbol	Pin	Description
L1, L2, L4, L8, L16, L32	2, 1, 15, 14, 13, 12	bit-length control input
MR	3	asynchronous master reset
CP0	4	clock input
CP1	5	clock input
DA, DB	7, 6	data input
V <sub>ss</sub>	8	ground (0 V)
A/ $\overline{B}$	9	select data input

Table 2. Pin description table ...continued

Symbol	Pin	Description
Q	10	buffered output
$\overline{Q}$	11	complementary buffered output
V <sub>DD</sub>	16	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs						Output
MR	A/ $\overline{B}$	DA	DB	CP0	CP1	Q
L	L	D <sub>1</sub>	D <sub>2</sub>	↑	L	D <sub>2</sub>
L	H	D <sub>1</sub>	D <sub>2</sub>	↑	L	D <sub>1</sub>
L	L	D <sub>1</sub>	D <sub>2</sub>	H	↓	D <sub>2</sub>
L	H	D <sub>1</sub>	D <sub>2</sub>	H	↓	D <sub>1</sub>
H	X	X	X	X	X	L

[1] The moment D<sub>n</sub> appears at Q depends on the bit-length shown in Table 4; H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition; D<sub>1</sub>, D<sub>2</sub> = either HIGH or LOW.

Table 4. Bit-length select function table

L32	L16	L8	L4	L2	L1	Register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
L1 to L16 continue to increment in a binary count with L32 LOW						
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
L1 to L16 continue to increment in a binary count with L32 HIGH						
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

## 7. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$I_{IO}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	SO16 package [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 7. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	50	-	50	-	375	$\mu\text{A}$
			10 V	-	100	-	100	-	750	$\mu\text{A}$
			15 V	-	200	-	200	-	1500	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CP0, $\overline{CP1}$ to Q, $\overline{Q}$ ; see <a href="#">Figure 4</a>	5 V <a href="#">[1]</a>	$213\text{ ns} + (0.55\text{ ns/pF})C_L$	-	240	480	ns
			10 V	$79\text{ ns} + (0.23\text{ ns/pF})C_L$	-	90	180	ns
			15 V	$57\text{ ns} + (0.16\text{ ns/pF})C_L$	-	65	130	ns
		MR to Q; see <a href="#">Figure 4</a>	5 V	$143\text{ ns} + (0.55\text{ ns/pF})C_L$	-	170	340	ns
			10 V	$69\text{ ns} + (0.23\text{ ns/pF})C_L$	-	80	160	ns
			15 V	$52\text{ ns} + (0.16\text{ ns/pF})C_L$	-	60	120	ns
$t_{PLH}$	LOW to HIGH propagation delay	CP0, $\overline{CP1}$ to Q, $\overline{Q}$ ; see <a href="#">Figure 4</a>	5 V <a href="#">[1]</a>	$213\text{ ns} + (0.55\text{ ns/pF})C_L$	-	240	480	ns
			10 V	$79\text{ ns} + (0.23\text{ ns/pF})C_L$	-	90	180	ns
			15 V	$57\text{ ns} + (0.16\text{ ns/pF})C_L$	-	65	130	ns
		MR to $\overline{Q}$ ; see <a href="#">Figure 4</a>	5 V	$113\text{ ns} + (0.55\text{ ns/pF})C_L$	-	140	280	ns
			10 V	$59\text{ ns} + (0.23\text{ ns/pF})C_L$	-	70	140	ns
			15 V	$47\text{ ns} + (0.16\text{ ns/pF})C_L$	-	55	110	ns
$t_t$	transition time	see <a href="#">Figure 4</a>	5 V <a href="#">[1]</a>	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{su}$	set-up time	DA, DB, $\overline{A/B}$ to CP0, $\overline{CP1}$ ; L1 to L32 = LOW; see <a href="#">Figure 5</a>	5 V <a href="#">[2]</a>		360	180	-	ns
			10 V		140	70	-	ns
			15 V		90	45	-	ns
		DA, DB, $\overline{A/B}$ to CP0, $\overline{CP1}$ ; L32 = HIGH; see <a href="#">Figure 5</a>	5 V		+40	-20	-	ns
			10 V		+35	-10	-	ns
			15 V		+30	-5	-	ns
$t_h$	hold time	DA, DB, $\overline{A/B}$ to CP0, $\overline{CP1}$ ; L1 to L32 = LOW; see <a href="#">Figure 5</a>	5 V <a href="#">[2]</a>		-40	-110	-	ns
			10 V		-10	-45	-	ns
			15 V		0	-30	-	ns
		DA, DB, $\overline{A/B}$ to CP0, $\overline{CP1}$ ; L1 to L32 = HIGH; see <a href="#">Figure 5</a>	5 V		90	30	-	ns
			10 V		60	20	-	ns
			15 V		50	15	-	ns
$t_w$	pulse width	CP0 input LOW; minimum width; see <a href="#">Figure 5</a>	5 V		180	90	-	ns
			10 V		60	30	-	ns
			15 V		40	20	-	ns
		$\overline{CP1}$ input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		180	90	-	ns
			10 V		60	30	-	ns
			15 V		40	20	-	ns
		MR input HIGH; minimum width; see <a href="#">Figure 5</a>	5 V		150	75	-	ns
			10 V		70	35	-	ns
			15 V		50	25	-	ns

**Table 8.** Dynamic characteristics ...continued

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{rec}$	recovery time	MR input; L1 to L32 = LOW; see <a href="#">Figure 5</a>	5 V <sup>[2]</sup>		500	250	-	ns
			10 V		250	125	-	ns
			15 V		150	75	-	ns
		MR input; L32 = HIGH	5 V		110	50	-	ns
			10 V		70	30	-	ns
			15 V		60	25	-	ns
$f_{max}$	maximum frequency	see <a href="#">Figure 5</a>	5 V		2.5	5	-	MHz
			10 V		7	14	-	MHz
			15 V		10	20	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

[2] The set-up, hold, and recovery times vary with the minimum number of bits selected. For intermediate numbers not specified, interpolate as shown in [Table 9](#).

**Table 9.** Interpolation table <sup>[1]</sup>

Length control inputs						Minimum number of bits selected	Set-up, hold, and recovery times	Example: $t_{rec}$ minimum, $V_{DD} = 5\text{ V}$
L1	L2	L4	L8	L16	L32			
L	L	L	L	L	L	1	see <a href="#">Table 8</a>	500 ns
H	L	L	L	L	L	2	(interpolate in 6 equal steps)	435 ns
X	H	L	L	L	L	3		370 ns
X	X	H	L	L	L	5		305 ns
X	X	X	H	L	L	9		240 ns
X	X	X	X	H	L	17		175 ns
X	X	X	X	X	H	33	see <a href="#">Table 8</a>	110 ns

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

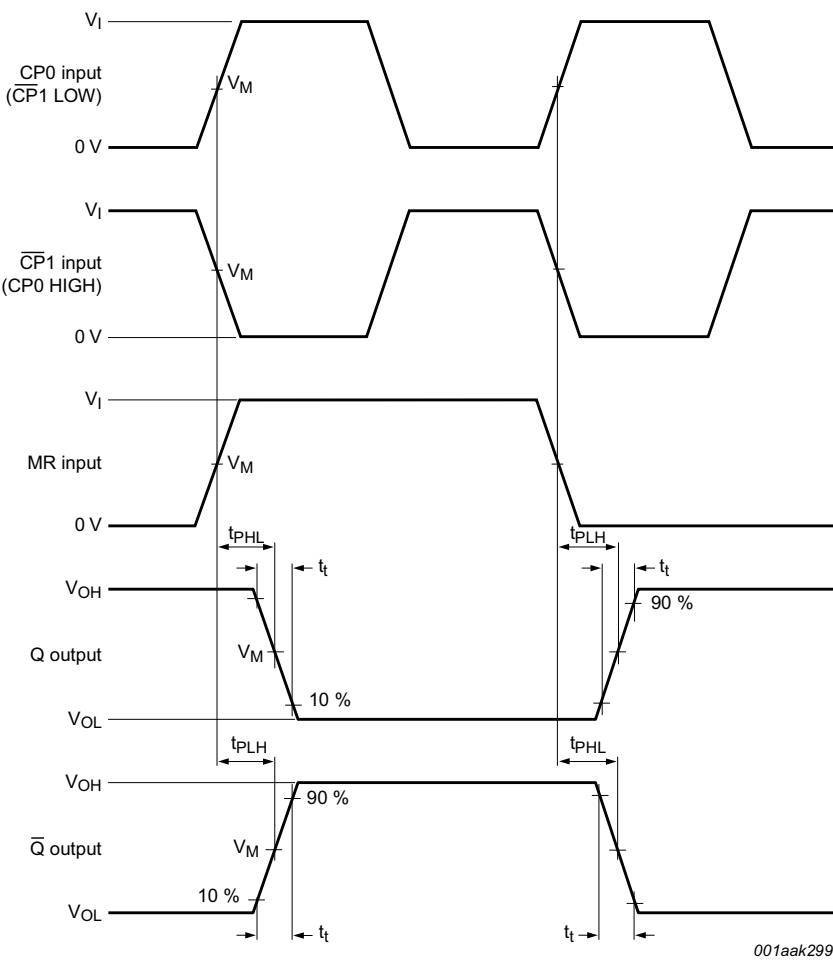
**Table 10.** Dynamic power dissipation  $P_D$ 

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 3500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 37000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

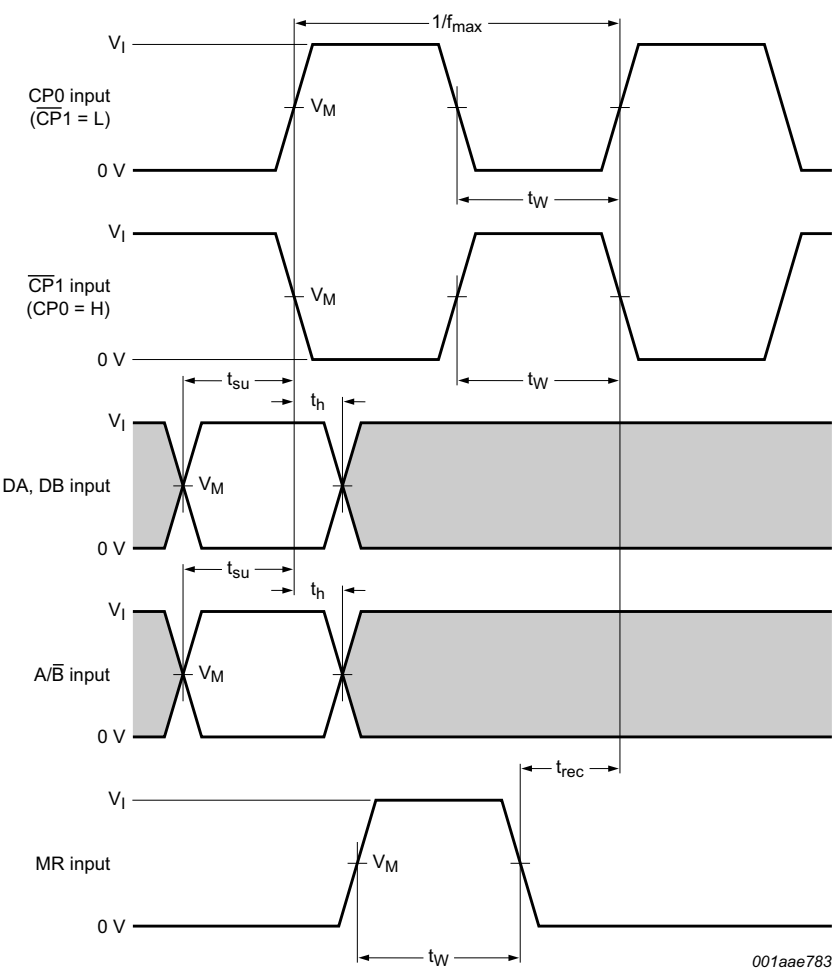


11. Waveforms



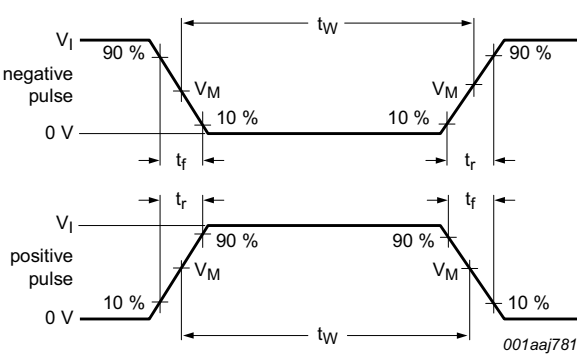
For measurement points see [Table 11](#).  
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 4. Propagation delays**

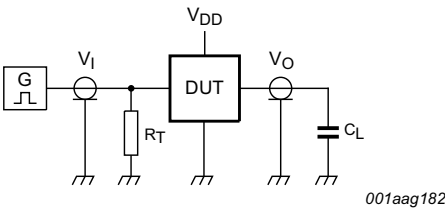


Set-up and hold times are shown as positive values but may be specified as negative values.  
The shaded area indicates where data can change for predictable performance.  
For measurement points see [Table 11](#).

**Fig 5.** Waveforms showing recovery time for MR and minimum CP0,  $\overline{CP1}$ , and MR pulse widths, set-up and hold times for DA, DB, and A/ $\overline{B}$  to CP0 and CP1



a. Input waveforms



b. Test circuit

Test data is given in [Table 11](#).

Definitions for test circuit:

Device Under Test (DUT)

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 6. Test circuit for measuring switching times

Table 11. Measurement points and test data

Supply voltage	Input			Load
$V_{DD}$	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

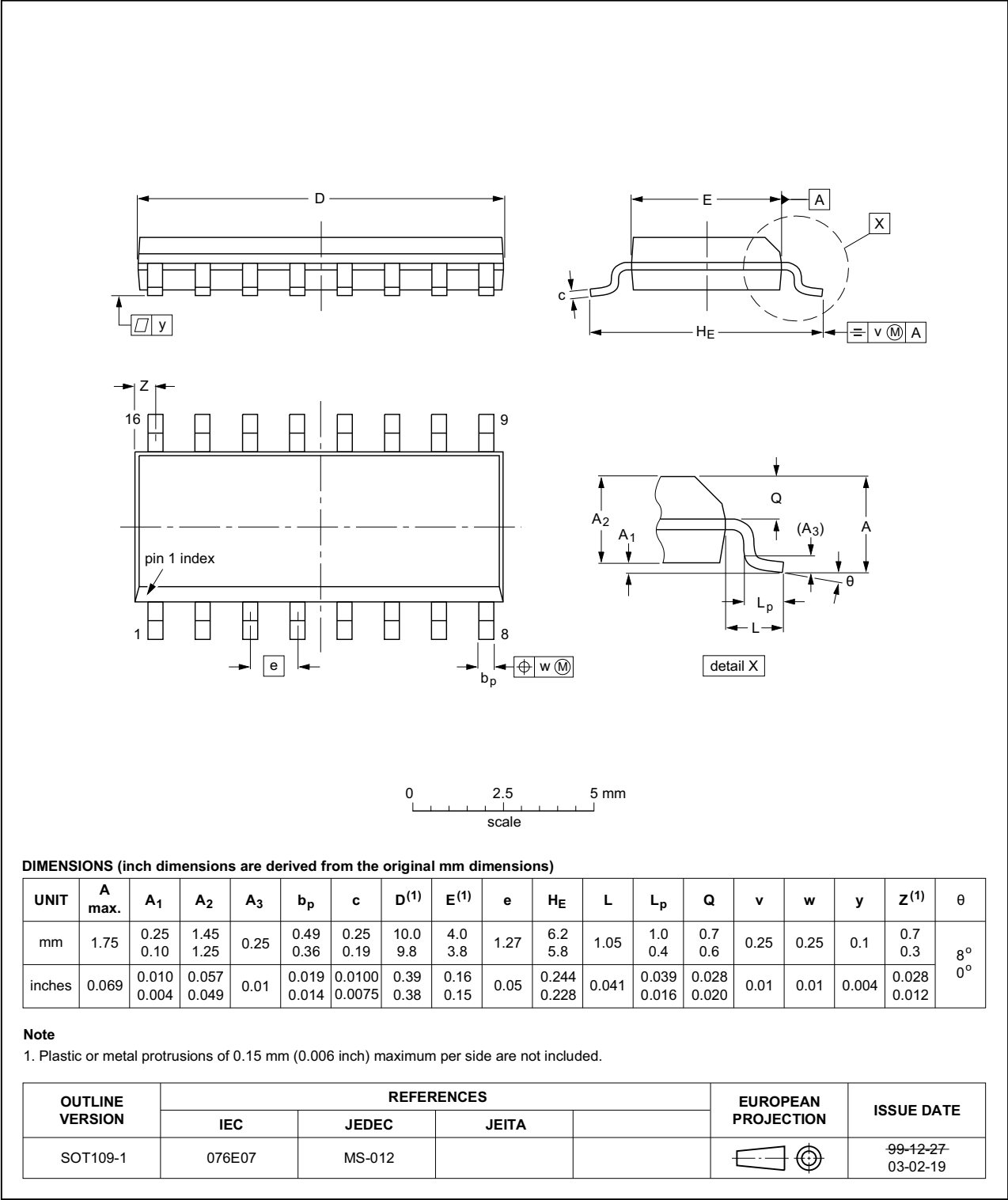


Fig 7. Package outline SOT109-1 (SO16)

## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4557B v.7	20160401	Product data sheet	-	HEF4557B v.6
Modifications:	<ul style="list-style-type: none"><li>Type number HEF4557BP (SOT38-4) removed.</li></ul>			
HEF4557B v.6	20111118	Product data sheet	-	HEF4557B v.5
Modifications:	<ul style="list-style-type: none"><li>Section Applications removed</li><li><a href="#">Table 7</a>: <math>I_{OH}</math> minimum values changed to maximum</li><li><a href="#">Figure 5</a>: "<math>\overline{A/B}</math> input" changed to "<math>A/\overline{B}</math> input"</li></ul>			
HEF4557B v.5	20091216	Product data sheet	-	HEF4557B v.4
HEF4557B v.4	20090916	Product data sheet	-	HEF4557B_CNV v.3
HEF4557B_CNV v.3	19950101	Product specification	-	HEF4557B_CNV v.2
HEF4557B_CNV v.2	19950101	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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