HEF4543B

BCD to 7-segment latch/decoder/driver

Rev. 9 — 15 August 2024 Product data sheet

1. General description

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. It has four address inputs (D0 to D3), an active LOW latch enable input ($\overline{LE}$), an active HIGH blanking input (BL), an active HIGH phase input (PH) and seven buffered segment outputs (Qa to Qg).

The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BL) and latch enable ($\overline{LE}$) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays, a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4543BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

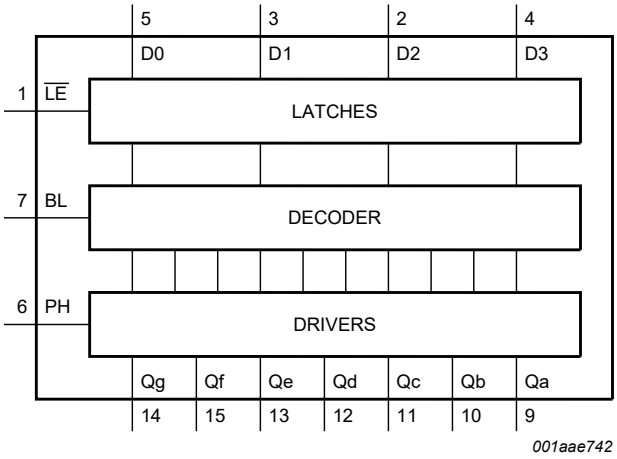


Fig. 1. Functional diagram

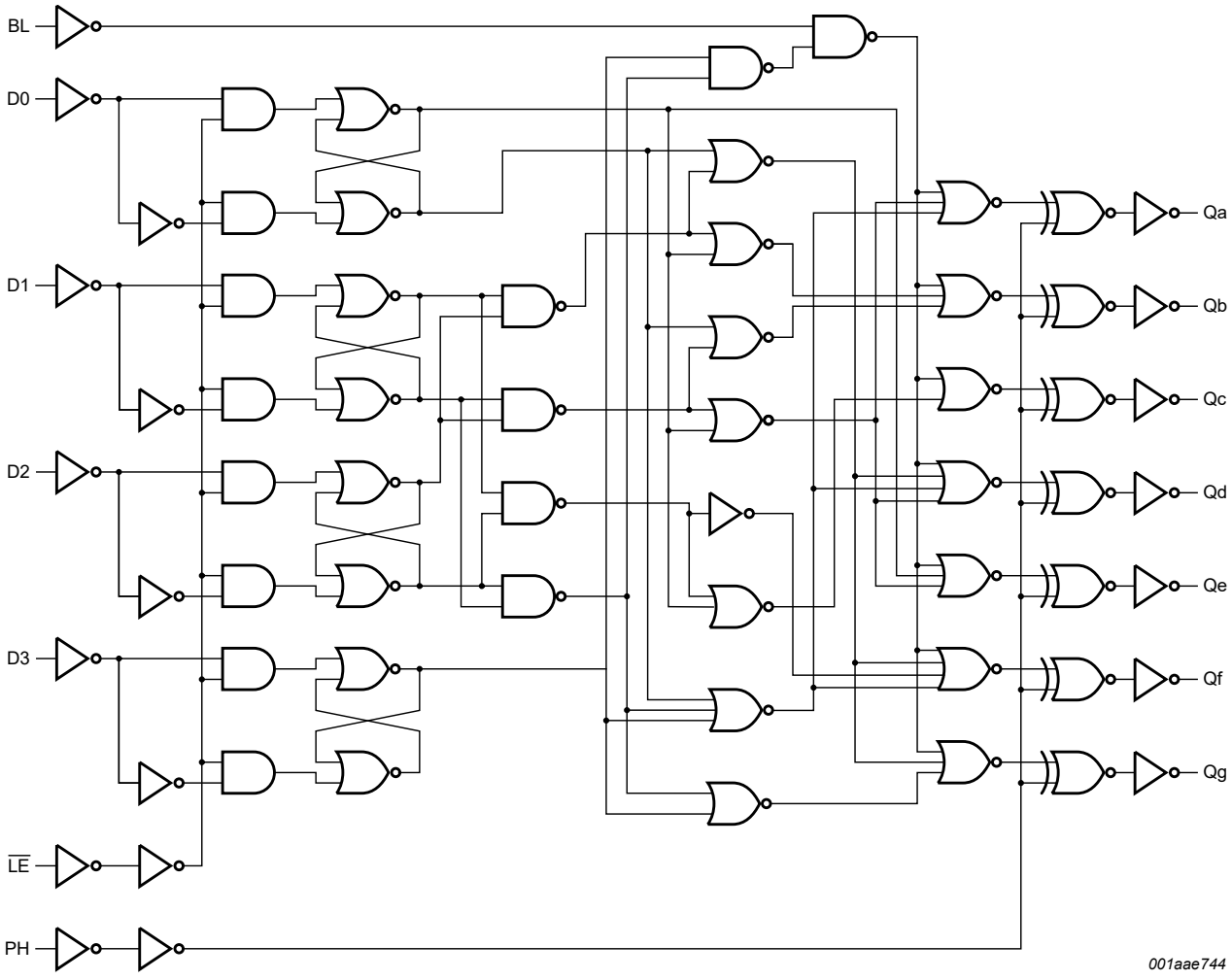
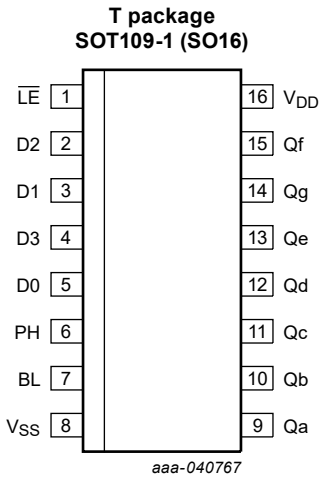


Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{LE}$	1	latch enable input (active LOW)
D0, D1, D2, D3	5, 3, 2, 4	address (data) input
PH	6	phase input (active HIGH)
BL	7	blanking input (active HIGH)
V_{SS}	8	ground supply voltage
Qa, Qb, Qc, Qd, Qe, Qf, Qg	9, 10, 11, 12, 13, 15, 14	segment output
V_{DD}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; n.c. = no change.

Inputs							Outputs							Display
$\overline{LE}$	BL	PH[1]	D3	D2	D1	D0	Qa	Qb	Qc	Qd	Qe	Qf	Qg	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	X	L	L	L	L	L	L	L	blank
H	L	L	H	H	X	X	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X	n.c.							n.c
as above		H	as above				inverse of above							as above

[1] For liquid crystal displays, apply a square-wave to PH;
For common cathode LED displays, select PH = LOW;
For common anode LED displays, select PH = HIGH.

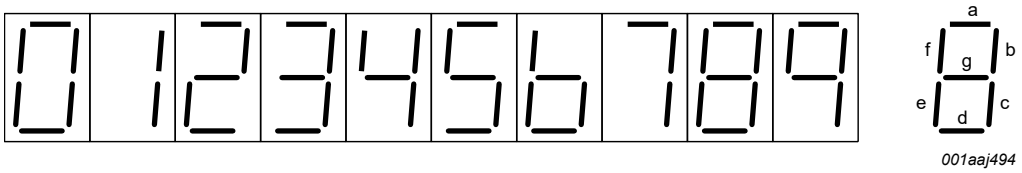


Fig. 3. Seven segment digital display with segment designation

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
V_I	input voltage		-0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current		-	±10	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation		-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; For test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	Dn to Qn; see Fig. 4	5 V	153 ns + (0.55 ns/pF)C_L	-	180	360	ns
			10 V	64 ns + (0.23 ns/pF)C_L	-	75	150	ns
			15 V	47 ns + (0.16 ns/pF)C_L	-	55	110	ns
		$\overline{LE}$ to Qn; see Fig. 4	5 V	143 ns + (0.55 ns/pF)C_L	-	170	340	ns
			10 V	69 ns + (0.23 ns/pF)C_L	-	80	160	ns
			15 V	52 ns + (0.16 ns/pF)C_L	-	60	120	ns
		BL to Qn; see Fig. 4	5 V	118 ns + (0.55 ns/pF)C_L	-	145	290	ns
			10 V	54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V	37 ns + (0.16 ns/pF)C_L	-	45	90	ns
t_{PLH}	LOW to HIGH propagation delay	Dn to Qn; see Fig. 4	5 V	153 ns + (0.55 ns/pF)C_L	-	180	360	ns
			10 V	64 ns + (0.23 ns/pF)C_L	-	75	150	ns
			15 V	47 ns + (0.16 ns/pF)C_L	-	55	110	ns
		$\overline{LE}$ to Qn; see Fig. 4	5 V	163 ns + (0.55 ns/pF)C_L	-	190	380	ns
			10 V	69 ns + (0.23 ns/pF)C_L	-	80	160	ns
			15 V	52 ns + (0.16 ns/pF)C_L	-	60	120	ns
		BL to Qn; see Fig. 4	5 V	98 ns + (0.55 ns/pF)C_L	-	125	250	ns
			10 V	54 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
t_t	transition time	pin Qn; see Fig. 4	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	Dn to $\overline{LE}$; see Fig. 5	5 V		40	20	-	ns
			10 V		20	5	-	ns
			15 V		15	0	-	ns
t_h	hold time	Dn to $\overline{LE}$; see Fig. 5	5 V		0	-15	-	ns
			10 V		15	0	-	ns
			15 V		20	5	-	ns
t_W	pulse width	pin $\overline{LE}$ HIGH; minimum width; see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns

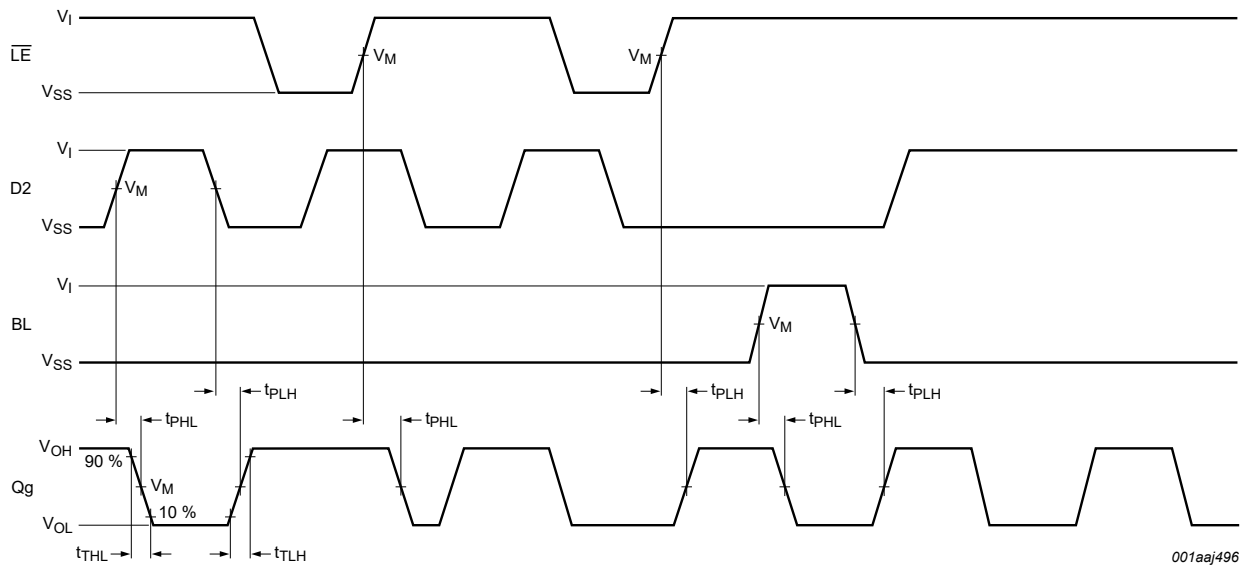
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

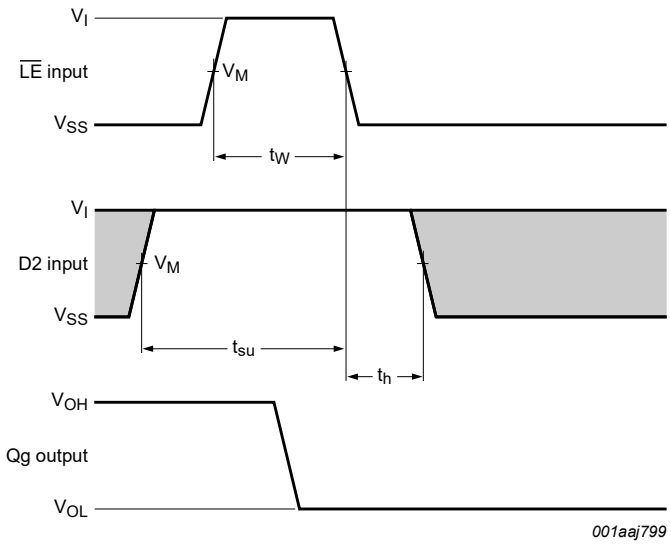
Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 10400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 33000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

10.1. Waveforms and test circuit



Conditions: D3 = LOW and D0 = D1 = HIGH.

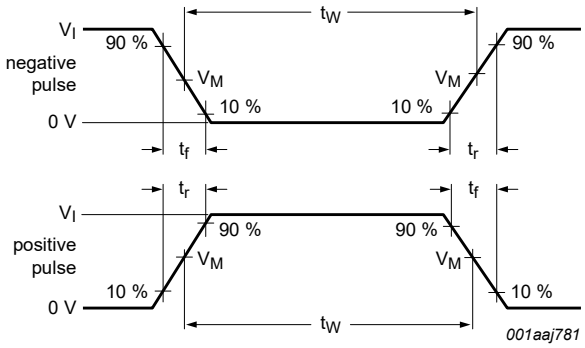
Fig. 4. Propagation delays and output transitions times



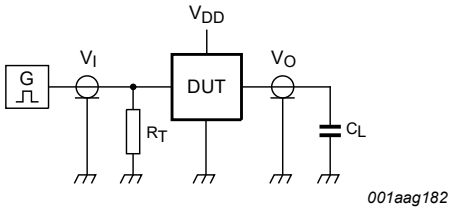
Conditions:

D3 = BL = LOW; D0 = D1 = $\overline{LE}$ = HIGH

Fig. 5. Waveforms showing minimum $\overline{LE}$ pulse width, set-up, and hold time for DC to $\overline{LE}$



a. Input waveforms



b. Test circuit

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

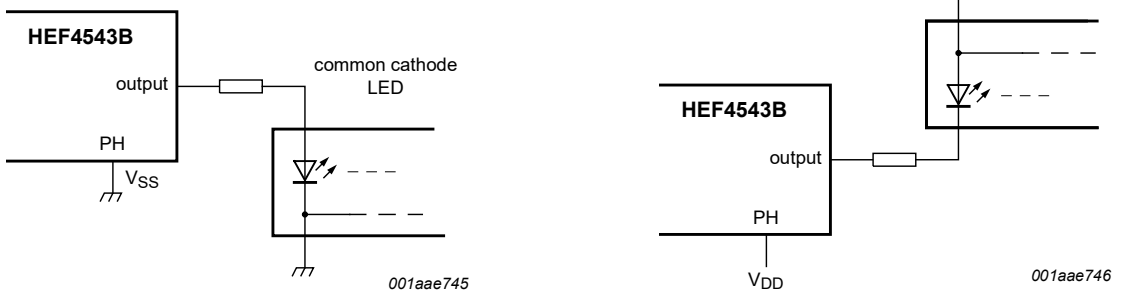
Table 9. Test data

Supply voltage	Input			Load
V_{DD}	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

11. Application information

Some examples of applications for the HEF4543B are:

- Driving LCD displays
- Driving LED displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays



a. Common cathode

b. Common anode

Bipolar transistors may be added for gain where $V_{DD} \leq 10$ V or $I_O \geq 10$ mA.

Fig. 7. Connection to LED display readout

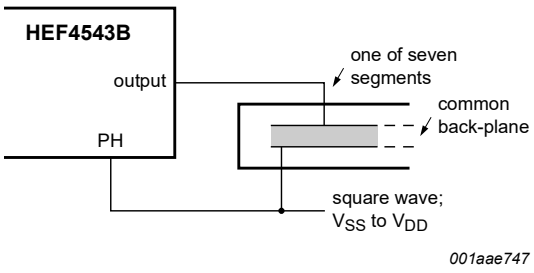


Fig. 8. Connection to LCD readout

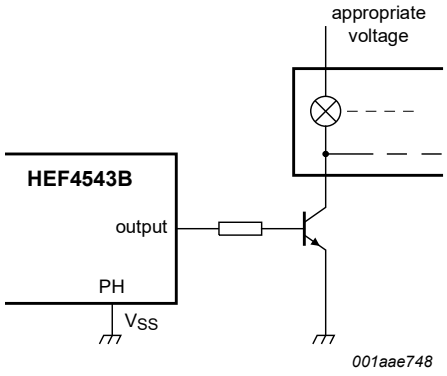


Fig. 9. Connection to incandescent display readout

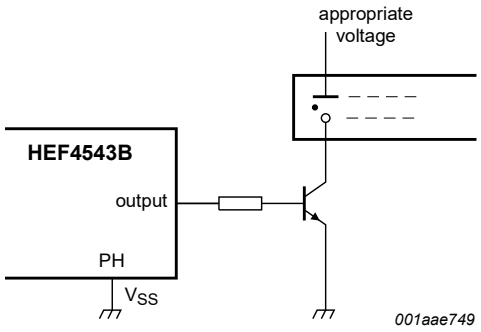


Fig. 10. Connection to gas discharge display readout

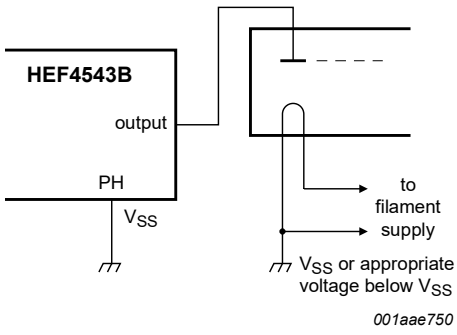
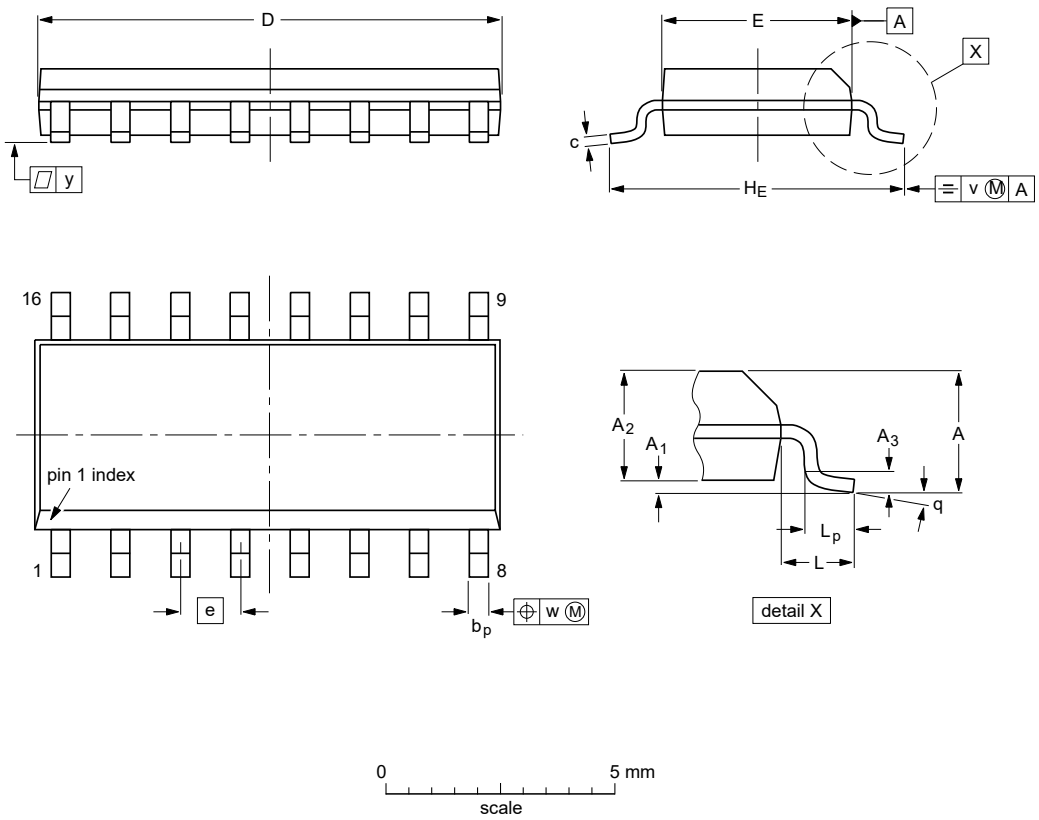


Fig. 11. Connection to fluorescent display readout

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 12. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
LCD	Liquid Crystal Display
LED	Light Emitting Diode

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4543B v.9	20240815	Product data sheet	-	HEF4543B v.8
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 12: Aligned SO package outline drawing to JEDEC MS-012			
HEF4543B v.8	20211124	Product data sheet	-	HEF4543B v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 6: V_{OH} condition added (errata).			
HEF4543B v.7	20160401	Product data sheet	-	HEF4543B v.6
Modifications:	• Type number HEF4543BP (SOT38-4) removed.			
HEF4543B v.6	20111117	Product data sheet	-	HEF4543B v.5
Modifications:	• Section Applications removed • Table 6: I_{OH} minimum values changed to maximum • Fig. 5: signal $\overline{LT}$ removed; signal $\overline{BL}$ replaced by BL (inverted)			
HEF4543B v.5	20091027	Product data sheet	-	HEF4543B v.4
HEF4543B v.4	20090317	Product data sheet	-	HEF4543B_CNV v.3
HEF4543B_CNV v.3	19950101	Product specification	-	HEF4543B_CNV v.2
HEF4543B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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