

HEF4047B-Q100

Monostable/astable multivibrator

Rev. 2 — 3 September 2024

Product data sheet

1. General description

The HEF4047B-Q100 is a retriggerable astable multivibrator that can be configured as either a positive-edge or negative-edge triggered monostable multivibrator. The output pulse width is programmed by selection of external components (R_t and C_t). Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

General

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external resistor and capacitor required
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

Monostable multivibrator

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components with external counter provision
- Fast recovery time independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

Astable multivibrator

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4047BT-Q100	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

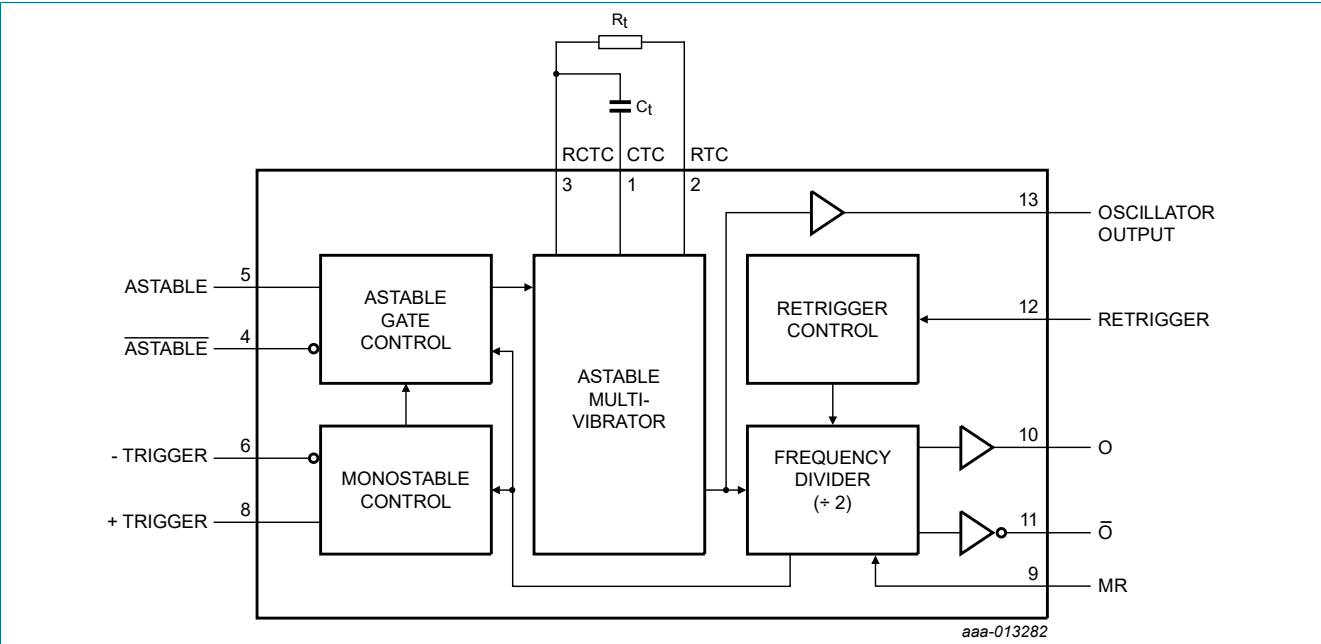
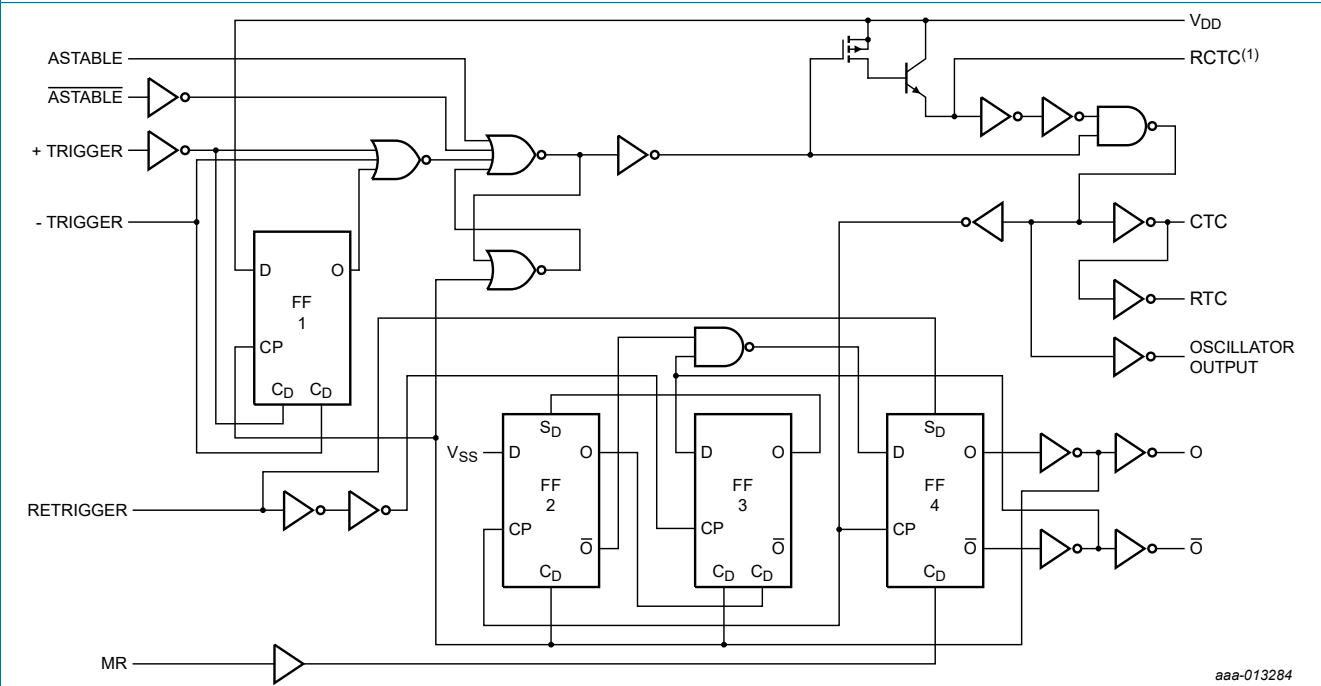


Fig. 1. Functional diagram

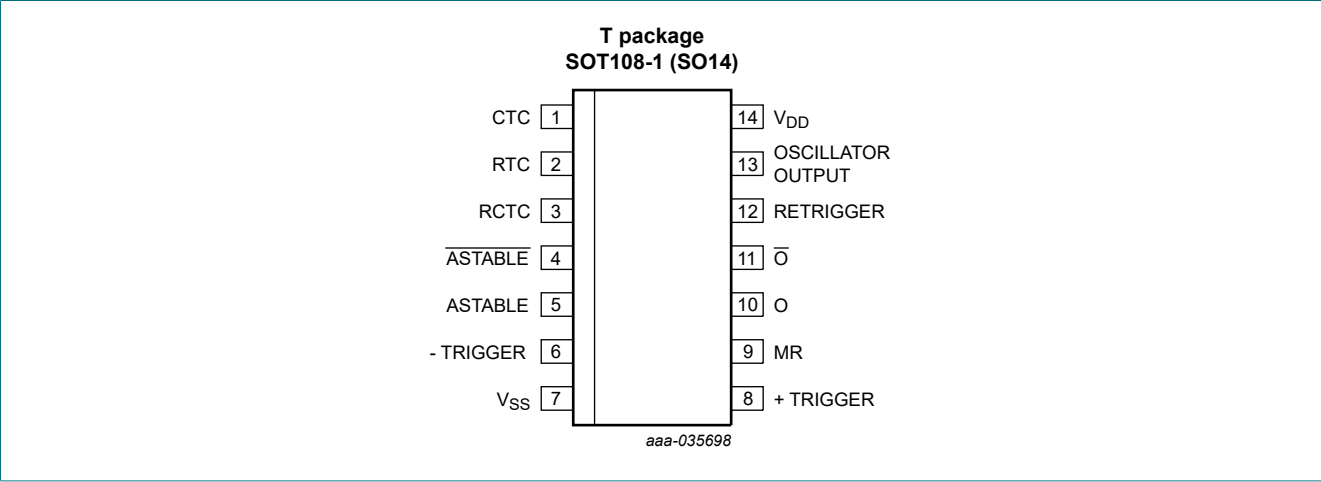


(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard inputprotection pin 3 (RCTC) is more sensitive to static discharge; extra handling precautions are recommended.

Fig. 2. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
CTC	1	external capacitor connection
RTC	2	external resistor connection
RCTC	3	external capacitor/resistor connection
ASTABLE	4	input
ASTABLE	5	input
-TRIGGER	6	input
V _{SS}	7	ground supply voltage
+TRIGGER	8	input
MR	9	master reset input
O	10	output
$\bar{O}$	11	output
RETRIGGER	12	input
OSCILLATOR OUTPUT	13	oscillator output
V _{DD}	14	supply voltage

6. Functional description

The HEF4047B-Q100 consists of a gate-able astable multivibrator incorporating logic techniques to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (master reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between CTC and RCTC, and an external resistor (R_t) must be connected between RTC and RCTC.

A HIGH level on the ASTABLE input enables astable operation. The period of the square wave at O and $\overline{\text{O}}$ outputs is a function of the external components employed. 'True' input pulses on the ASTABLE or 'complement' pulses on the $\overline{\text{ASTABLE}}$ input, allow the circuit to be used as a gate-able multivibrator. The OSCILLATOR OUTPUT period is half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the +TRIGGER input and a LOW level to the -TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the -TRIGGER and a HIGH level to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode, the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option implements coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

7. Limiting values

Table 3. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{DD} + 0.5 \text{ V}$	-	± 10	mA
$I_{I/O}$	input/output current		-	± 10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C to } +85 \text{ °C}$	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		3	15	V
V _I	input voltage		0	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	3.75	μs/V
		V _{DD} = 10 V	-	0.5	μs/V
		V _{DD} = 15 V	-	0.08	μs/V

9. Static characteristics

Table 5. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} = -40 °C		T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
		output transistor OFF; pin 3 at V _{DD} or V _{SS}	15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 6. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified; for waveform and test circuit, see [Fig. 3](#) and [Fig. 4](#).

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to OSCILLATOR OUTPUT	5 V [1]	$68\text{ ns} + (0.55\text{ ns/pF})C_L$	-	95	190	ns
			10 V [1]	$43\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V [1]	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t _{PLH}	LOW to HIGH propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to OSCILLATOR OUTPUT	5 V [1]	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	170	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t _{PHL}	HIGH to LOW propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to O, $\overline{\text{O}}$	5 V [1]	$123\text{ ns} + (0.55\text{ ns/pF})C_L$	-	150	300	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t _{PLH}	LOW to HIGH propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to O, $\overline{\text{O}}$	5 V [1]	$103\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
t _{PHL}	HIGH to LOW propagation delay	+/-TRIGGER to O, $\overline{\text{O}}$	5 V [1]	$133\text{ ns} + (0.55\text{ ns/pF})C_L$	-	160	320	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t _{PLH}	LOW to HIGH propagation delay	+/-TRIGGER to O, $\overline{\text{O}}$	5 V [1]	$128\text{ ns} + (0.55\text{ ns/pF})C_L$	-	155	310	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t _{PHL}	HIGH to LOW propagation delay	+TRIGGER, RETRIGGER to $\overline{\text{O}}$	5 V [1]	$38\text{ ns} + (0.55\text{ ns/pF})C_L$	-	65	130	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
t _{PLH}	LOW to HIGH propagation delay	+TRIGGER, RETRIGGER to O	5 V [1]	$68\text{ ns} + (0.55\text{ ns/pF})C_L$	-	95	190	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t _{PHL}	HIGH to LOW propagation delay	MR to O	5 V [1]	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	100	200	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t _{PLH}	LOW to HIGH propagation delay	MR to $\overline{\text{O}}$	5 V [1]	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	100	200	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t _{THL}	HIGH to LOW output transition time		5 V [1]	$10\text{ ns} + (1.0\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time		5 V [1]	$10\text{ ns} + (1.0\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _W	pulse width	any input except MR	5 V	-	220	110	-	ns
			10 V	-	100	50	-	ns
			15 V	-	70	35	-	ns
		MR HIGH	5 V	-	60	30	-	ns
			10 V	-	30	15	-	ns
			15 V	-	20	10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

10.1. Waveform and test circuit

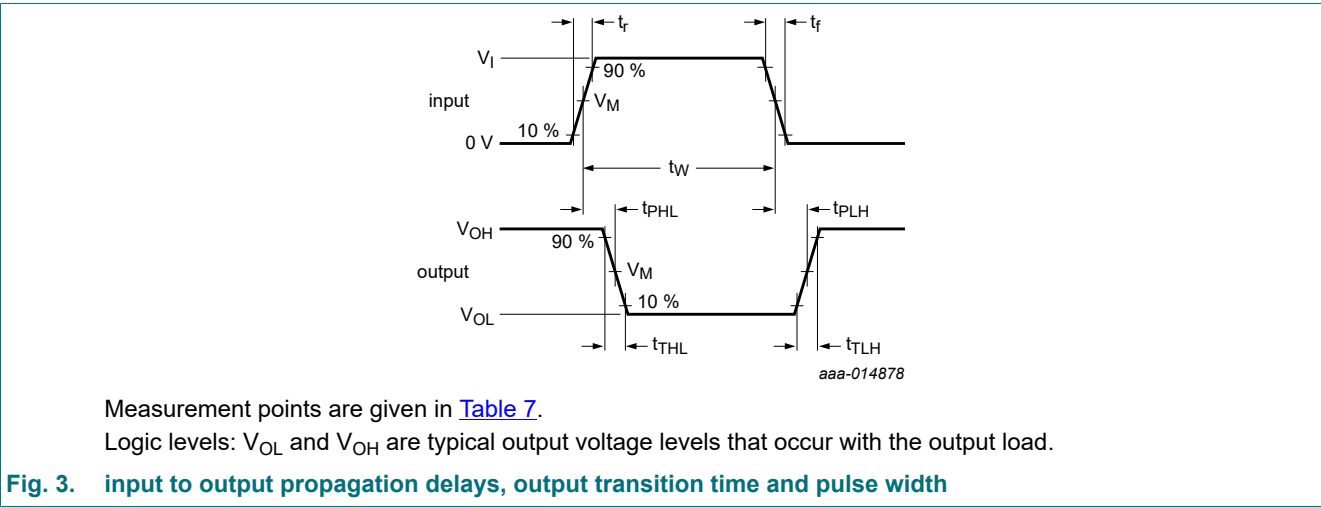


Table 7. Measurement points

Supply voltage	Input	Output
V _{DD}	V _M	V _M
5 V to 15 V	0.5 × V _{DD}	0.5 × V _{DD}

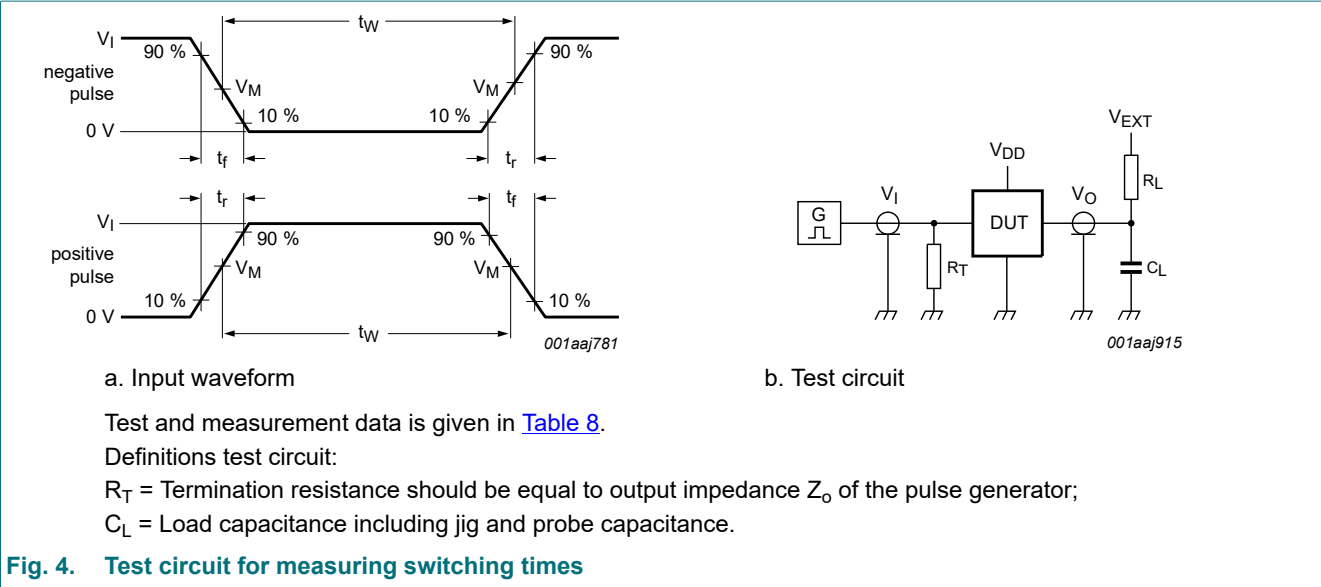


Table 8. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 k Ω	open

11. Application information

Table 9. Functional connections

In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

Function	Pins connected to			Output pulse from pins	Output period or pulse width
	V _{DD}	V _{SS}	input pulse		
Astable multivibrator					
Free running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	at pins 10, 11; t _A = 4.40 R _t C _t at pin 13; t _A = 2.20 R _t C _t
True gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	
Complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable multivibrator					
Positive edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	at pins 10, 11; t _M = 2.48 R _t C _t
Negative edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External countdown [1]	14	5, 6, 7, 8, 9, 12	-	10, 11	

[1] Input pulse to RESET of external counting chip: external counting chip output to pin 4.

11.1. Astable mode design information

11.1.1. Unit-to-unit transfer voltage variations

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage (V_{TR}) shift for free running (astable) operation.

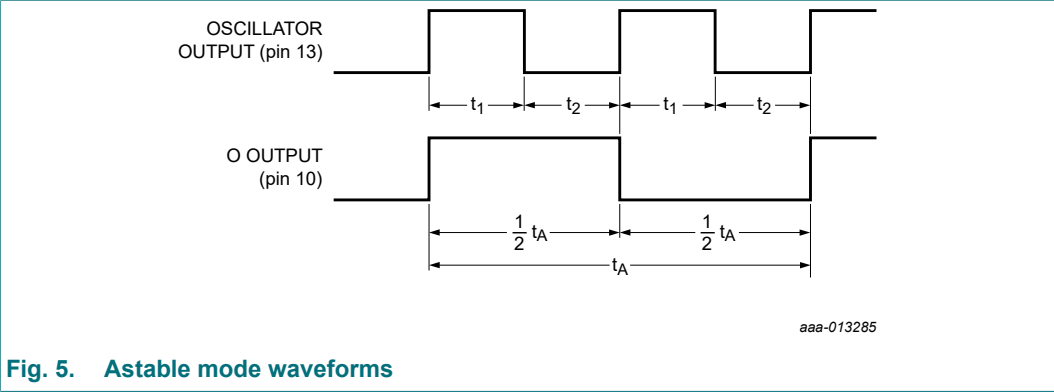


Fig. 5. Astable mode waveforms

(1)
$$t_1 = -R_t C_t \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

(2)
$$t_2 = -R_t C_t \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

(3)
$$t_A = 2 (t_1 + t_2) = -2R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

, where t_A = astable mode pulse width; see [Table 10](#).

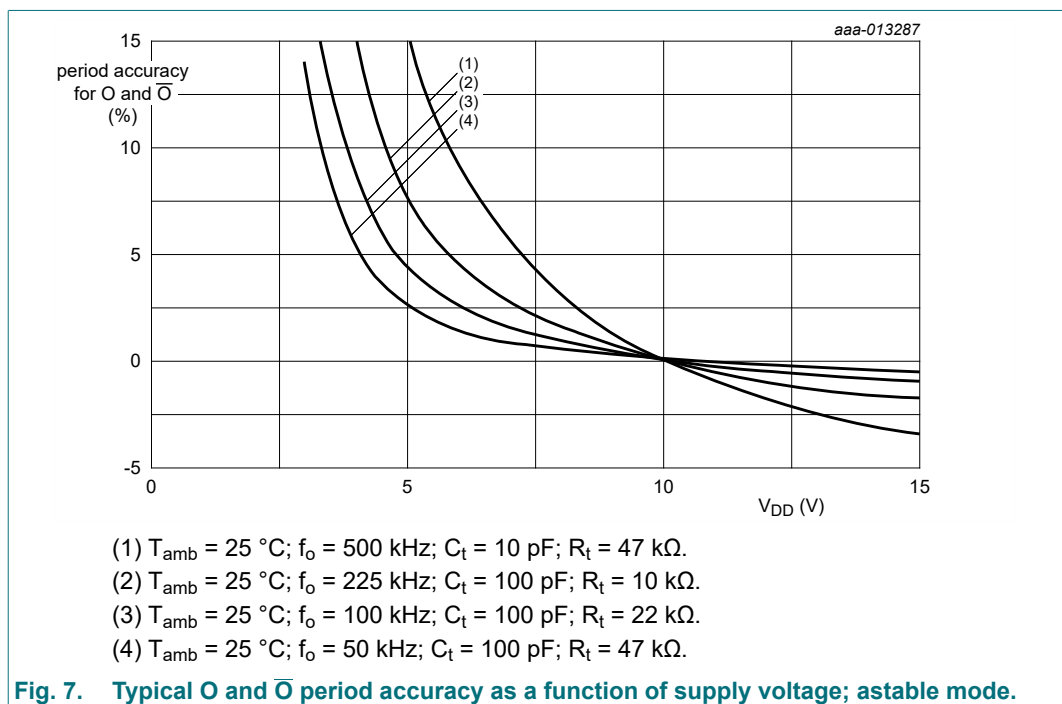
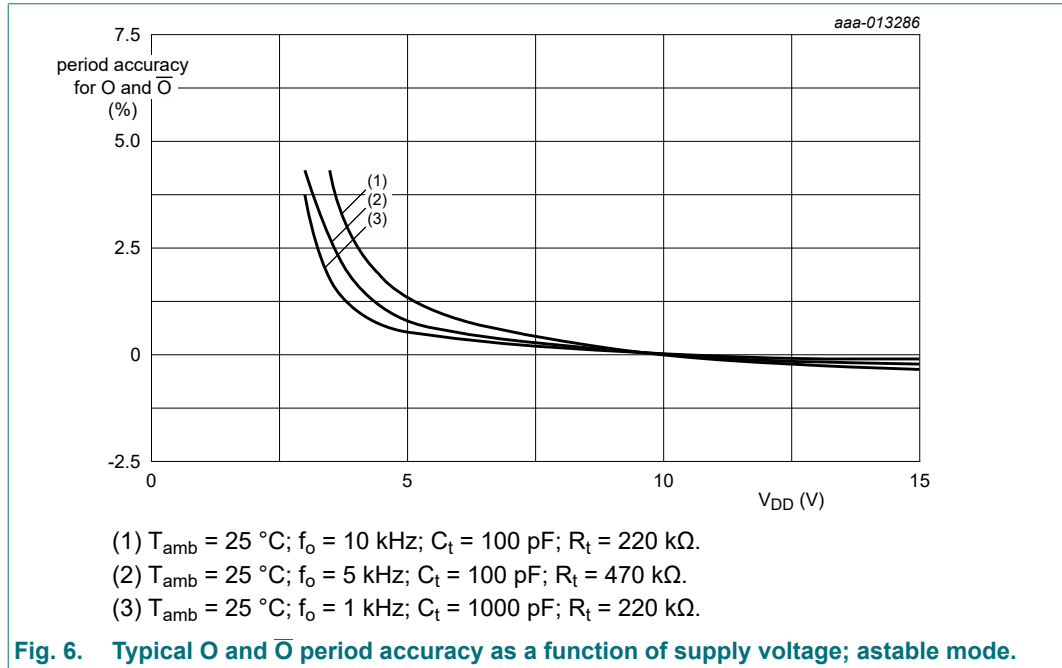
Table 10. Values for astable mode pulse width (t_A)

	V_{TR}			t_A		
	Min	Typ	Max	Min	Typ [1]	Max
$V_{DD} = 5 \text{ V or } 10 \text{ V}$	$0.3 \times V_{DD}$	$0.5 \times V_{DD}$	$0.7 \times V_{DD}$	$4.71 R_t C_t$	$4.40 R_t C_t$	$4.71 R_t C_t$
$V_{DD} = 15 \text{ V}$	4 V	$0.5 \times V_{DD}$	11 V	$4.84 R_t C_t$	$4.40 R_t C_t$	$4.84 R_t C_t$

[1] Therefore if $t_A = 4.40 R_t C_t$ is used, the maximum variation is (+7.0%; -0.0%) at 10 V.

11.1.2. Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} . Typical variations are presented graphically in Fig. 6 and Fig. 7 with 10 V as a reference.



11.2. Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage (V_{TR}) shift for one-shot (monostable) operation.

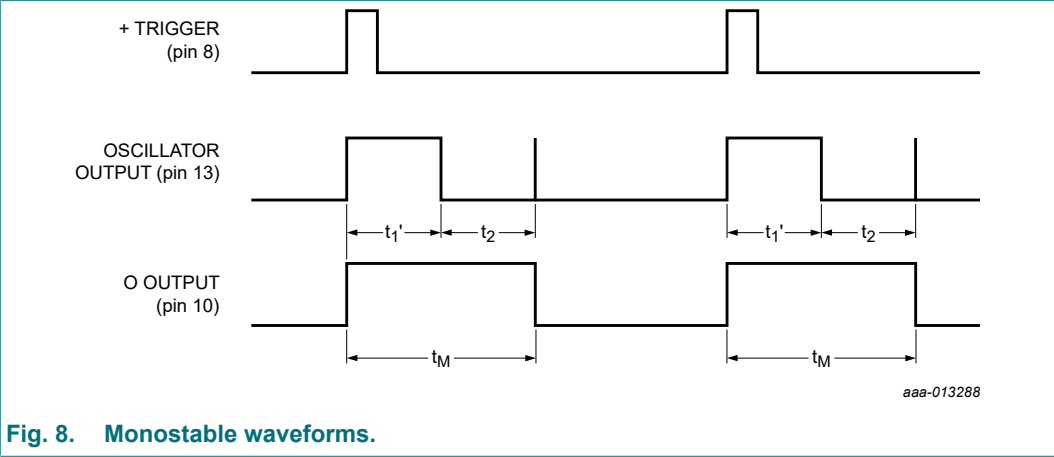


Fig. 8. Monostable waveforms.

(4)
$$t_1' = -R_t C_t \ln \frac{V_{TR}}{2V_{DD}}$$

(5)
$$t_M = (t_1' + t_2)$$

(6)
$$t_M = -R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

, where t_M = monostable mode pulse width; see table [Table 11](#).

Table 11. Values for monostable mode pulse width (t_M)

	V_{TR}			t_M		
	Min	Typ	Max	Min	Typ [1]	Max
$V_{DD} = 5\text{ V or }10\text{ V}$	$0.3 \times V_{DD}$	$0.5 \times V_{DD}$	$0.7 \times V_{DD}$	$2.78 R_t C_t$	$2.48 R_t C_t$	$2.52 R_t C_t$
$V_{DD} = 15\text{ V}$	4 V	$0.5 \times V_{DD}$	11 V	$2.88 R_t C_t$	$2.48 R_t C_t$	$2.56 R_t C_t$

[1] In the astable mode, the first positive half cycle has a duration of t_M ; succeeding durations are $\frac{1}{2} t_A$. Therefore if $t_M = 2.48 R_t C_t$ is used, the maximum variation is (+12%; -0.0%) at 10 V.

11.2.1. Retrigger mode operation

The HEF4047B-Q100 can be used in the retrigger mode to extend the output pulse duration. It can also be used to compare the frequency of an input signal with the frequency of the internal oscillator. In the retrigger mode, the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (see Fig. 9). Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (output O), terminates at some variable time, t_D , after the termination of the last retrigger pulse. t_D is variable because t_{RE} (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

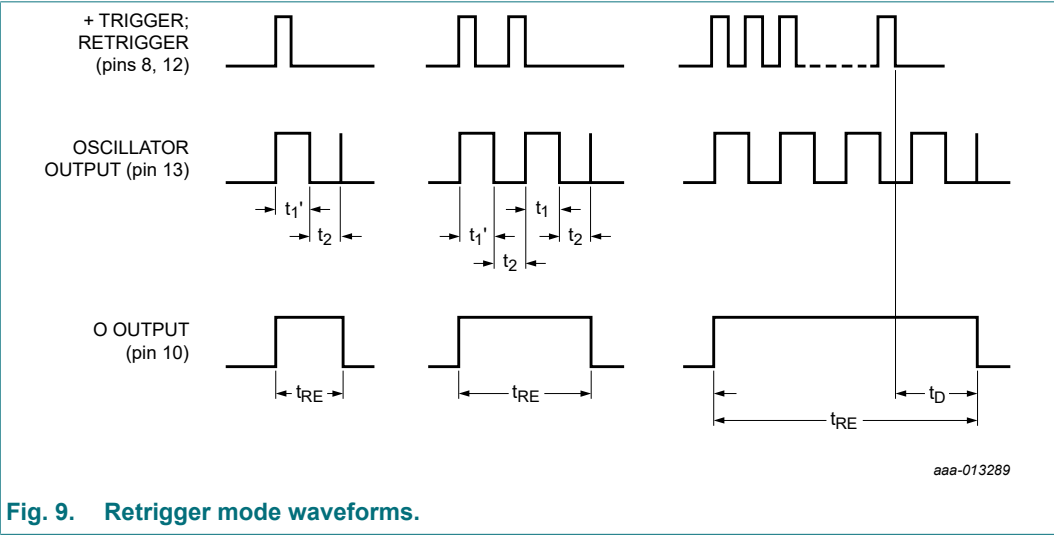


Fig. 9. Retrigger mode waveforms.

11.2.2. External counter option

The use of external counting circuitry extends time t_M by any amount. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 10.

The pulse duration at the output is:

(7)
$$t_{ext} = (N - 1)(t_A) + (t_M + 1/2 t_A)$$

, where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

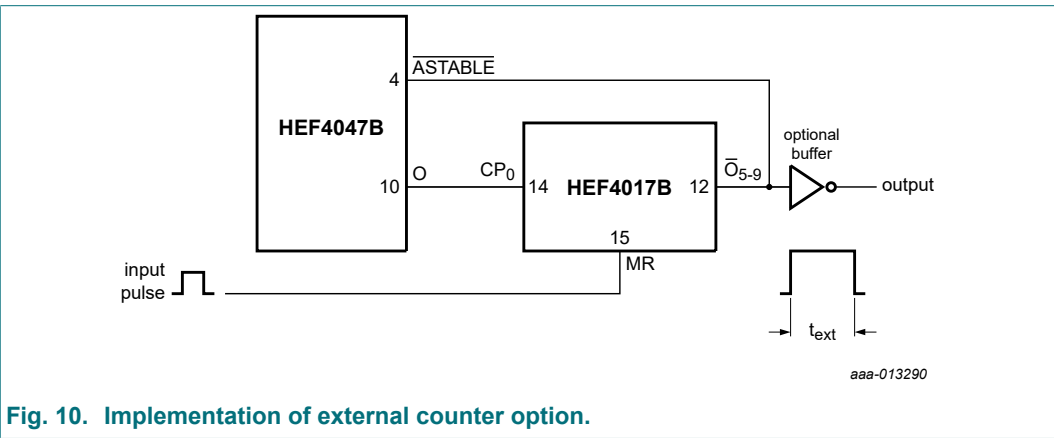


Fig. 10. Implementation of external counter option.

11.2.3. Timing component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (that is the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R_t or C_t value to maintain oscillation. However, for accuracy, C_t must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R_t must be much larger than the LOCMOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for R_t and C_t to comply with previously calculated formulae without trimming should be:

- $C_t \geq 100$ pF, up to any practical value
- $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$

11.2.4. Power consumption

In the standby mode (monostable or astable), power dissipation is a function of leakage current in the circuit. For dynamic operation, the power required to charge the external timing capacitor C_t is shown in the following formulae:

Astable mode:

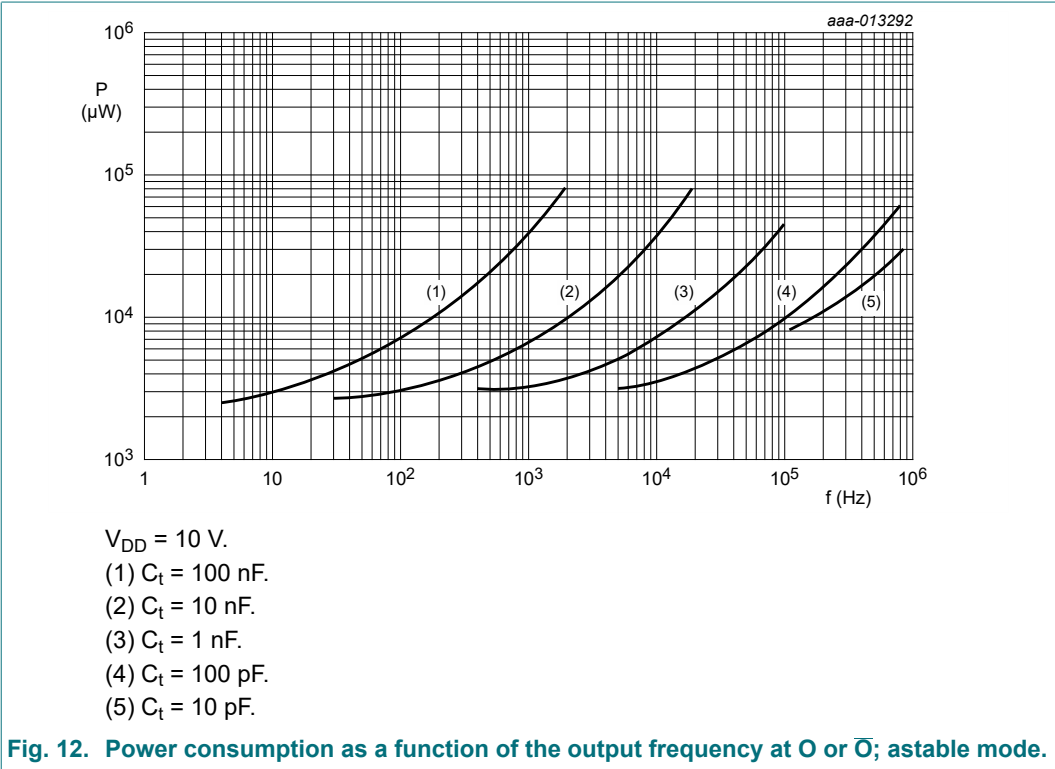
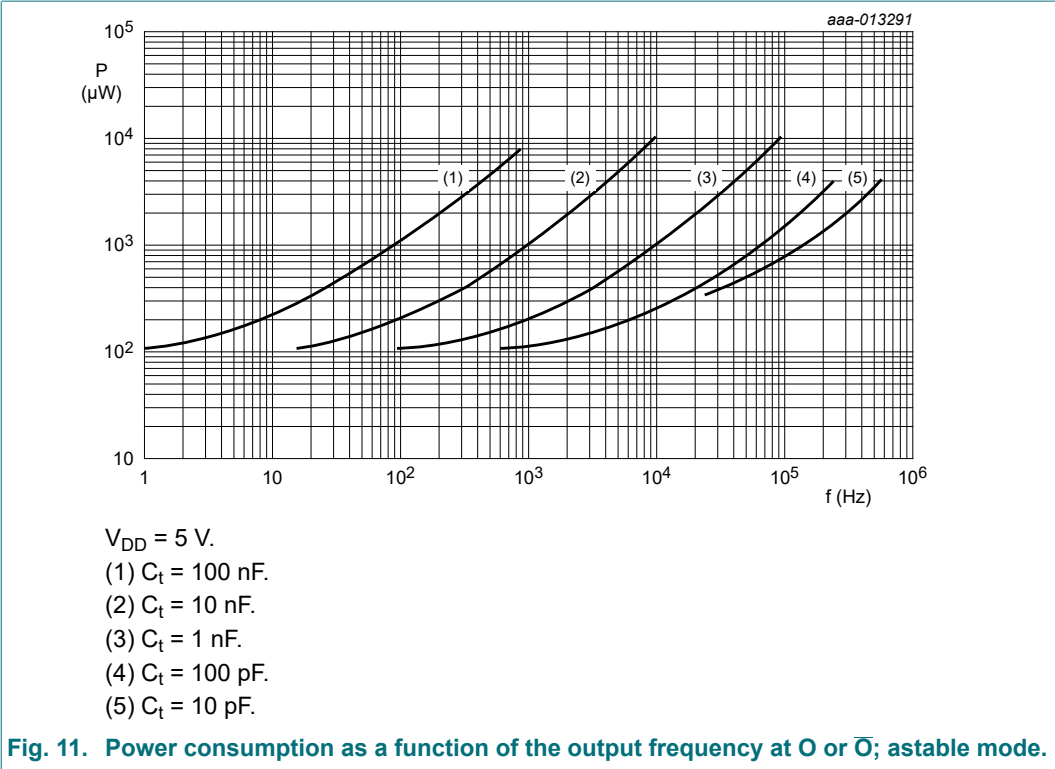
$$(8) \quad P = 2C_t V^2 f \quad (f \text{ at output pin 13})$$

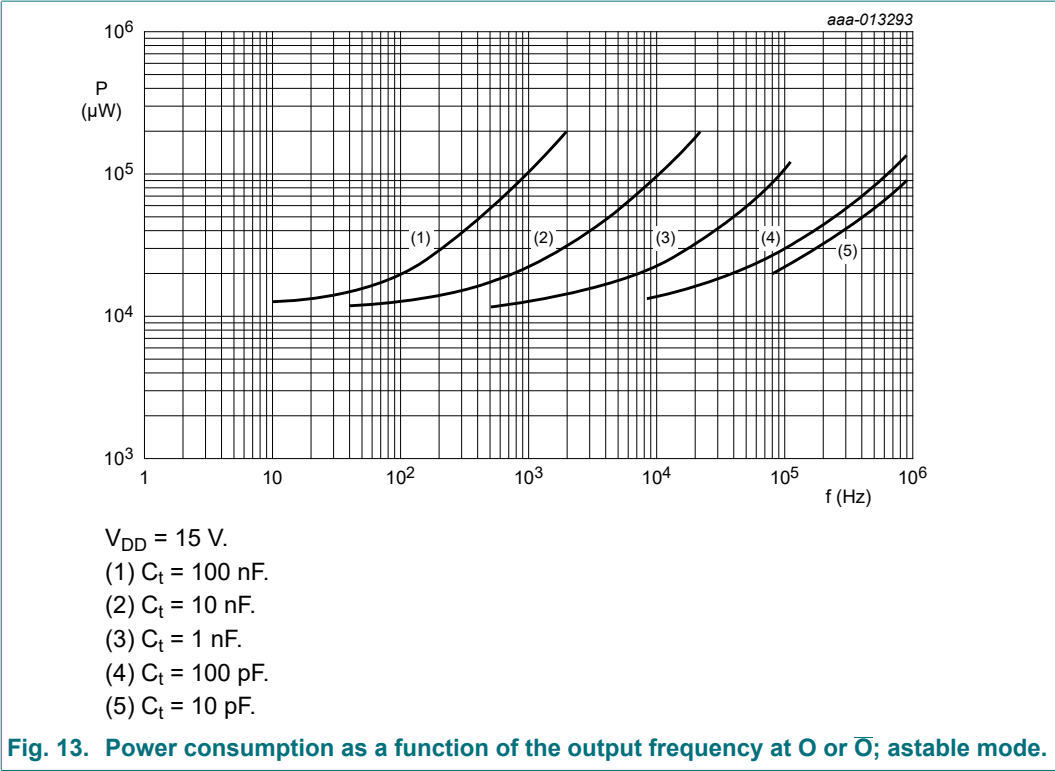
$$(9) \quad P = 4C_t V^2 f \quad (f \text{ at outputs pin 10 and 11})$$

Monostable mode:

$$(10) \quad P = \frac{(2.9C_t V^2)(duty \ cycle)}{T} \quad (f \text{ at outputs pin 10 and 11})$$

Because the power dissipation does not depend on R_t , a design for minimum power dissipation would be a small value of C_t . The value of R would depend on the desired period (within the limitations discussed previously). Typical power consumption in astable mode is shown in [Fig. 11](#), [Fig. 12](#) and [Fig. 13](#).





12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

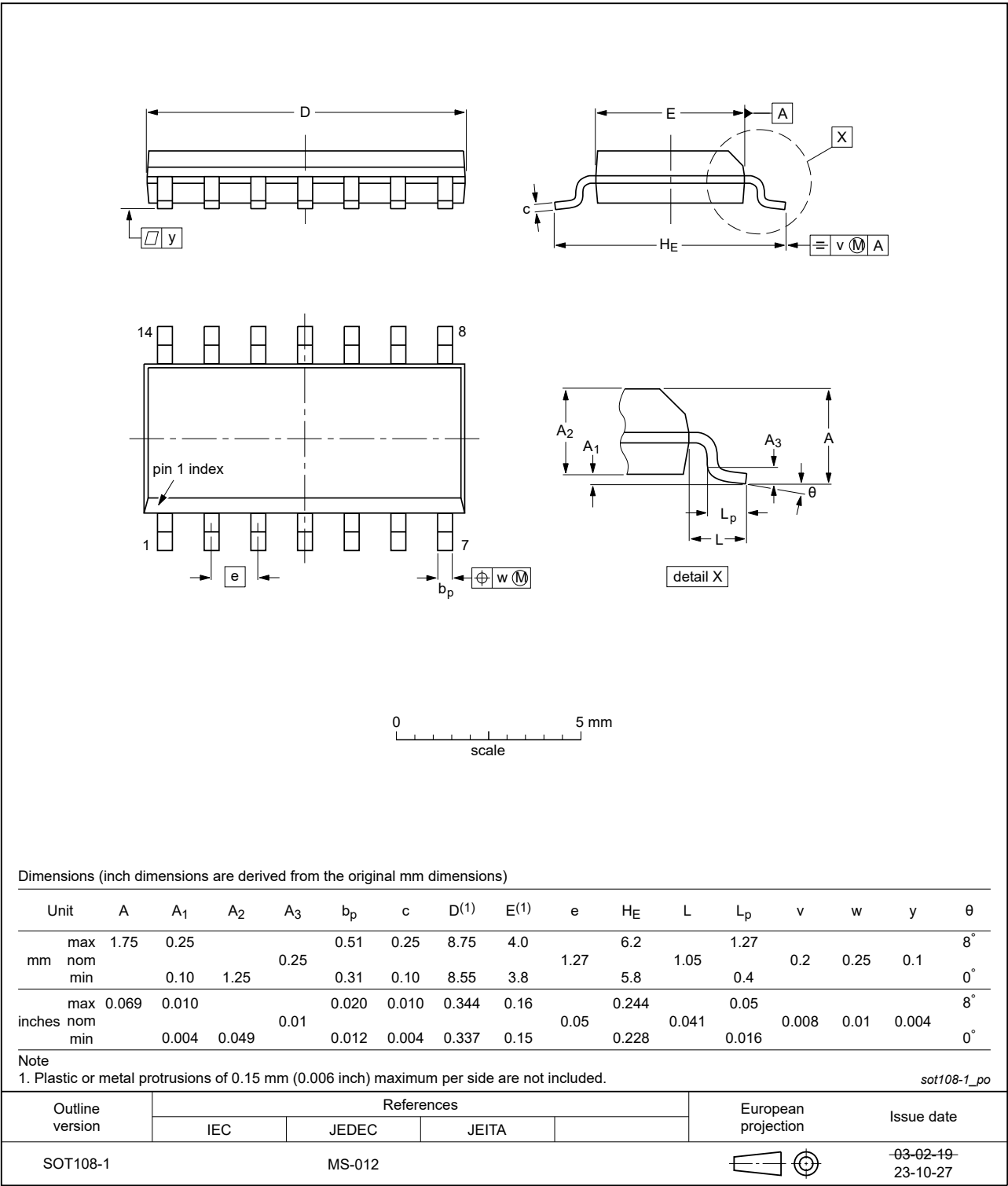


Fig. 14. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4047B_Q100 v.2	20240903	Product data sheet	-	HEF4047B_Q100 v.1
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard. Fig. 14: Aligned SO package outline drawing to JEDEC MS-012			
HEF4047B_Q100 v.1	20170317	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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