



GAN111-650WSB

650 V, 97 mOhm Gallium Nitride (GaN) FET in a TO-247 package

24 June 2024

Product data sheet

1. General description

The GAN111-650WSB is a 650 V, 97 mΩ Gallium Nitride (GaN) FET in a TO-247 package. It is a normally-off device that combines Nexperia's latest high-voltage GaN HEMT H2 technology and low-voltage silicon MOSFET technologies — offering superior reliability and performance.

2. Features and benefits

- Ultra-low reverse recovery charge
- Simple gate drive (0 V to +10 V or +12 V)
- Robust gate oxide (± 20 V capability)
- High gate threshold voltage (+4 V) for very good gate bounce immunity
- Very low source-drain voltage in reverse conduction mode
- Transient over-voltage capability

3. Applications

- Hard and soft switching converters for industrial and datacom power
- AC/DC Bridgeless totem-pole PFC
- DC/DC High-frequency resonant converters
- Datacom and telecom (AC/DC and DC/DC) converters
- Solar (PV) inverters
- Servo motor drives
- TV PSU and LED drivers

4. Quick reference data

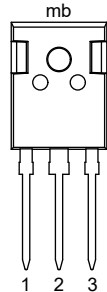
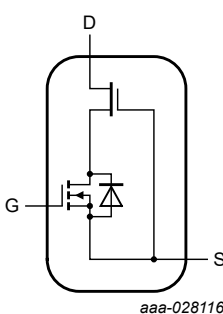
Table 1. Quick reference data

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	-55 °C ≤ T _j ≤ 175 °C		-	-	650	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	21	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	107	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 14 A; T _j = 25 °C; Fig. 10		-	97	114	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 14 A; V _{DS} = 400 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 12 ; Fig. 13		-	0.8	-	nC
Q _{G(tot)}	total gate charge			-	4.9	-	nC
Source-drain diode							
Q _r	recovered charge	I _S = 20 A; dI _S /dt = -1000 A/μs; V _{GS} = 0 V; V _{DS} = 400 V; Fig. 20		-	65	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-247-3L (SOT429-3)	 aaa-028116
2	S	source		
3	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN111-650WSB	TO-247-3L	Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247-3L	SOT429-3

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN111-650WSB	GAN111 650WSB

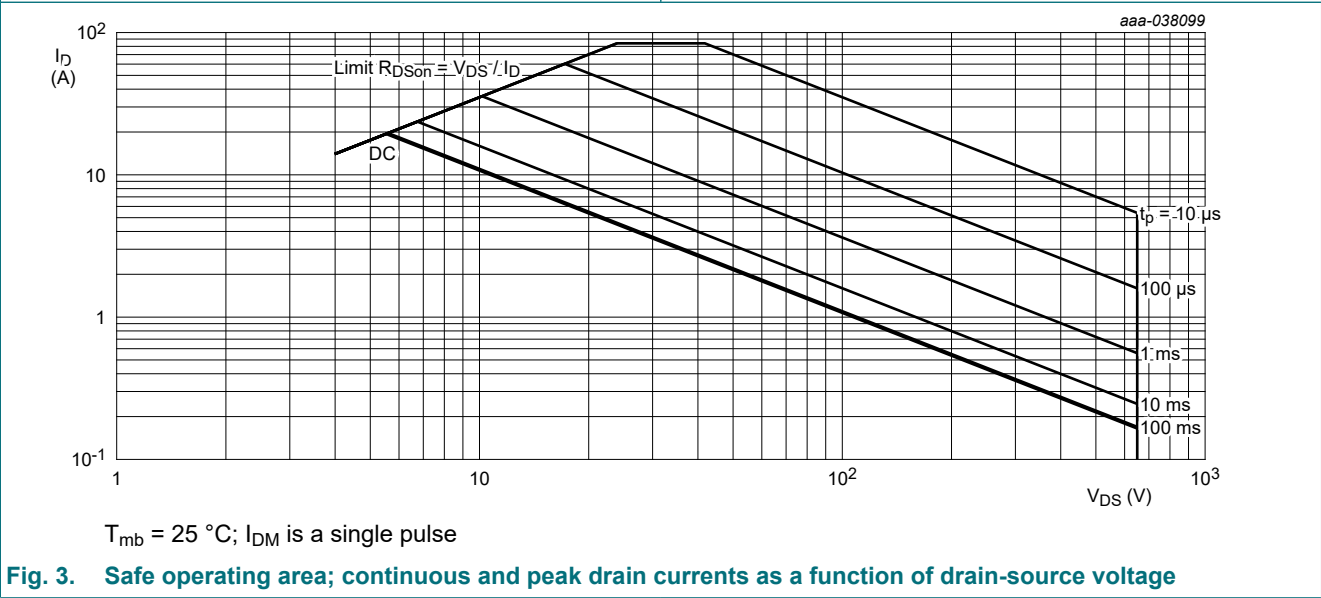
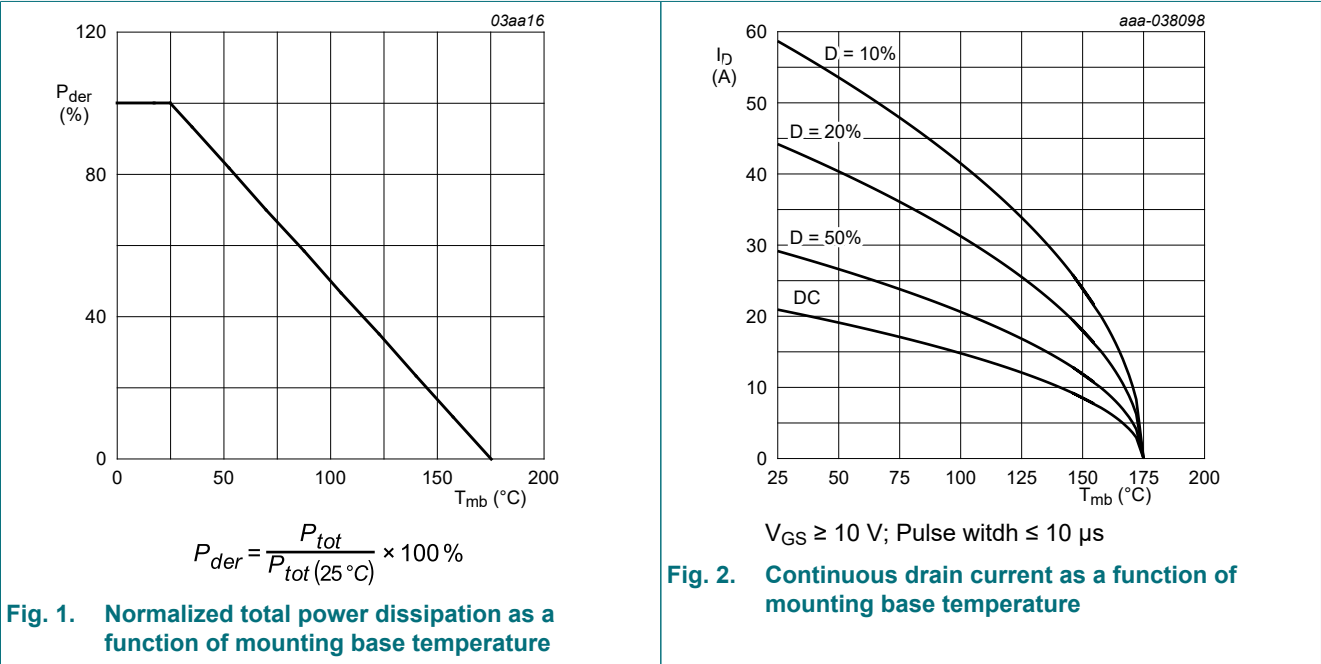
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	-55 °C ≤ T _J ≤ 175 °C	-	650	V
V _{TDS}	transient drain to source voltage	pulsed; t _p = 1 μs; δ _{factor} = 0.01	-	725	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	107	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	21	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	14.8	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	84	A
T _{stg}	storage temperature		-55	175	°C
T _J	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature	wave soldering only allowed at leads; soldering time of ≤ 10s	-	260	°C

Symbol	Parameter	Conditions		Min	Max	Unit
V _{ESD}	electrostatic discharge voltage	human body model		250	-	V
Source-drain diode						
I _S	source current	T _{mb} = 25 °C; V _{GS} = 0 V		-	21	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	84	A

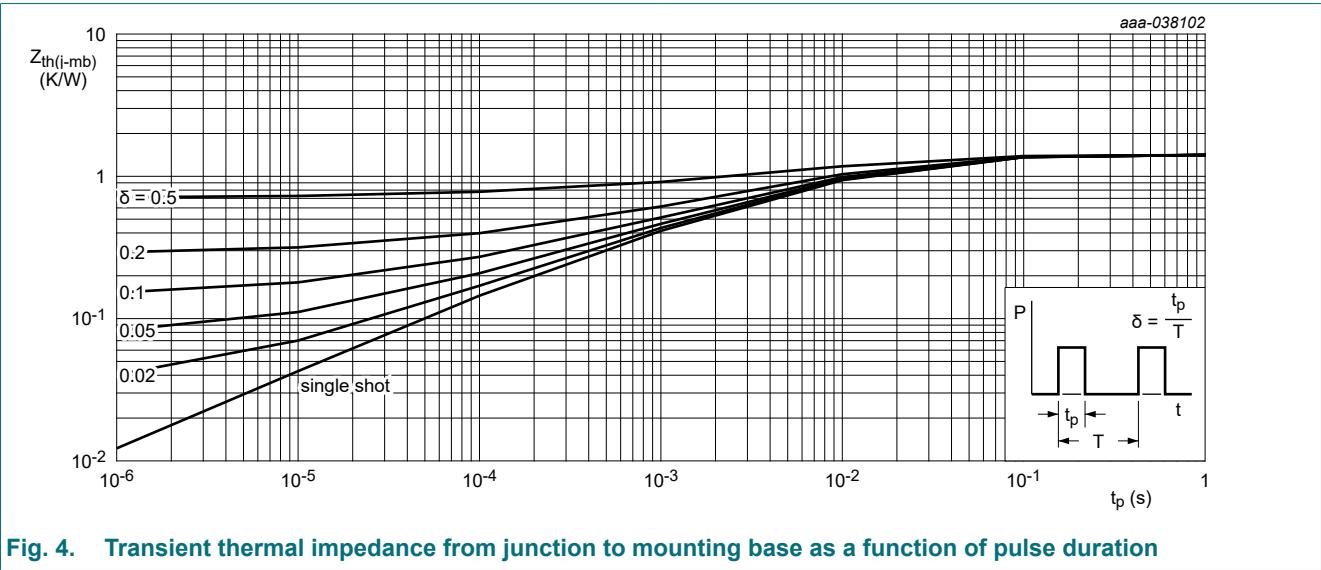


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 4	-	1	1.4	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W

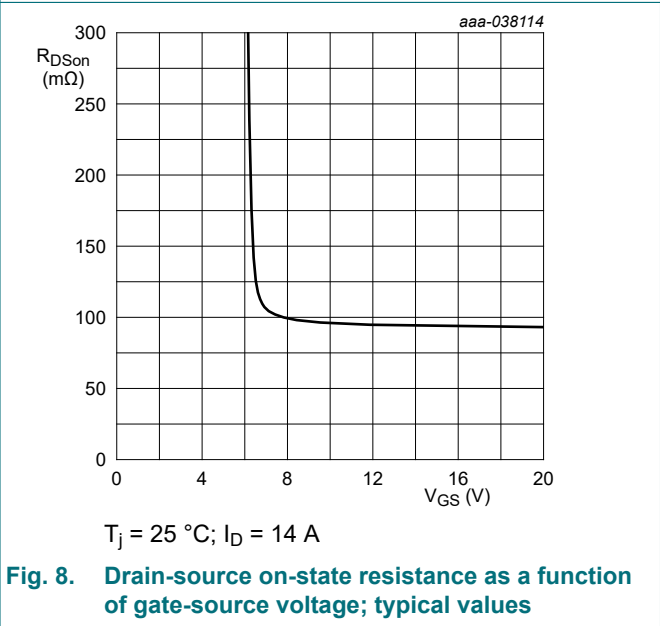
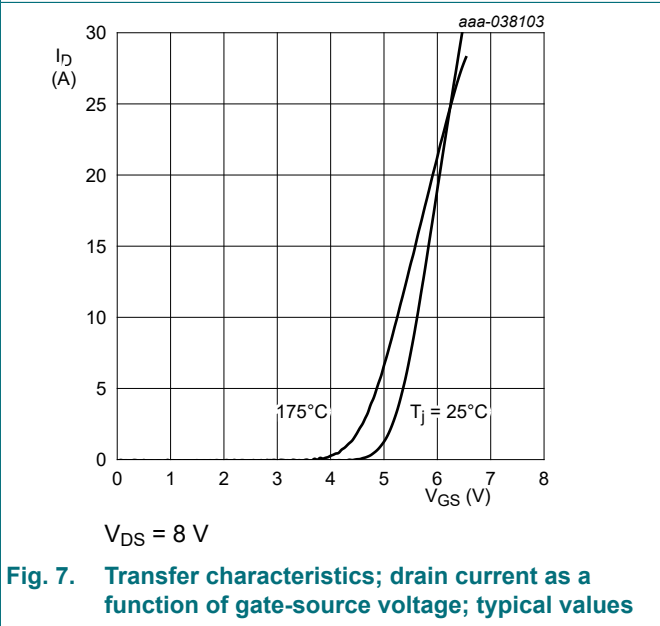
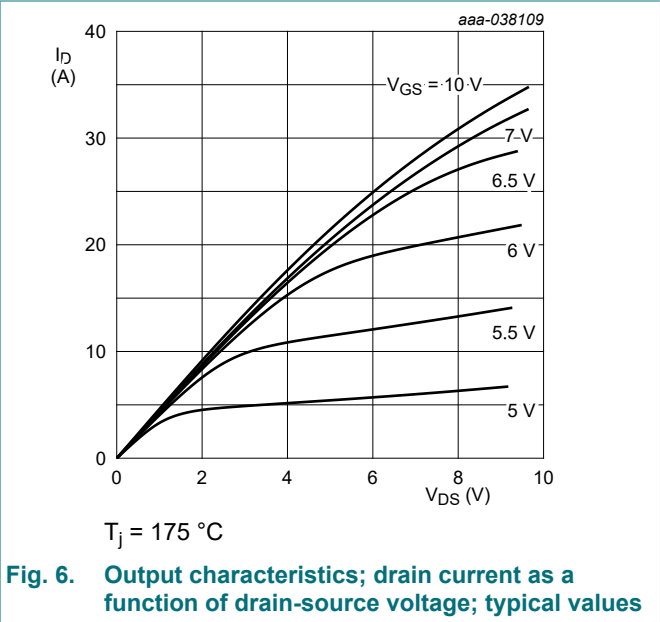
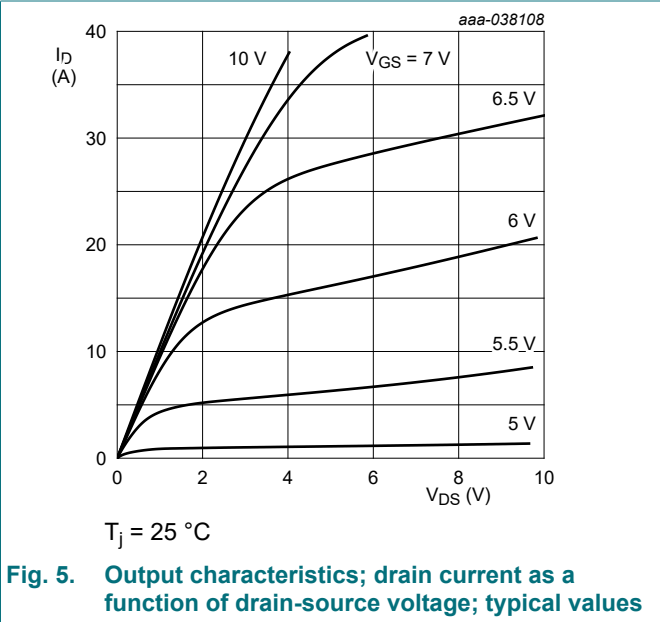


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$	3.5	4.1	4.8	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 175\text{ }^{\circ}\text{C}$; Fig. 9	2.4	-	-	V
		$I_D = 1\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55\text{ }^{\circ}\text{C}$; Fig. 9	-	-	5.4	V
I_{DSS}	drain leakage current	$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	1	10	μA
		$V_{DS} = 650\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^{\circ}\text{C}$	-	10	-	μA
I_{GSS}	gate leakage current	$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	10	400	nA
		$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	10	400	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 14\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 10	-	97	114	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 14\text{ A}$; $T_j = 175\text{ }^{\circ}\text{C}$; Fig. 11	-	242	285	m Ω
R_G	gate resistance	$f = 1\text{ MHz}$	2.4	6	15	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 14\text{ A}$; $V_{DS} = 400\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 12 ; Fig. 13	-	4.9	-	nC
Q_{GS}	gate-source charge		-	2.3	-	nC
Q_{GD}	gate-drain charge		-	0.8	-	nC
C_{iss}	input capacitance	$V_{DS} = 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 14	-	336	-	pF
C_{oss}	output capacitance		-	49	-	pF
C_{rss}	reverse transfer capacitance		-	0.3	-	pF
$C_{o(er)}$	effective output capacitance, energy related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 15	-	70	-	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{o(tr)}$	effective output capacitance, time related	$0\text{ V} \leq V_{DS} \leq 400\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ }^{\circ}\text{C}$		-	162	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 400\text{ V}$; $R_L = 29\text{ }\Omega$; $V_{GS} = 12\text{ V}$; $R_{G(ext)} = 12\text{ }\Omega$; $I_S = 14\text{ A}$; Fig. 16 ; Fig. 17		-	13	-	ns
t_r	rise time			-	12	-	ns
$t_{d(off)}$	turn-off delay time			-	20	-	ns
t_f	fall time			-	8	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; Fig. 18		-	65	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 14\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$; Fig. 19		-	1.8	-	V
		$I_S = 7\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$; Fig. 19		-	1.3	-	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -1000\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; Fig. 20		-	18	-	ns
Q_r	recovered charge			-	65	-	nC



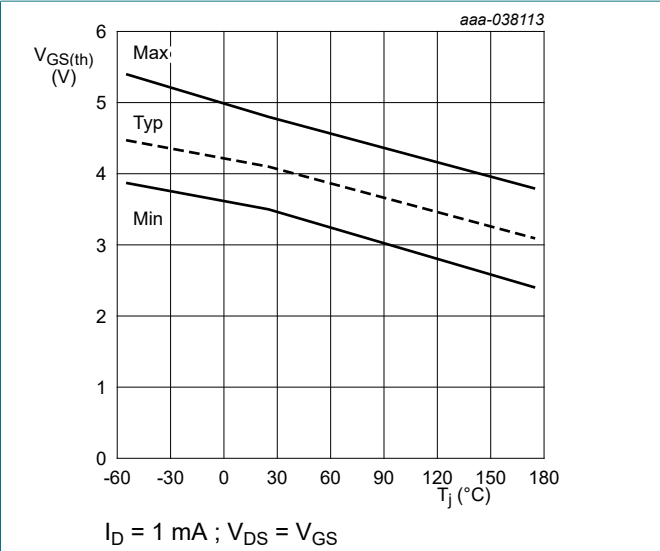


Fig. 9. Gate-source threshold voltage as a function of junction temperature

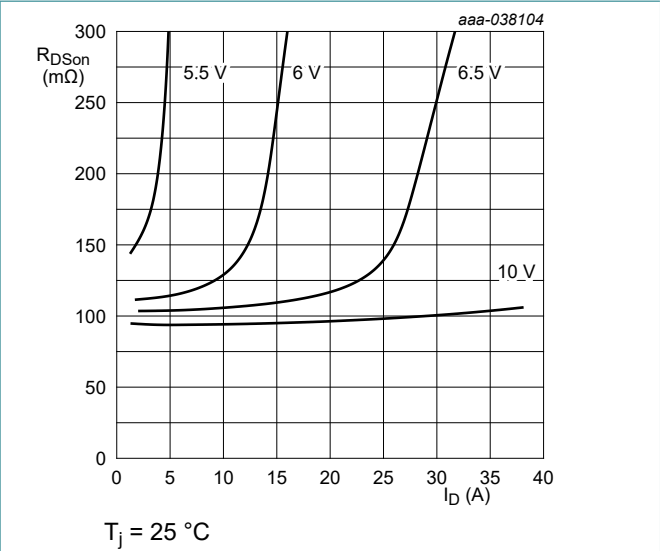


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

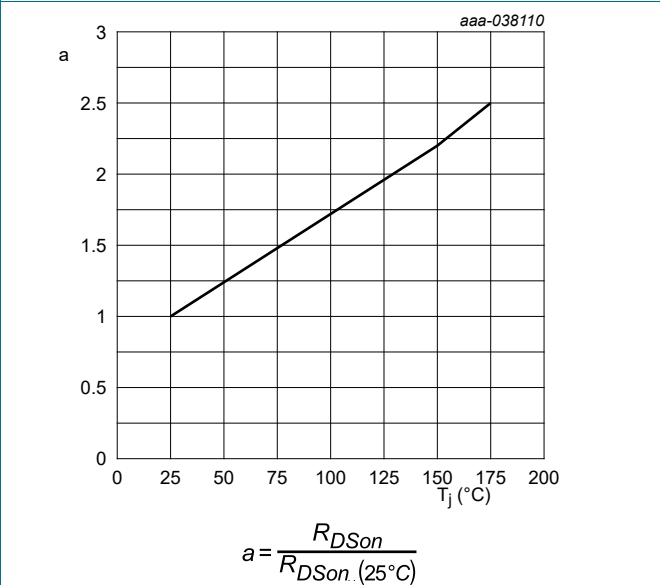


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

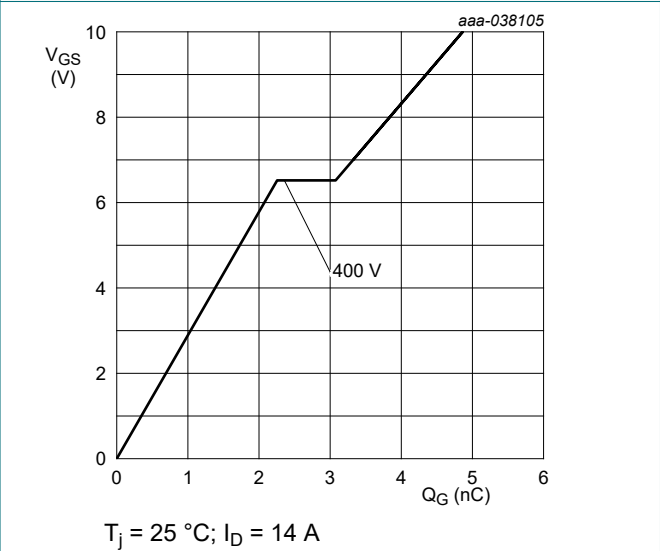


Fig. 12. Gate-source voltage as a function of gate charge; typical values

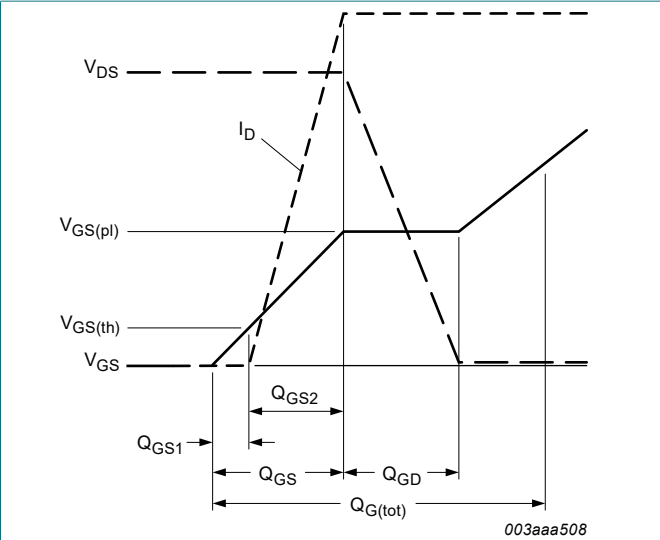


Fig. 13. Gate charge waveform definitions

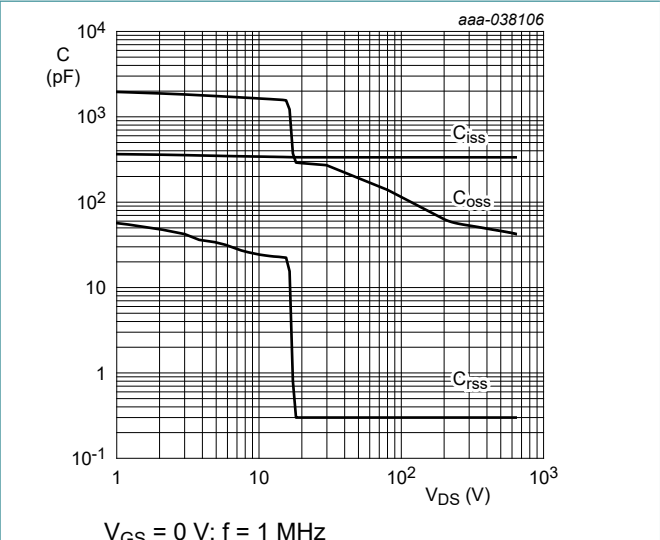


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

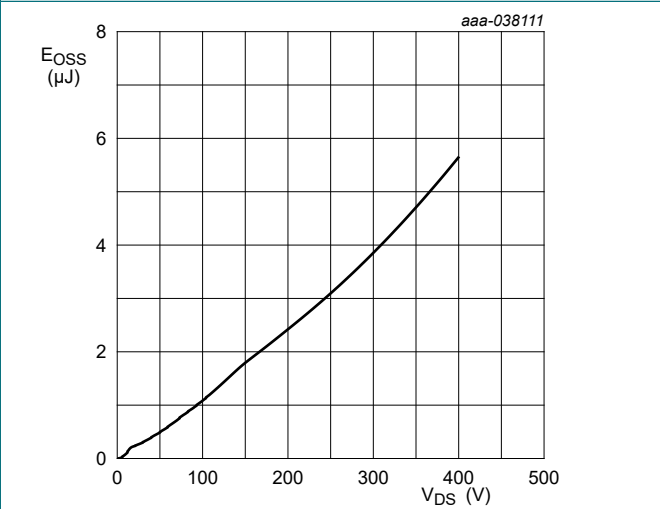


Fig. 15. Typical COSS Stored Energy

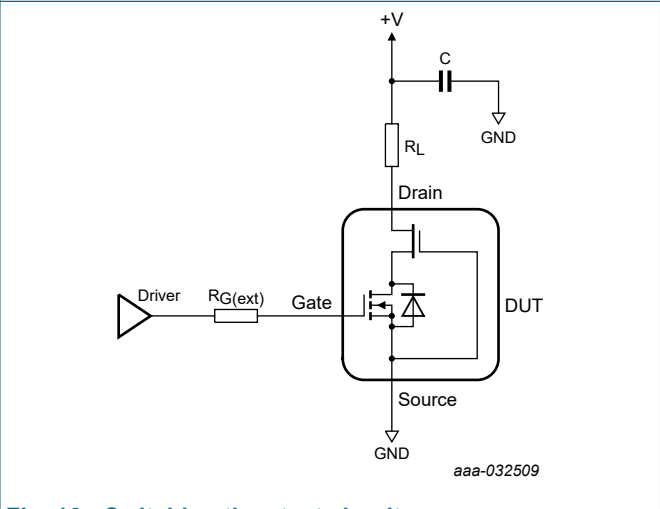


Fig. 16. Switching time test circuit

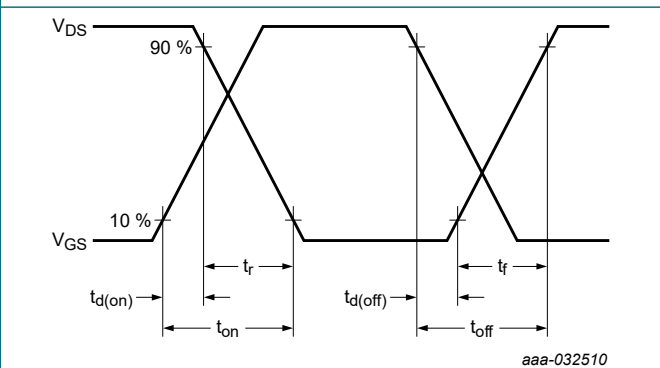


Fig. 17. Switching time waveform

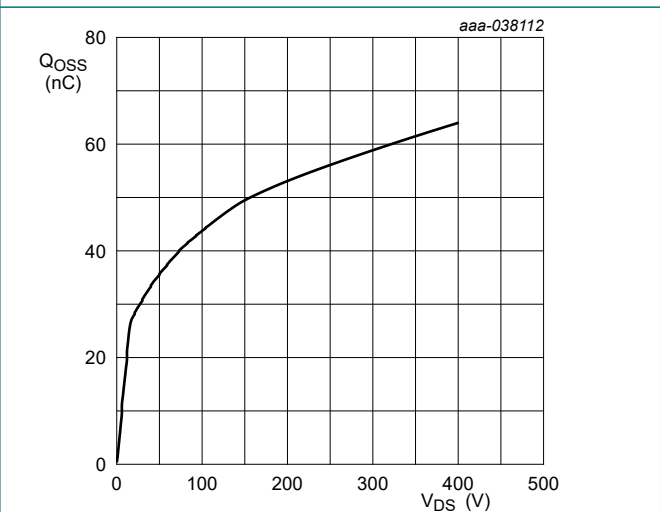
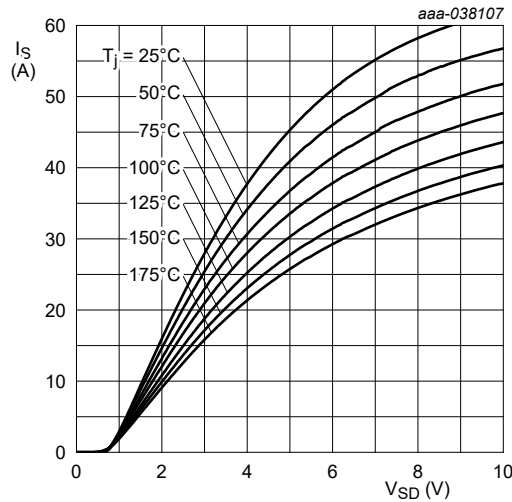


Fig. 18. Typical QOSS



$V_{GS} = 0 \text{ V}$

Fig. 19. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

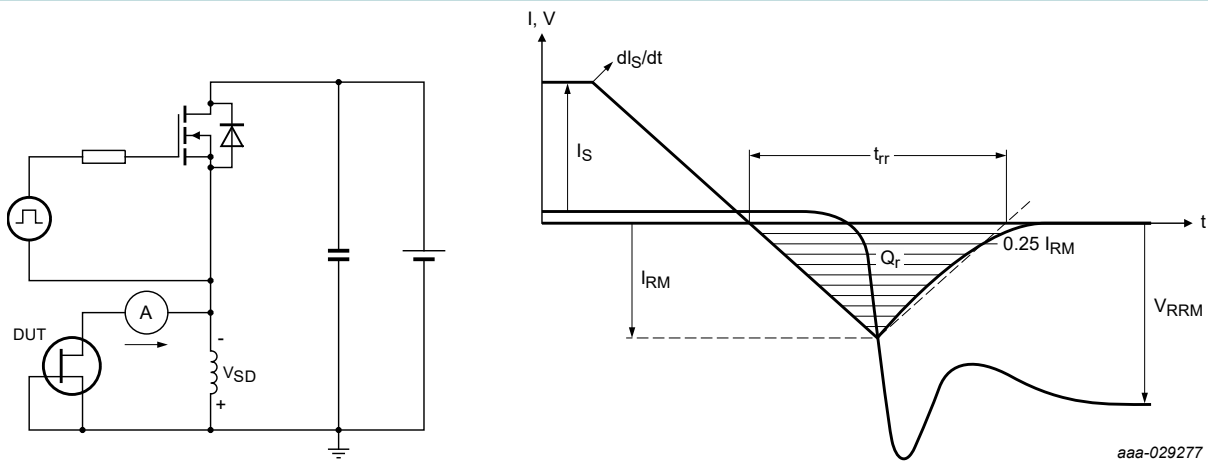


Fig. 20. Diode reverse recovery test circuit and waveform

11. Application information

To achieve stable switching performance, the following recommendations should be adopted:

- Gate resistor, $R_G = 30 \Omega$
- Gate ferrite bead = $30 \Omega @ 100 \text{ MHz}$ (part number: BLM18PG300SN1D)
- Switch node snubber, $R_{SN} = 33 \text{ pF}$, 37.5Ω optional

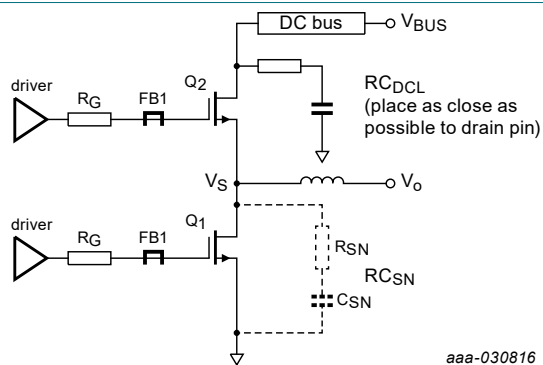


Fig. 21. Ferrite bead and RC snubber

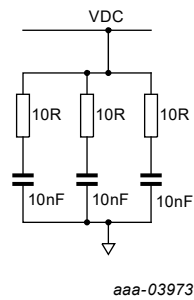


Fig. 22. Parallel RC combination

650 V, 97 mOhm Gallium Nitride (GaN) FET in a TO-247 package

Note: A DC-link resonance damper is recommended in all cases. Optimal is 30 nF in series with 3.3 Ω , most easily achieved with parallel combination 10 nF and 10 Ω . This resonance damper lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

12. Package outline

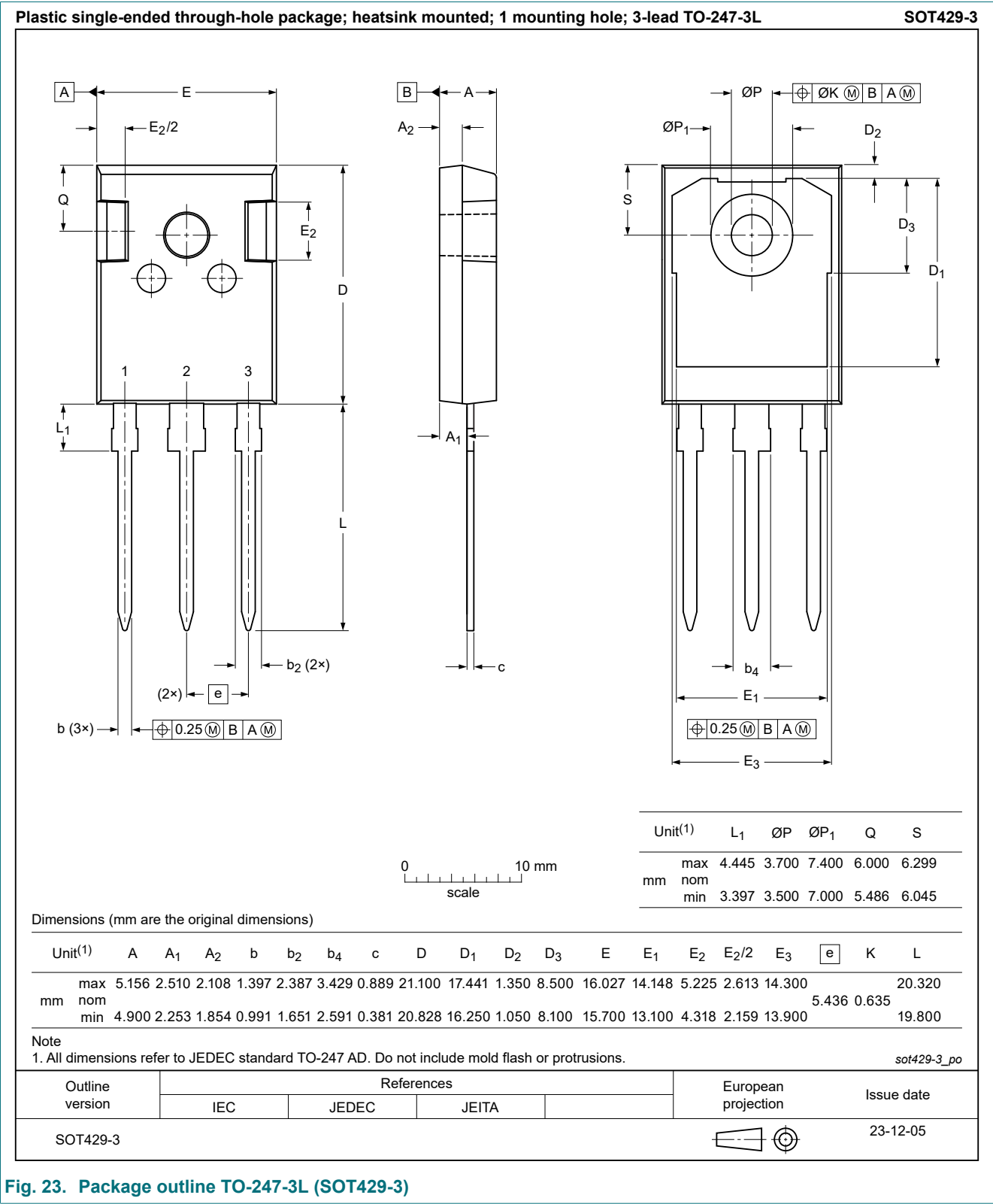


Fig. 23. Package outline TO-247-3L (SOT429-3)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 24 June 2024

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