



BUK9M4R3-40H

N-channel 40 V, 4.3 mΩ logic level MOSFET in LPAK33

10 January 2025

Product data sheet

1. General description

Automotive qualified logic level N-channel MOSFET in an LPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
 - Low power losses, high power density
- LPAK copper clip package technology:
 - High robustness and reliability
 - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

4. Quick reference data

Table 1. Quick reference data

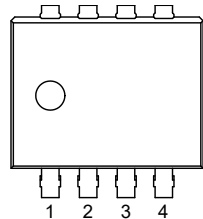
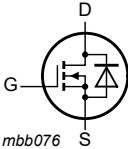
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	95	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	90	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		2.4	3.4	4.3	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 13 ; Fig. 14		-	3.3	6.6	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$		-	20	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	0.66	-	

[1] 95A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M4R3-40H	LPAK33	Plastic, single ended surface mounted package (LPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M4R3-40H	94H340

8. Limiting values

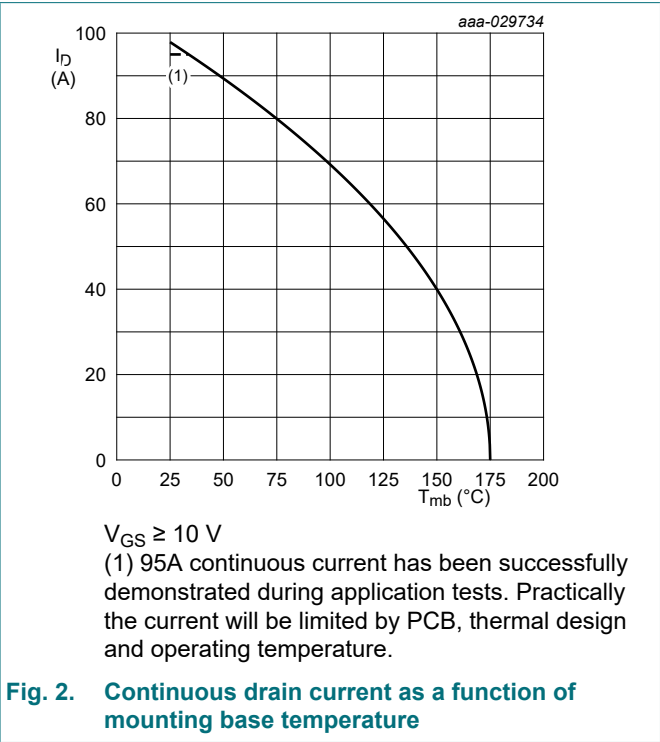
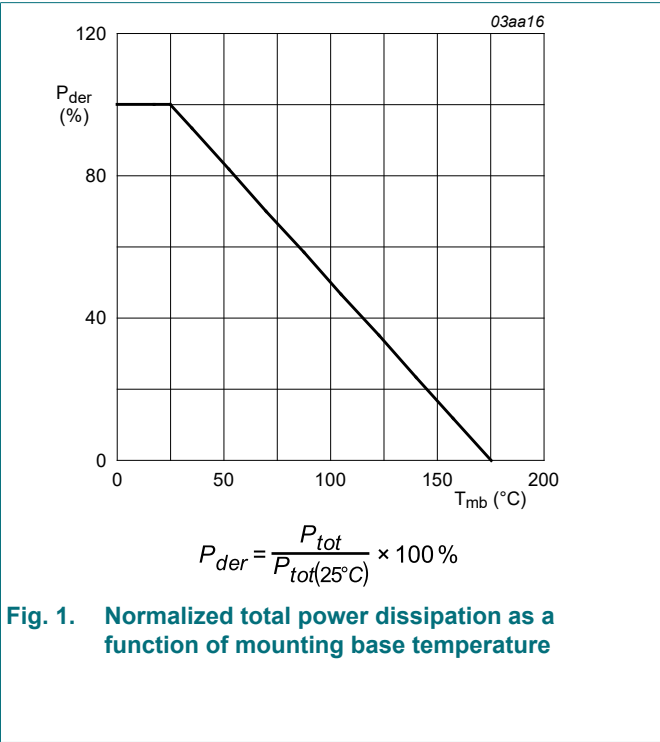
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ }^\circ\text{C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
V_{GS}	gate-source voltage		[1] -20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	90	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[2] -	95	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2	-	69	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	392	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	95	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	392	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 70 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3] [4] [5]	-	44	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[5]	-	70	A

- [1] Refer to application note AN90001 for further information.
- [2] 95A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.
- [5] Protected by 100% test.



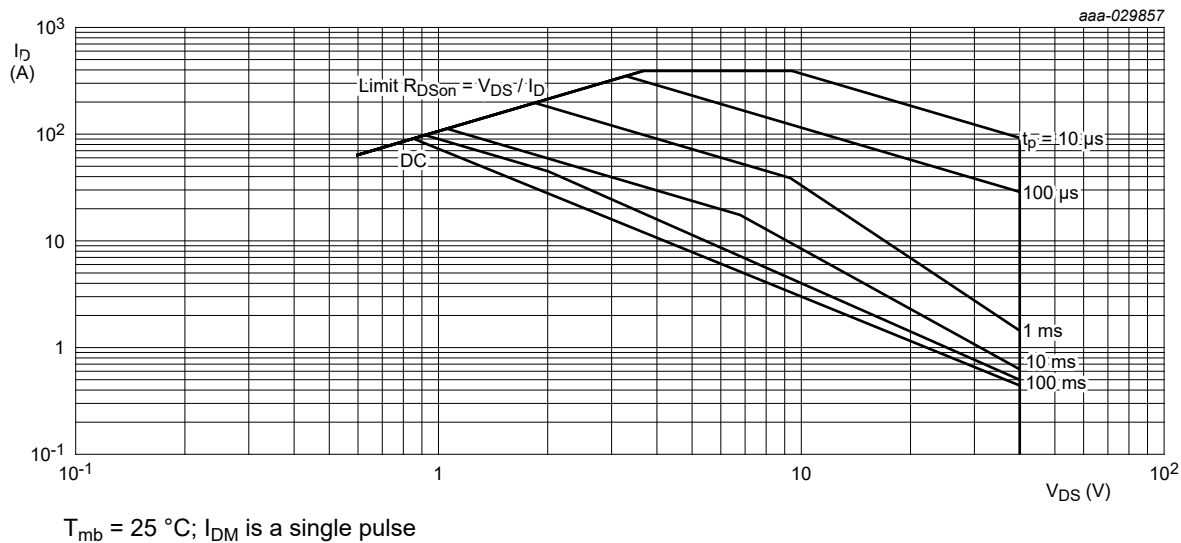
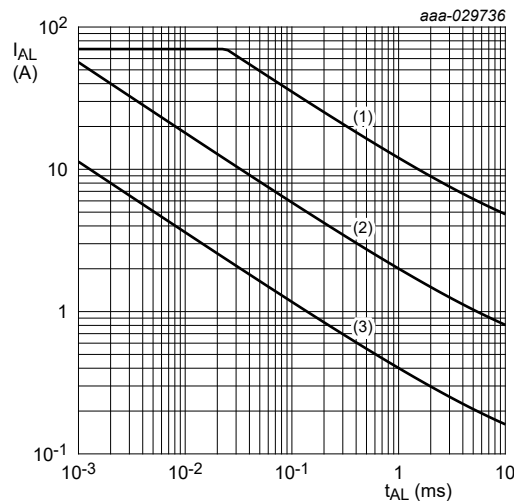


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



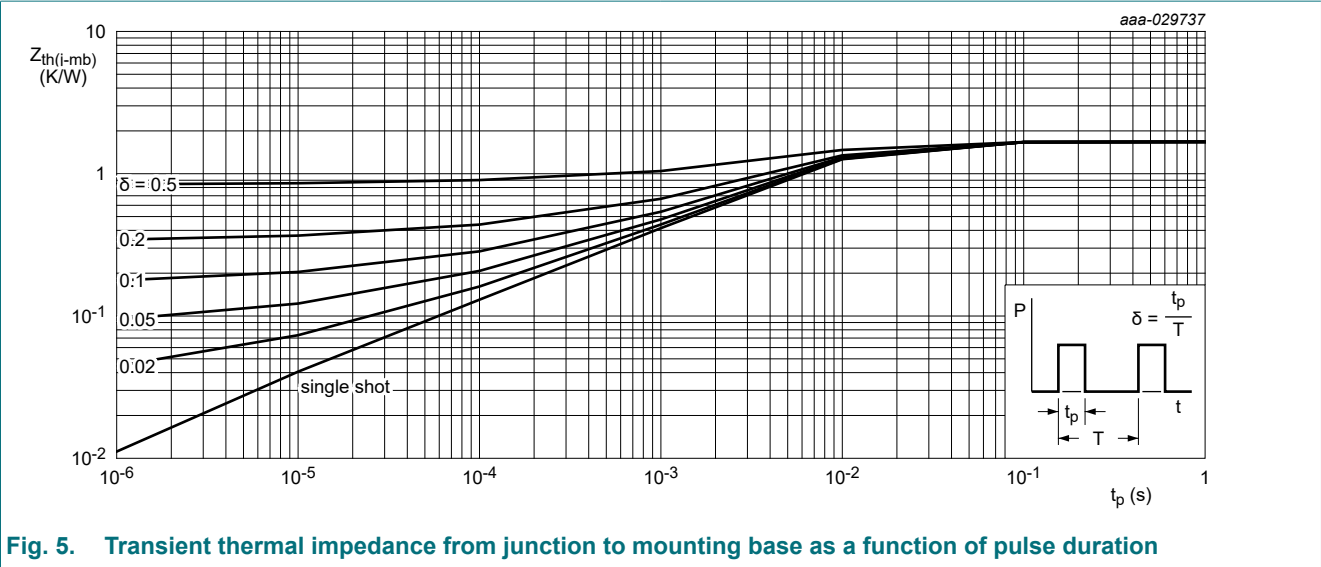
(1) $T_{j\text{ (init)}} = 25\text{ }^{\circ}\text{C}$; (2) $T_{j\text{ (init)}} = 150\text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.48	1.67	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	43	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C	-	40.5	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	40	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10	1.45	1.77	2.15	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C; Fig. 10	-	-	2.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C; Fig. 10	0.7	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C	-	0.03	5	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _J = 125 °C	-	0.76	10	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 175 °C	-	63	500	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11		2.4	3.4	4.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 12		3.5	5.2	6.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 12		3.9	5.8	7.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12		5	7.1	9.4	mΩ
		V _{GS} = 4.5 V; I _D = 20 A; T _j = 25 °C; Fig. 11		3	4.4	5.5	mΩ
		V _{GS} = 4.5 V; I _D = 20 A; T _j = 105 °C; Fig. 12		4.5	6.5	8.6	mΩ
		V _{GS} = 4.5 V; I _D = 20 A; T _j = 125 °C; Fig. 12		4.9	7.2	9.6	mΩ
		V _{GS} = 4.5 V; I _D = 20 A; T _j = 175 °C; Fig. 12		6.2	8.8	12	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.3	0.8	2	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14		-	31	43	nC
		I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 13 ; Fig. 14		-	14	20	nC
Q _{GS}	gate-source charge			-	5.6	8.4	nC
Q _{GD}	gate-drain charge			-	3.3	6.6	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	2132	2985	pF
C _{oss}	output capacitance			-	491	687	pF
C _{rss}	reverse transfer capacitance			-	80	176	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 0.8 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω		-	14	-	ns
t _r	rise time			-	16	-	ns
t _{d(off)}	turn-off delay time			-	15	-	ns
t _f	fall time			-	9.3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.83	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; Fig. 17		-	26	-	ns
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V		-	20	-	nC
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 17		-	0.66	-	
		I _S = 25 A; dI _S /dt = -500 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 17		-	0.44	-	

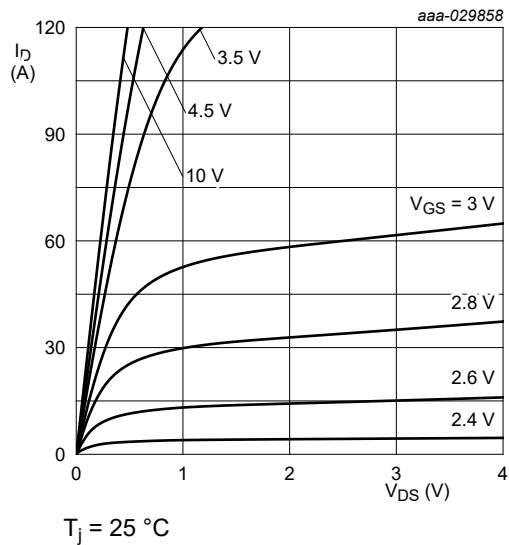


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

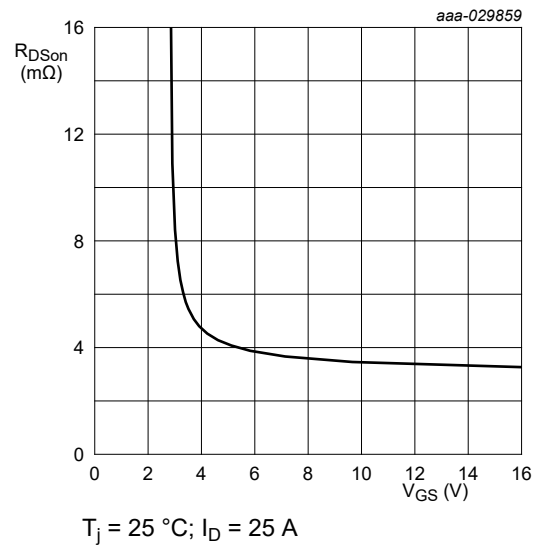


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

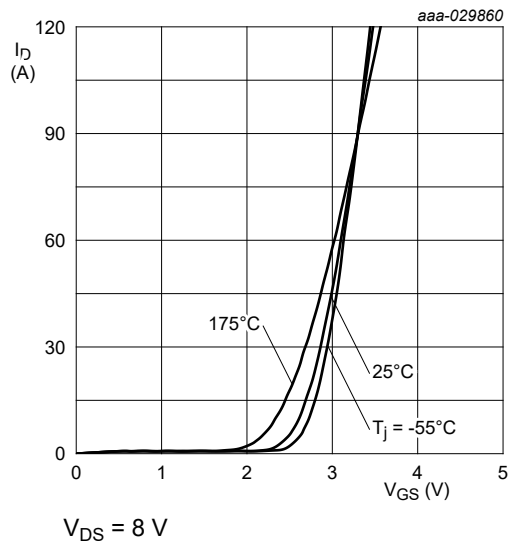


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

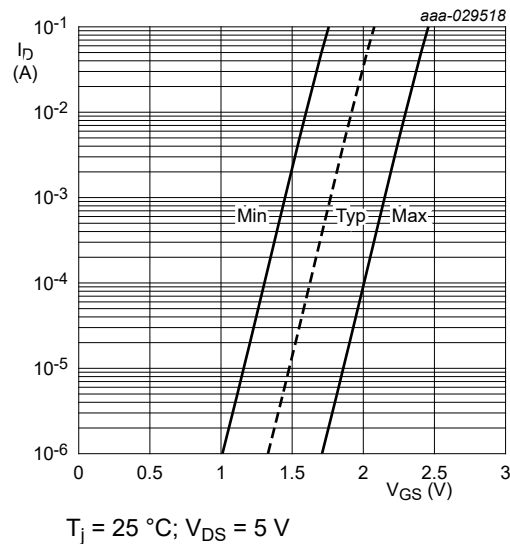


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

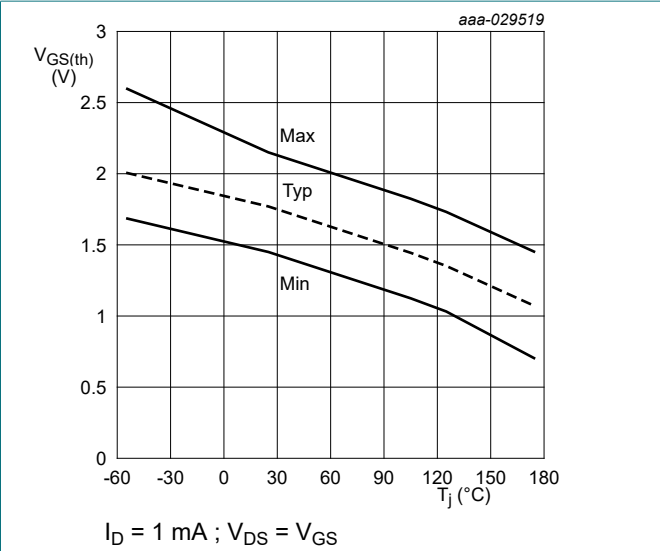


Fig. 10. Gate-source threshold voltage as a function of junction temperature

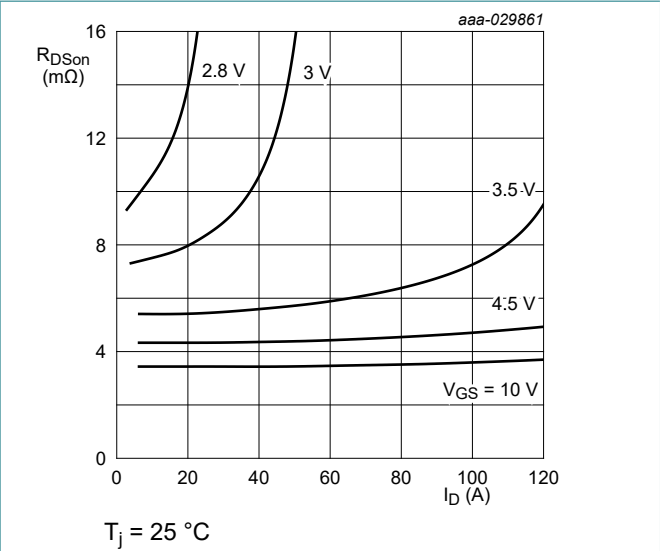


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

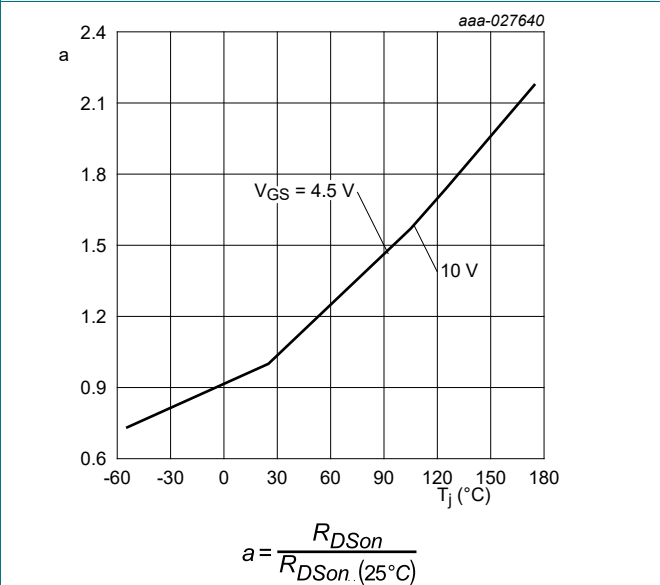


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

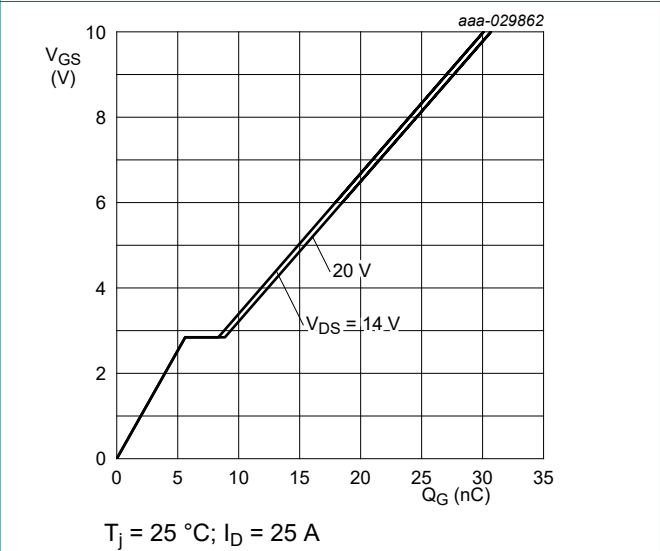


Fig. 13. Gate-source voltage as a function of gate charge; typical values

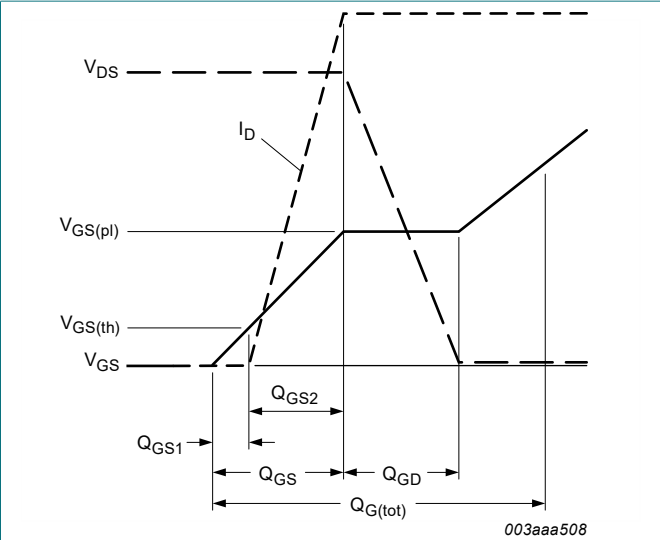


Fig. 14. Gate charge waveform definitions

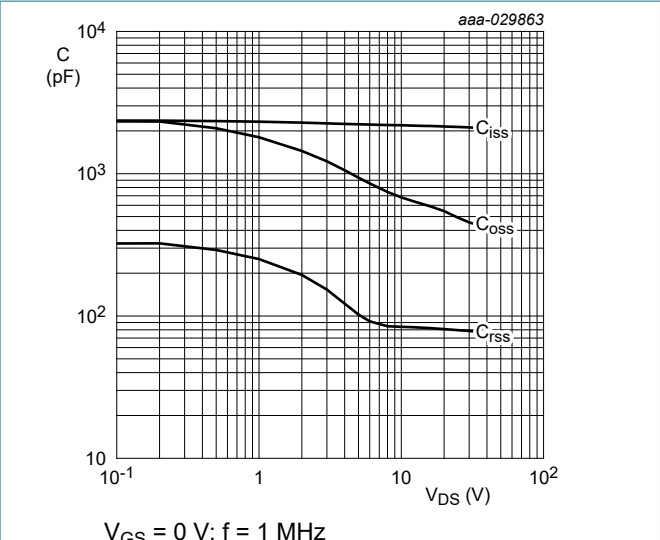


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

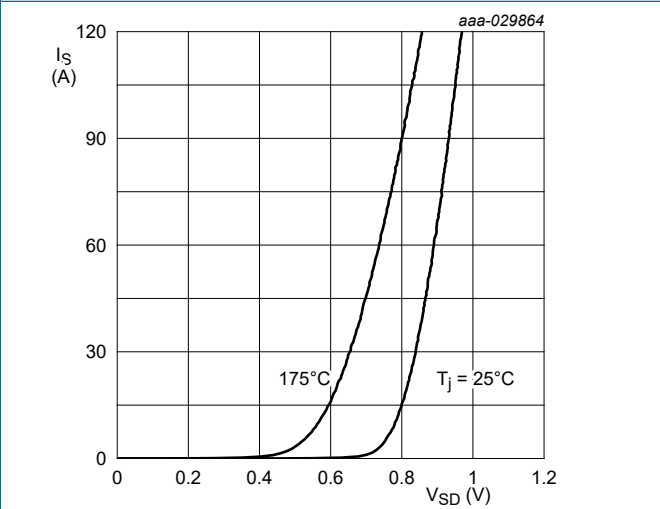


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

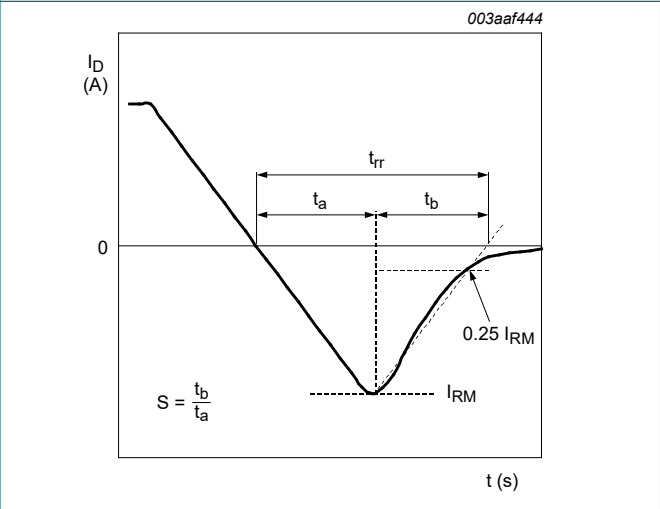


Fig. 17. Reverse recovery timing definition

11. Package outline

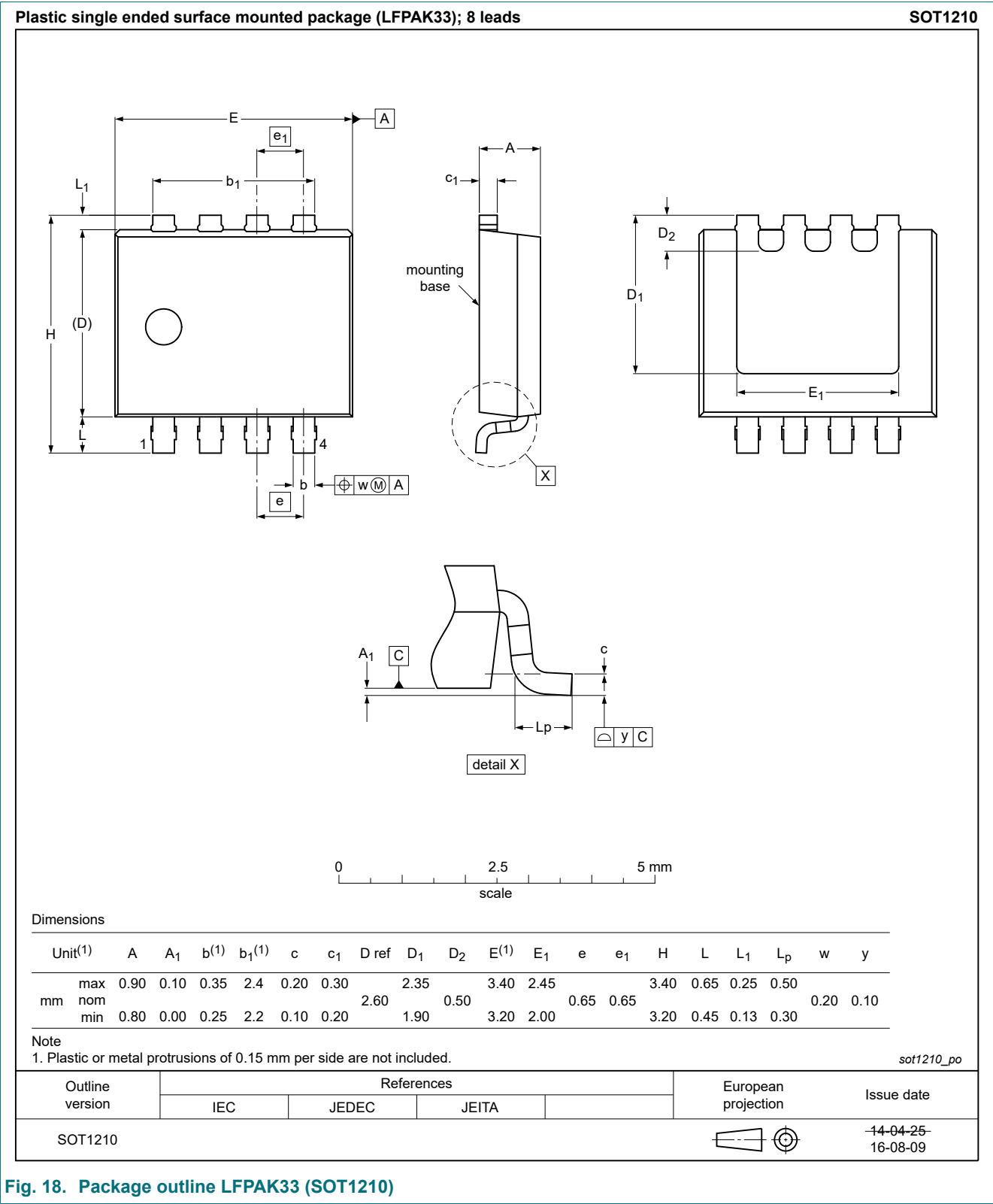


Fig. 18. Package outline LPAK33 (SOT1210)

12. Soldering

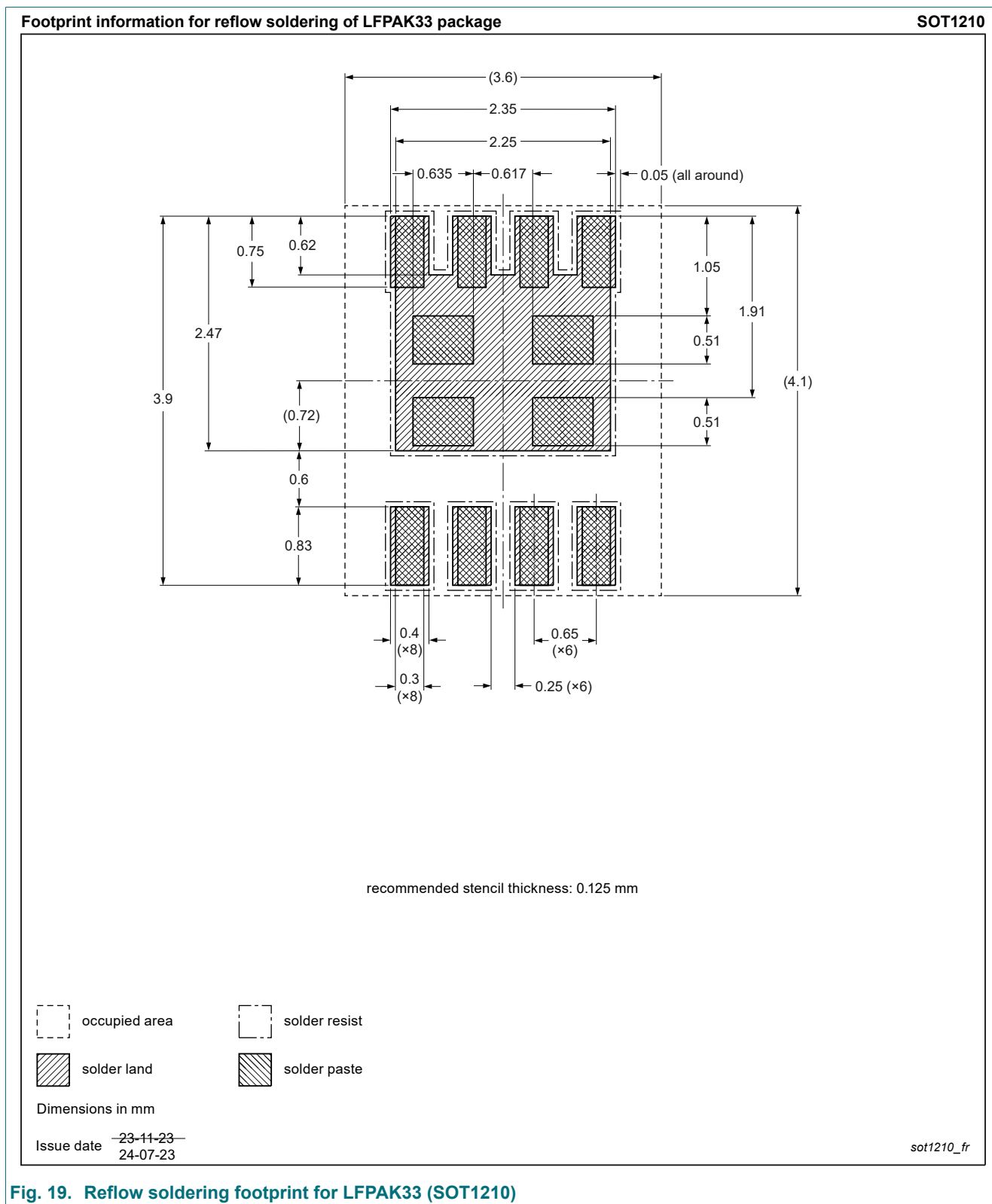


Fig. 19. Reflow soldering footprint for LPAK33 (SOT1210)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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