

Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

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If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

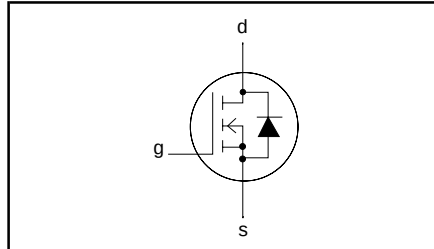
Kind regards,

Team Nexperia

N-channel enhancement mode TrenchMOS™ transistor

BSP100**FEATURES**

- 'Trench' technology
- Low on-state resistance
- Fast switching
- High thermal cycling performance
- Low thermal resistance

SYMBOL**QUICK REFERENCE DATA**

$$V_{DSS} = 30 \text{ V}$$

$$I_D = 6 \text{ A}$$

$$R_{DS(ON)} \leq 100 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$$

$$R_{DS(ON)} \leq 200 \text{ m}\Omega \text{ (} V_{GS} = 4.5 \text{ V)}$$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect transistor in a plastic envelope using 'trench' technology.

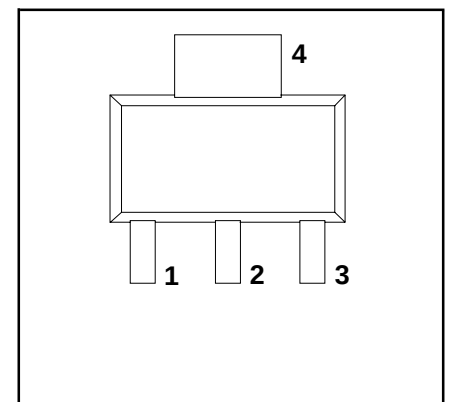
Applications:-

- Motor and relay drivers
- d.c. to d.c. converters
- Logic level translator

The BSP100 is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

SOT223**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 150°C	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 20 \text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{sp} = 25^\circ\text{C}$	-	6 ¹	A
		$T_{sp} = 100^\circ\text{C}$	-	4.4	A
		$T_{amb} = 25^\circ\text{C}$	-	3.2	A
I_{DM}	Pulsed drain current	$T_{sp} = 25^\circ\text{C}$	-	24	A
P_D	Total power dissipation	$T_{sp} = 25^\circ\text{C}$	-	8.3	W
T_j, T_{stg}	Operating junction and storage temperature		- 65	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th j-sp}$	Thermal resistance junction to solder point	surface mounted, FR4 board	12	15	K/W
$R_{th j-amb}$	Thermal resistance junction to ambient	surface mounted, FR4 board	70	-	K/W

¹ Continuous current rating limited by package

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 6$ A; $t_p = 0.2$ ms; T_j prior to avalanche = 25°C ; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V	-	23	mJ
I_{AS}	Non-repetitive avalanche current		-	6	A

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 10$ μA ; $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.4 -	2 - -	2.8 - 3.2	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 2.2$ A $V_{GS} = 4.5$ V; $I_D = 1$ A $V_{GS} = 10$ V; $I_D = 2.2$ A; $T_j = 150^\circ\text{C}$	- - -	80 120 -	100 200 170	m Ω m Ω m Ω
g_{fs}	Forward transconductance	$V_{DS} = 20$ V; $I_D = 2.2$ A	2	4.5	-	S
$I_{D(ON)}$	On-state drain current	$V_{GS} = 10$ V; $V_{DS} = 1$ V; $V_{GS} = 4.5$ V; $V_{DS} = 5$ V	3.5 2	- -	- -	A A
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 24$ V; $V_{GS} = 0$ V; $V_{DS} = 24$ V; $V_{GS} = 0$ V; $T_j = 150^\circ\text{C}$	- -	10 0.6	100 10	nA μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 2.3$ A; $V_{DD} = 15$ V; $V_{GS} = 10$ V	-	6	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	0.7	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 20$ V; $R_D = 18$ Ω ; $V_{GS} = 10$ V; $R_G = 6$ Ω	-	6 8	- -	ns ns
t_r	Turn-on rise time		-	21	-	ns
t_{doff}	Turn-off delay time	Resistive load	-	15	-	ns
t_f	Turn-off fall time		-	-	-	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 20$ V; $f = 1$ MHz	-	250	-	pF
C_{oss}	Output capacitance		-	88	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

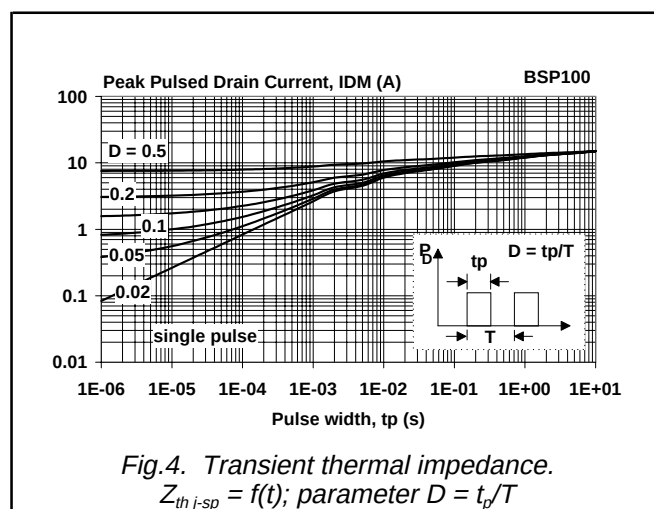
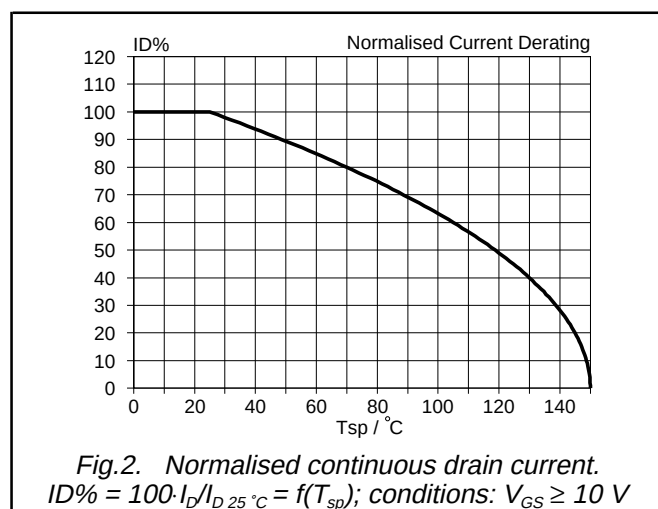
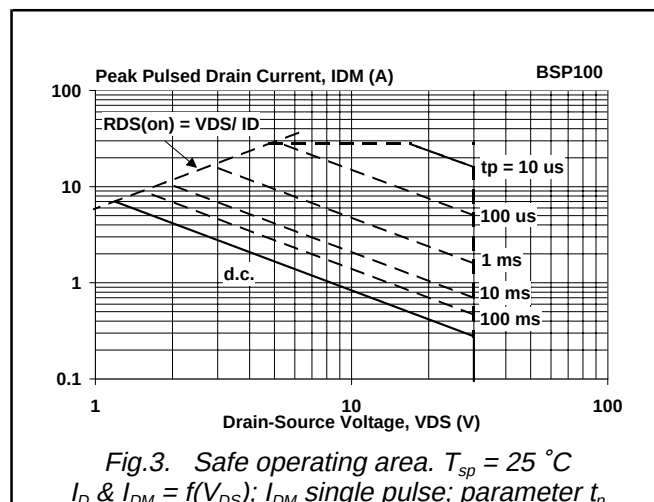
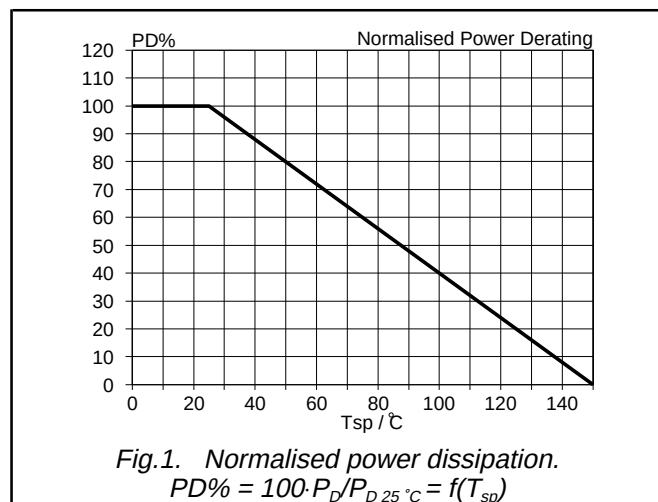
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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{sp} = 25^\circ\text{C}$	-	-	6	A
I_{SM}	Pulsed source current (body diode)		-	-	24	A
V_{SD}	Diode forward voltage	$I_F = 1.25\text{ A}; V_{GS} = 0\text{ V}$	-	0.82	1.2	V
t_{rr}	Reverse recovery time	$I_F = 1.25\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_R = 25\text{ V}$	-	69	-	ns
Q_{rr}	Reverse recovery charge		-	55	-	nC



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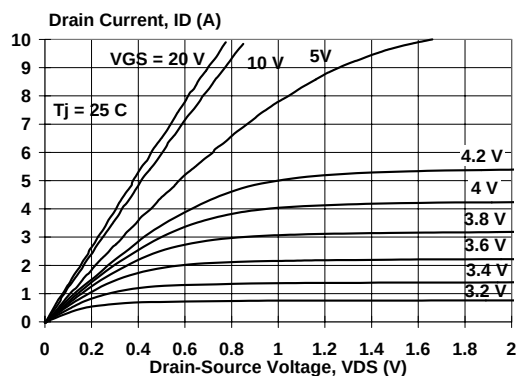


Fig.5. Typical output characteristics, $T_j = 25\text{ }^{\circ}\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

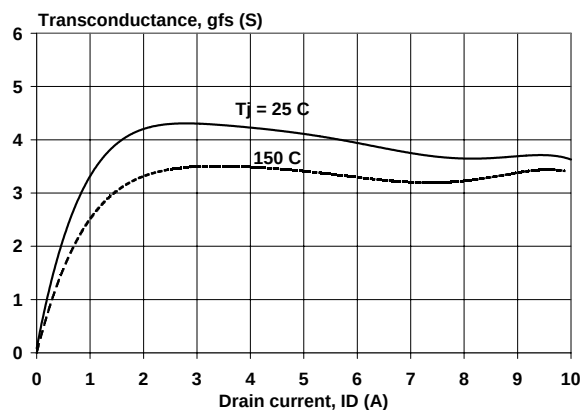


Fig.8. Typical transconductance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $g_{fs} = f(I_D)$; parameter T_j

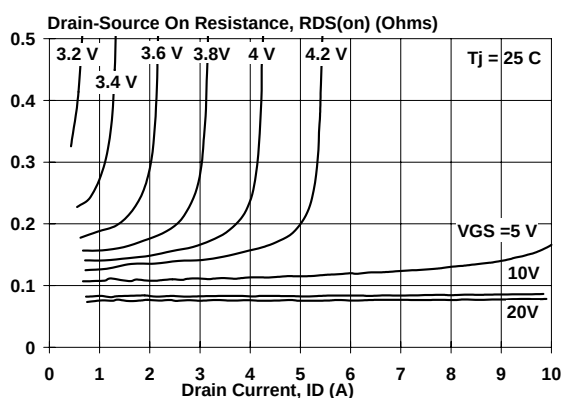


Fig.6. Typical on-state resistance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

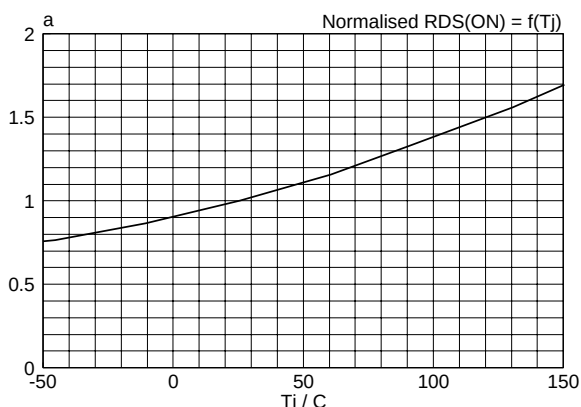


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^{\circ}\text{C}} = f(T_j)$

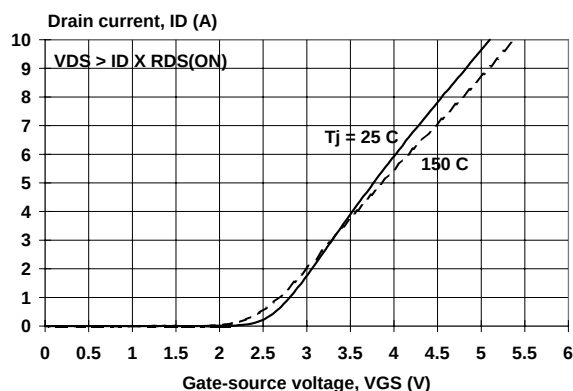


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; parameter T_j

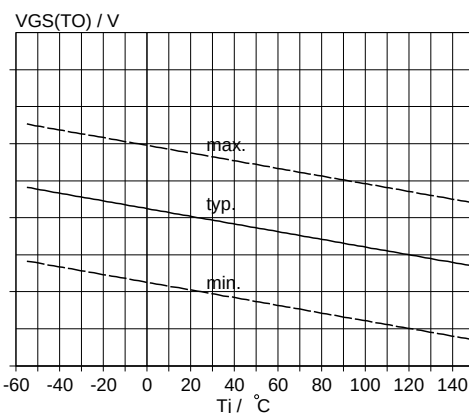
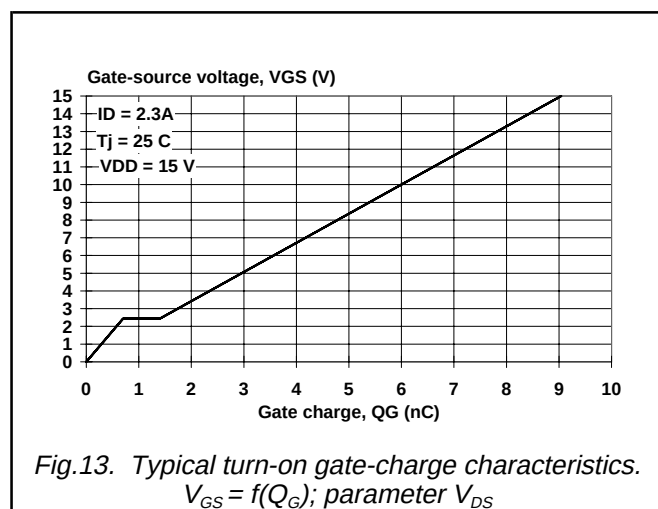
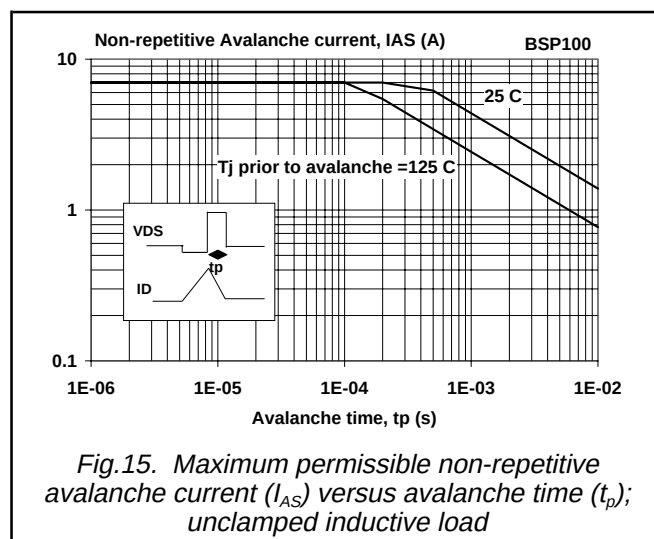
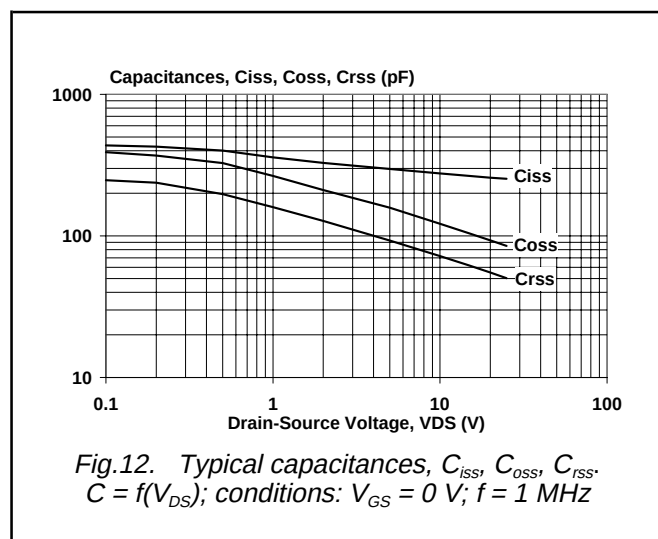
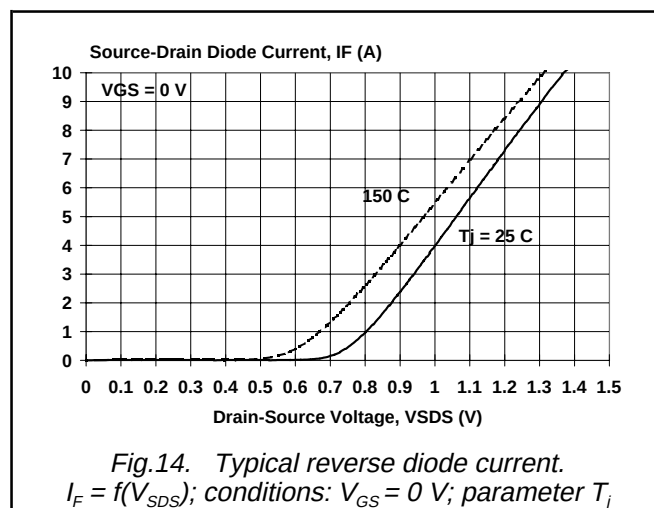
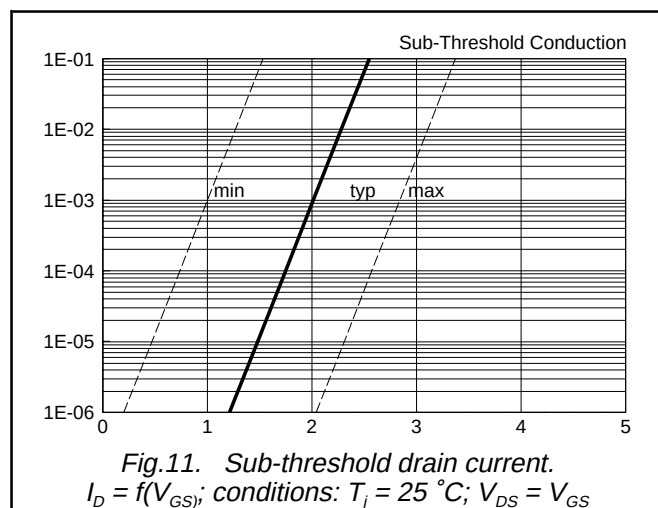


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

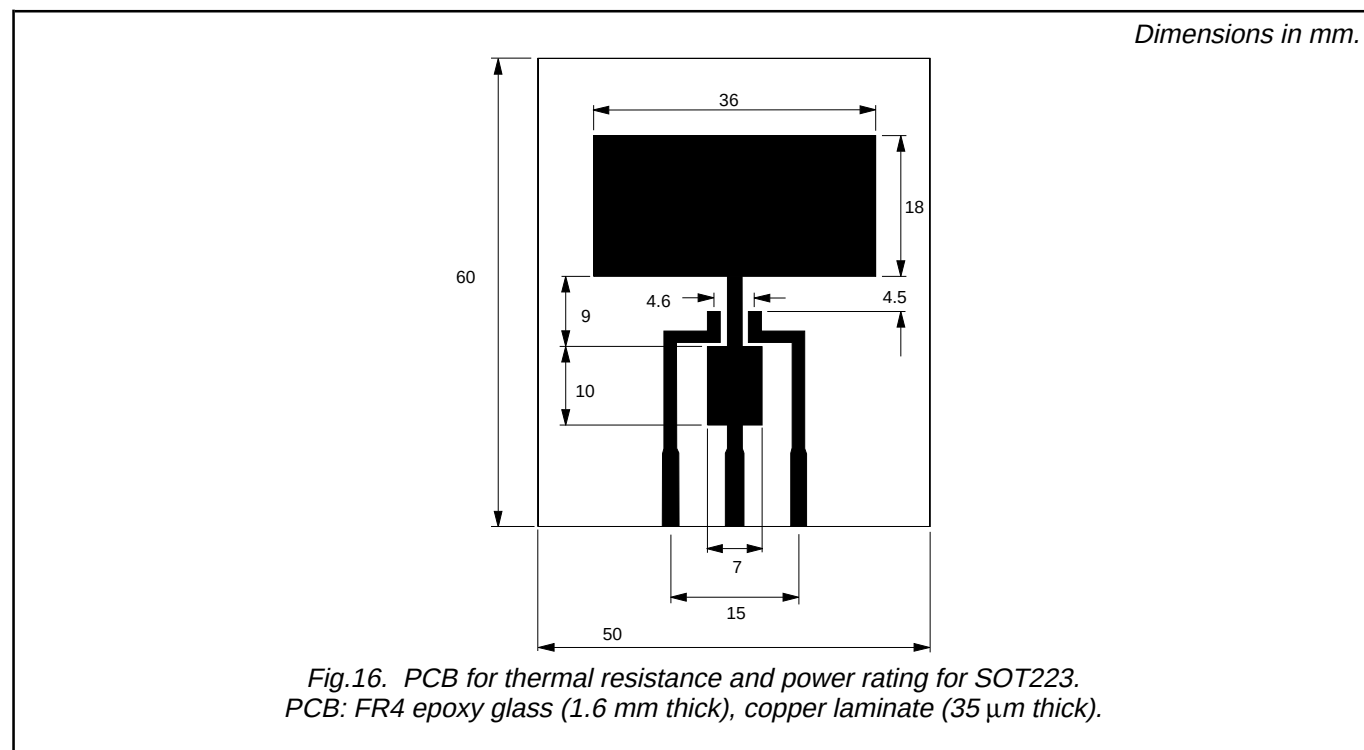
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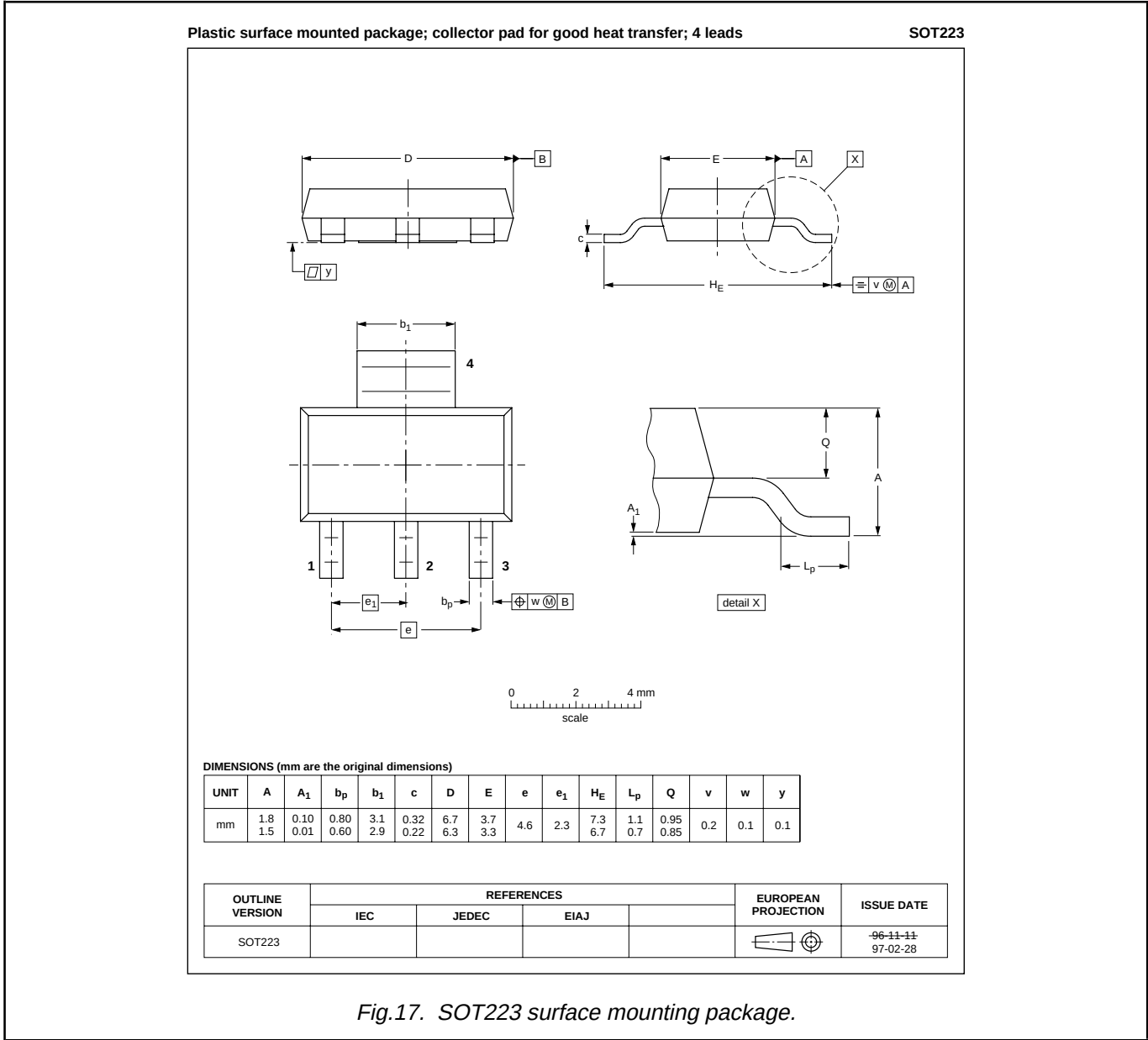
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PRINTED CIRCUIT BOARD

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MECHANICAL DATA



- Notes**
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
 2. Refer to Discrete Semiconductor Packages, Data Handbook SC18.
 3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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