74LVC157A-Q100

Quad 2-input multiplexer

Rev. 3 — 19 March 2020 Product data sheet

1. General description

The 74LVC157A-Q100 is a quad 2-input multiplexer which select four bits of data from two sources under the control of a common select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When pin $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all the other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LVC157A-Q100. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

It is useful for implementing highly irregular logic by generating any 4 of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to pin S.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
-
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V (C = 200 pF, R = 0 Ω)
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC157AD-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC157APW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC157ABQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

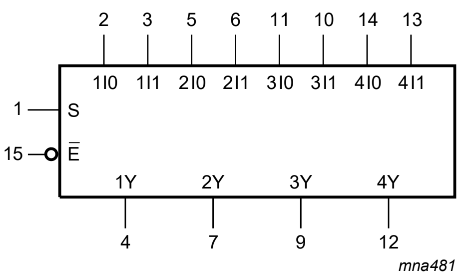


Fig. 1. Logic symbol

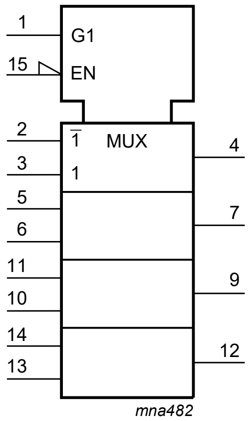


Fig. 2. IEC logic symbol

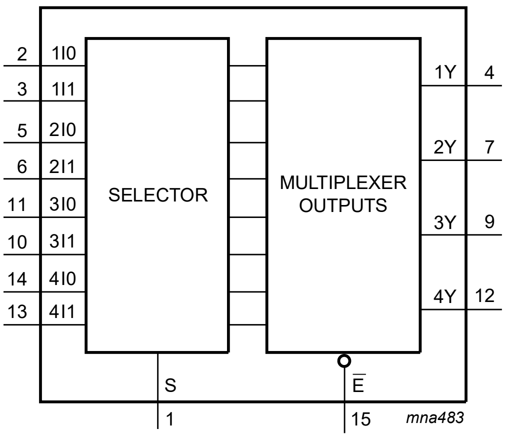


Fig. 3. Functional diagram

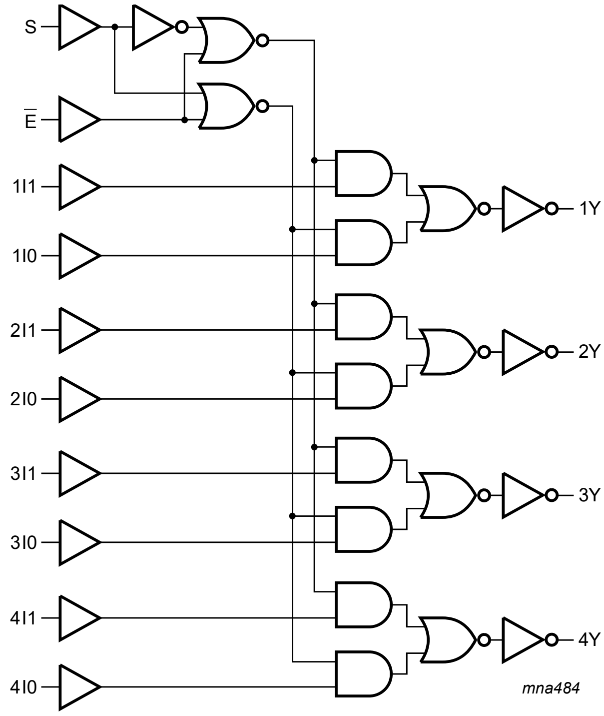


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

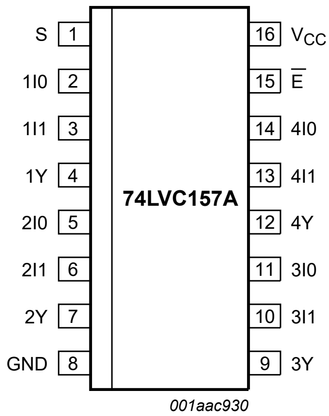
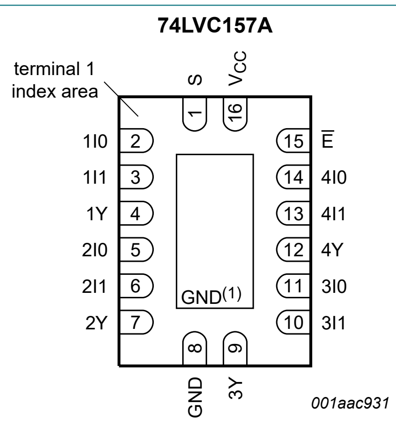


Fig. 5. Pin configuration for SO16 and TSSOP16



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 6. Pin configuration for DHVQFN16

All information provided in this document is subject to legal disclaimers.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0	2	data input from source 0
1I1	3	data input from source 1
1Y	4	multiplexer output
2I0	5	data input from source 0
2I1	6	data input from source 1
2Y	7	multiplexer output
GND	8	ground (0 V)
3Y	9	multiplexer output
3I1	10	data input from source 1
3I0	11	data input from source 0
4Y	12	multiplexer output
4I1	13	data input from source 1
4I0	14	data input from source 0
$\overline{E}$	15	enable input (active LOW)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input				Output
$\overline{E}$	S	nI0	nI1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage	[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
V_O	output voltage	[2]	-0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}	-	-	0.65 x V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.35 x V_{CC}	-	0.35 x V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.2	-	-	V_{CC} - 0.3	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = -18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 0.6 V; V_{CC} = 2.7 V to 3.6 V; I_O = 0 A	-	5	500	-	5000	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

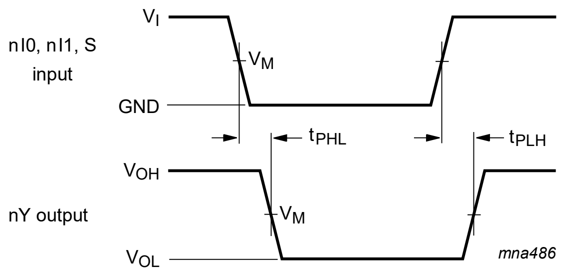
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nI0, nI1 to nY; see Fig. 7	[2]						
		V_{CC} = 1.2 V		-	16	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.0	4.8	10.2	1.0	11.8	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	2.8	5.8	1.5	6.7	ns
		V_{CC} = 2.7 V		1.0	2.9	5.9	1.0	7.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.5	5.2	1.0	6.5	ns
		$\overline{E}$ to nY; see Fig. 8	[2]						
		V_{CC} = 1.2 V		-	17	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		0.5	4.8	12.8	0.5	14.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	2.8	7.2	1.5	8.3	ns
		V_{CC} = 2.7 V		1.0	2.9	7.8	1.0	10.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.6	6.5	1.0	8.5	ns
		S to nY; see Fig. 7	[2]						
		V_{CC} = 1.2 V		-	16	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V		1.0	5.1	12.4	1.0	14.3	ns
		V_{CC} = 2.3 V to 2.7 V		1.5	3.0	7.0	1.5	8.1	ns
		V_{CC} = 2.7 V		1.0	3.1	7.3	1.0	9.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.7	6.3	1.0	8.0	ns
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC}	[4]						
		V_{CC} = 1.65 V to 1.95 V		-	9.4	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V		-	12.8	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V		-	15.9	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
N = number of inputs switching
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

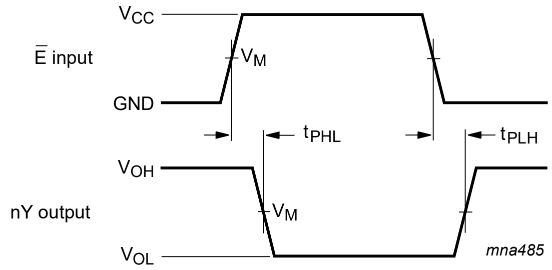
10.1. Waveforms and test circuit



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V; V_M = 0.5 x V_{CC} at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

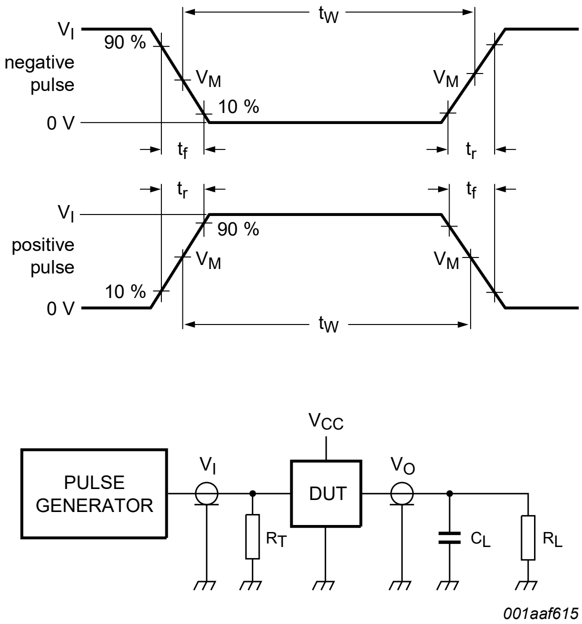
Fig. 7. Data inputs (nI0, nI1) and common data select input (S) to output (nY) propagation delays



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V; V_M = 0.5 x V_{CC} at V_{CC} < 2.7 V.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Enable input ($\overline{E}$) to output (nY) propagation delays



Test data is given in Table 8. Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

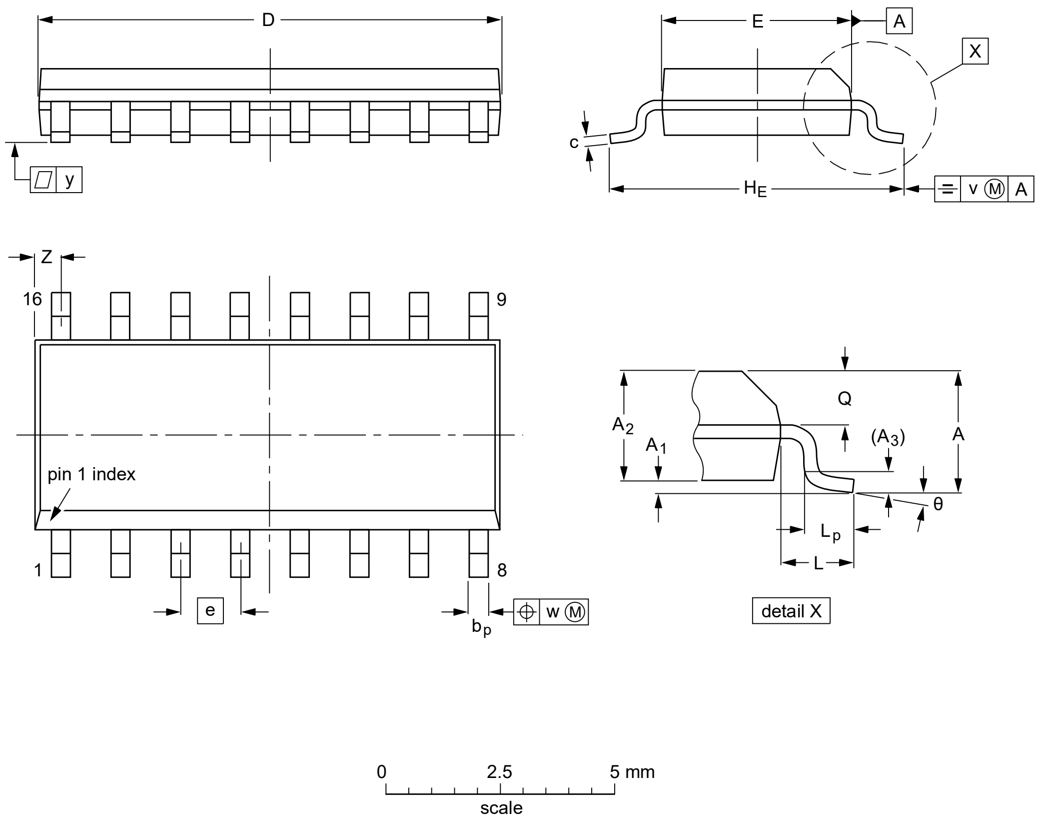
Fig. 9. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

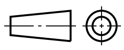
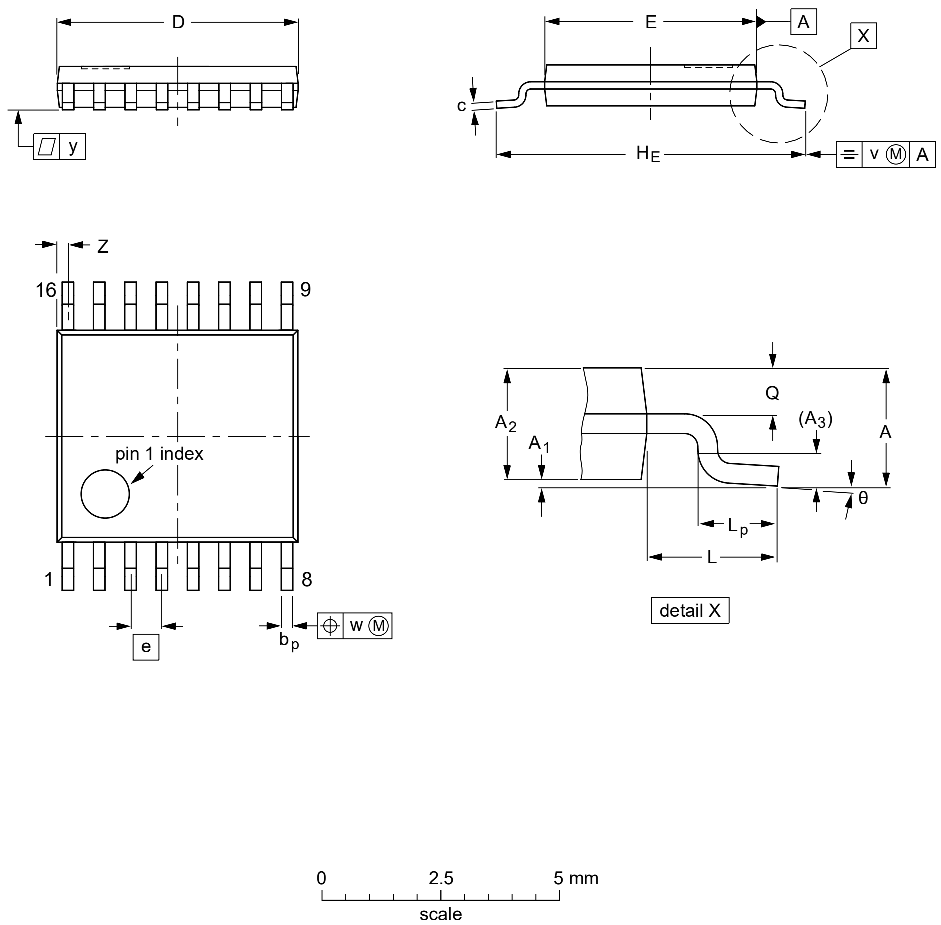
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

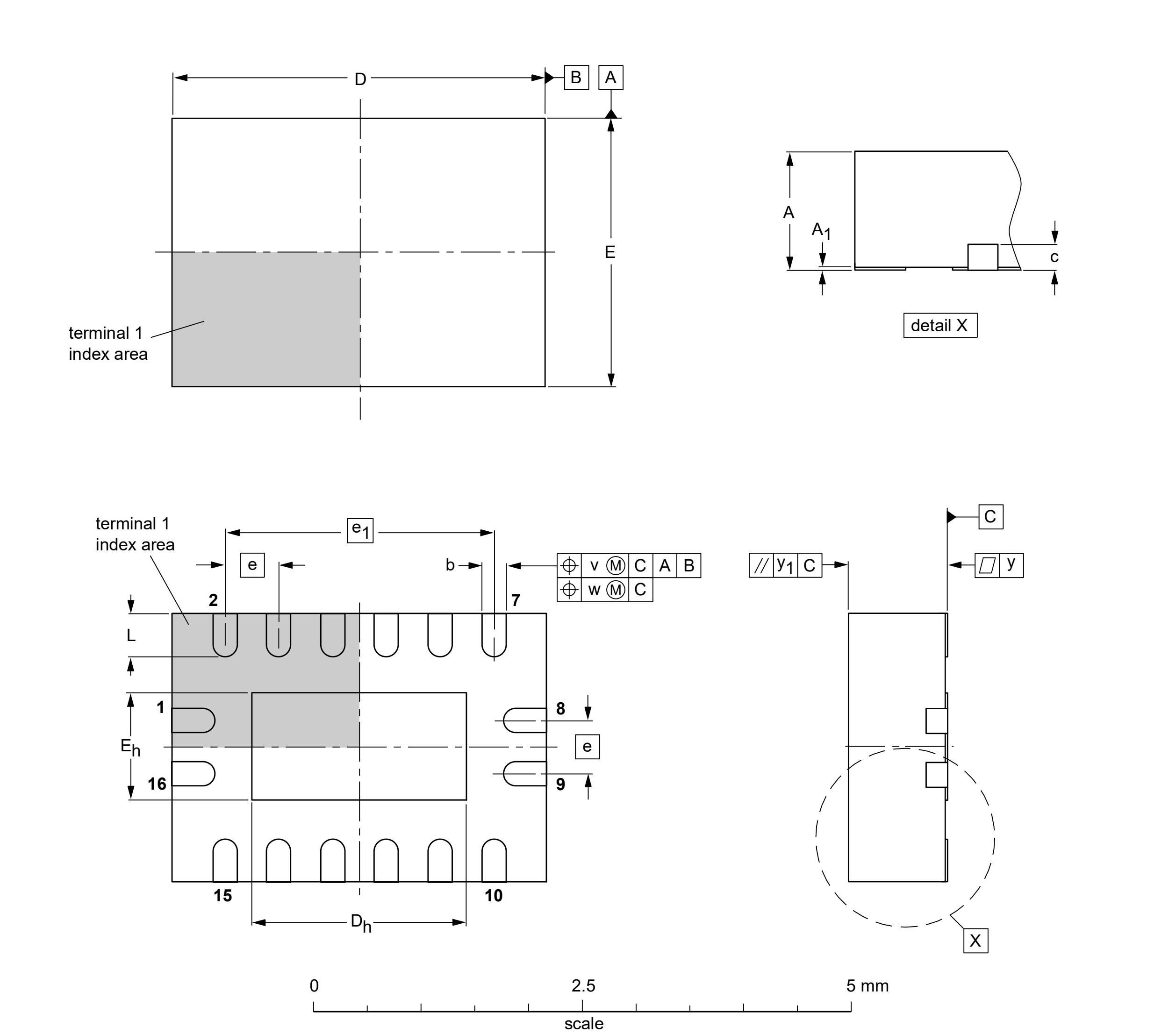
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 12. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC157A_Q100 v.3	20200319	Product data sheet	-	74LVC157A_Q100 v.2
Modifications:	• Table 4: Derating values for P_{tot} total power dissipation updated. • Type number 74LVC157ADB-Q100 removed.			
74LVC157A_Q100 v.2	20130502	Product data sheet	-	74LVC157A_Q100 v.1
Modifications:	• 74LVC157ADB-Q100 added.-			
74LVC157A_Q100 v.1	20120807	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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