



74HC4351; 74HCT4351

8-channel analog multiplexer/demultiplexer with latch

Rev. 6 — 25 July 2024

Product data sheet

1. General description

The 74HC4351; 74HCT4351 is a single-pole octal-throw analog switch (SP8T) suitable for use in analog or digital 8:1 multiplexer/demultiplexer applications. The switch features three digital select inputs (S0 to S2), eight independent inputs/outputs (Yn), a common input/output (Z) and two digital enable inputs (E1 and E2). With E1 LOW and E2 HIGH, one of the eight switches is selected (low impedance ON-state) by S0 to S2. The data at the select inputs may be latched by using the latch enable input (\overline{LE}). When \overline{LE} is HIGH the latch is transparent. When $\overline{E1}$ is HIGH or E2 is LOW all 8 analog switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide analog input voltage range from -5 V to +5 V
- Complies with JEDEC standard no. 7A
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC} - V_{EE} = 4.5$ V
 - 70 Ω (typical) at $V_{CC} - V_{EE} = 6.0$ V
 - 60 Ω (typical) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical 'break before make' built-in
- Address latches provided
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4351D 74HCT4351D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HC4351PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

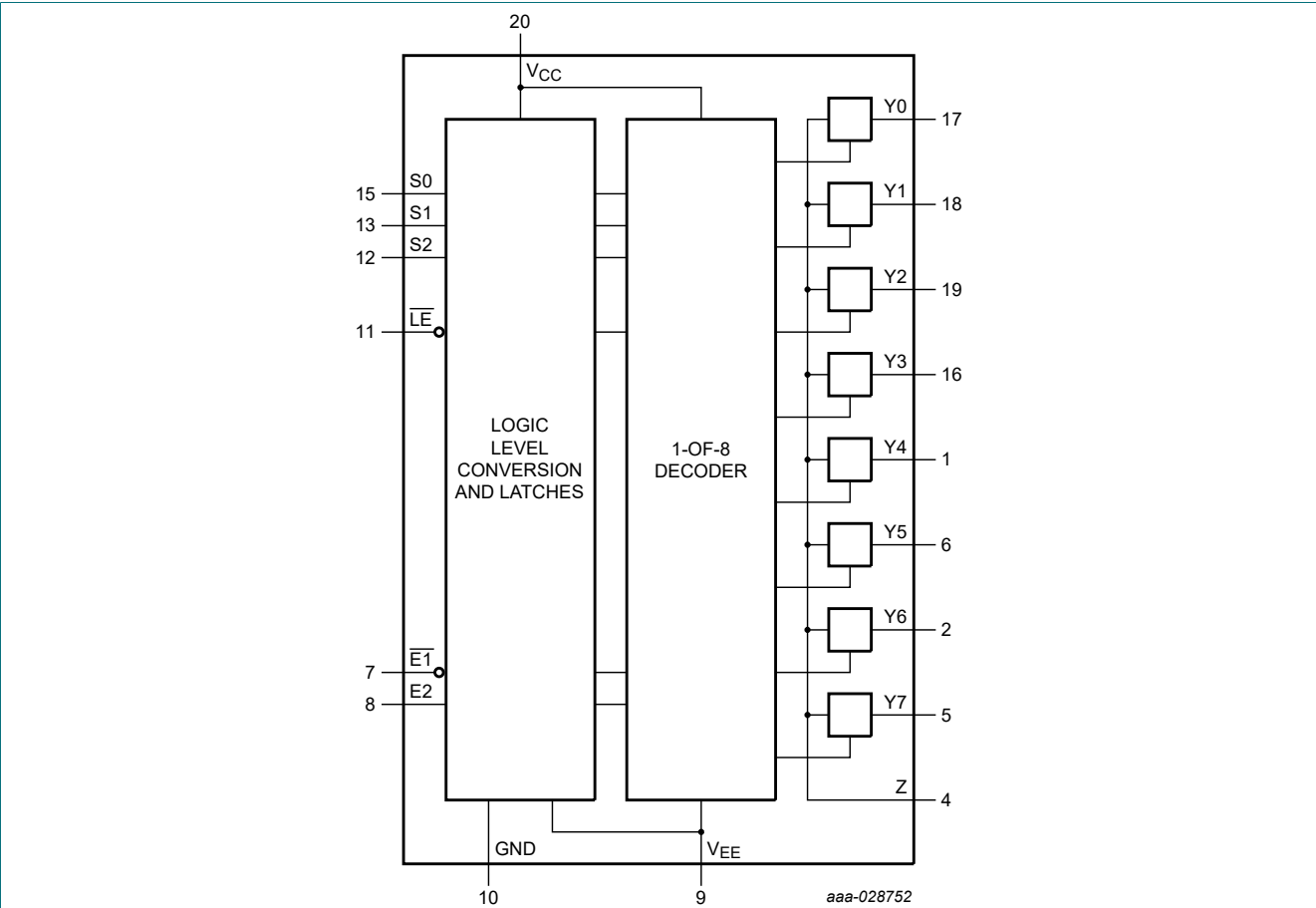


Fig. 1. Functional diagram

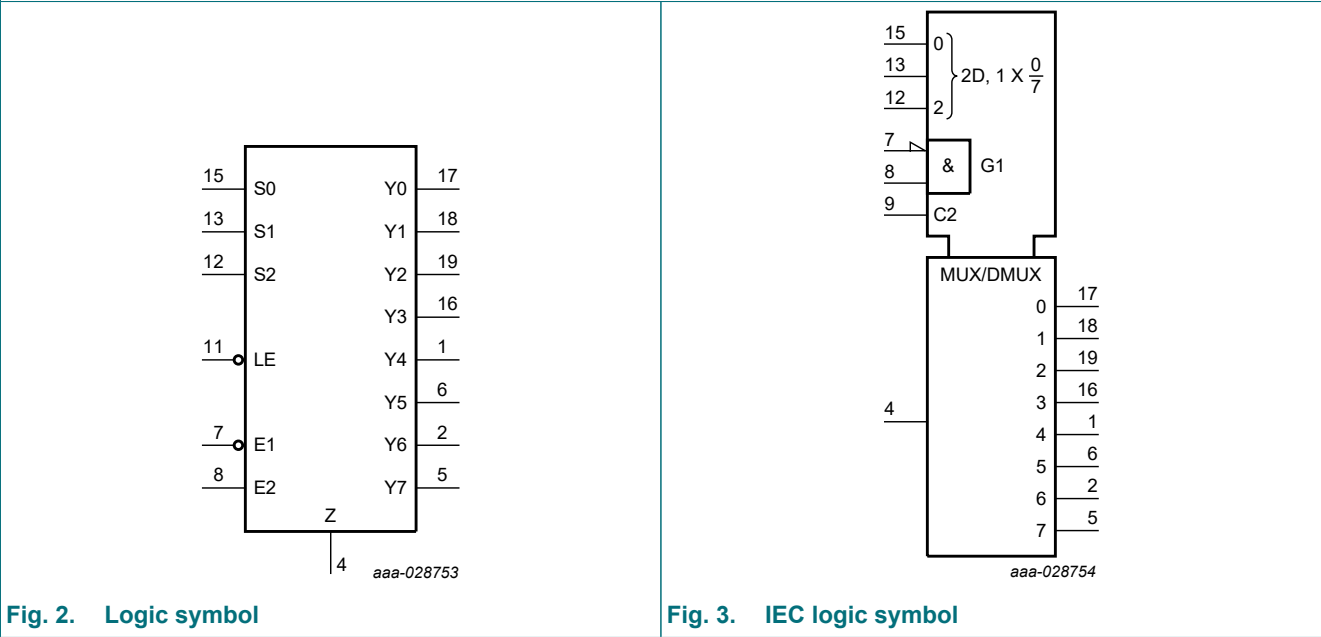


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

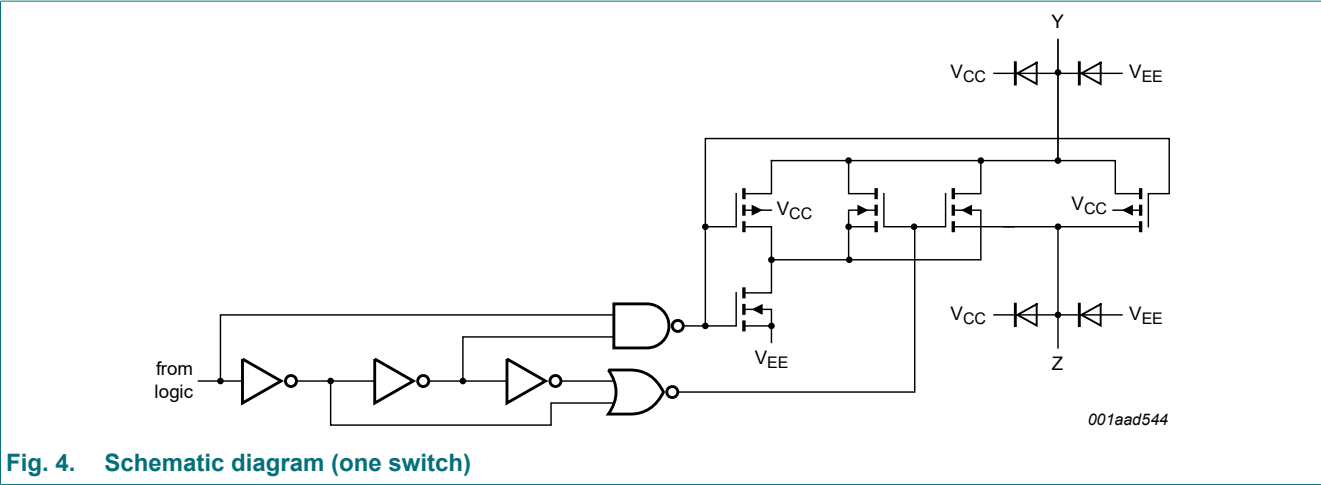
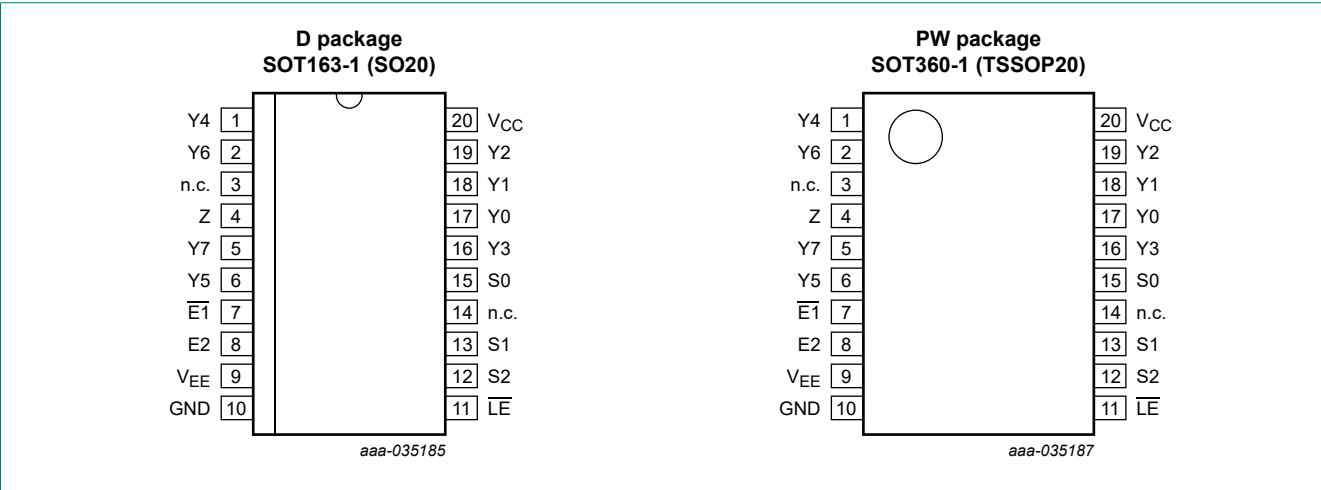


Fig. 4. Schematic diagram (one switch)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
E1	7	enable input (active LOW)
E2	8	enable input (active HIGH)
LE	11	latch enable input (active LOW)
S0, S1, S2	15, 13, 12	select inputs
Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	17, 18, 19, 16, 1, 6, 2, 5	independent input or output
Z	4	common output or input
VEE	9	supply voltage
GND	10	ground (0 V)
VCC	20	supply voltage
n.c.	3, 14	not connected

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↓ = HIGH-to-LOW LE transition.

Input						Channel ON
E1	E2	LE	S2	S1	S0	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	Y0
L	H	H	L	L	H	Y1
L	H	H	L	H	L	Y2
L	H	H	L	H	H	Y3
L	H	H	H	L	L	Y4
L	H	H	H	L	H	Y5
L	H	H	H	H	L	Y6
L	H	H	H	H	H	Y7
L	H	L	X	X	X	last selected channel "ON"
X	X	↓	X	X	X	select channels latched

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	[1]	-0.5	+11.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{SK}	switch clamping current	V _{SW} < -0.5 V or V _{SW} > V _{CC} + 0.5 V	-	±20	mA
I _{SW}	switch current	-0.5 V < V _{SW} < V _{CC} + 0.5 V	-	±25	mA
I _{EE}	supply current		-	±20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW
P	power dissipation	per switch	-	100	mW

- [1] To avoid drawing V_{CC} current out of terminal Z, when switch current flows into terminals Y_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n. In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or V_{EE}.
- [2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4351			74HCT4351			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage	see Fig. 5 and Fig. 6							
		V _{CC} - GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V _{CC} - V _{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V
V _I	input voltage		GND	-	V _{CC}	GND	-	V _{CC}	V
V _{SW}	switch voltage		V _{EE}	-	V _{CC}	V _{EE}	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V _{CC} = 10.0 V	-	-	31	-	-	-	ns/V

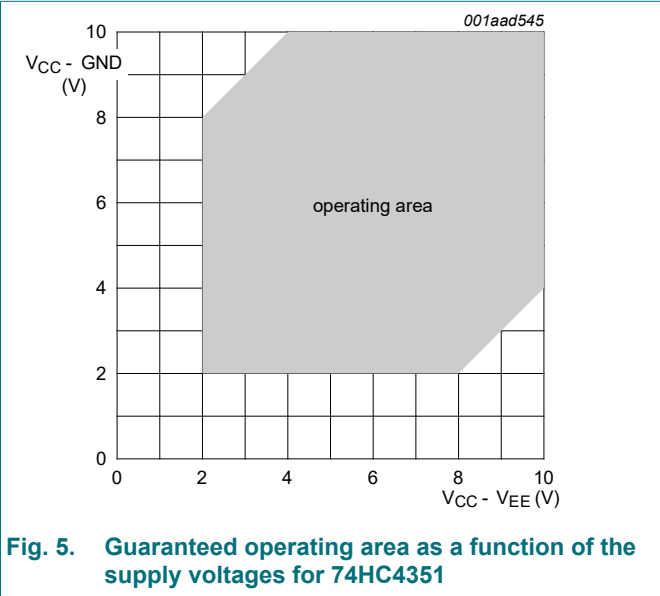


Fig. 5. Guaranteed operating area as a function of the supply voltages for 74HC4351

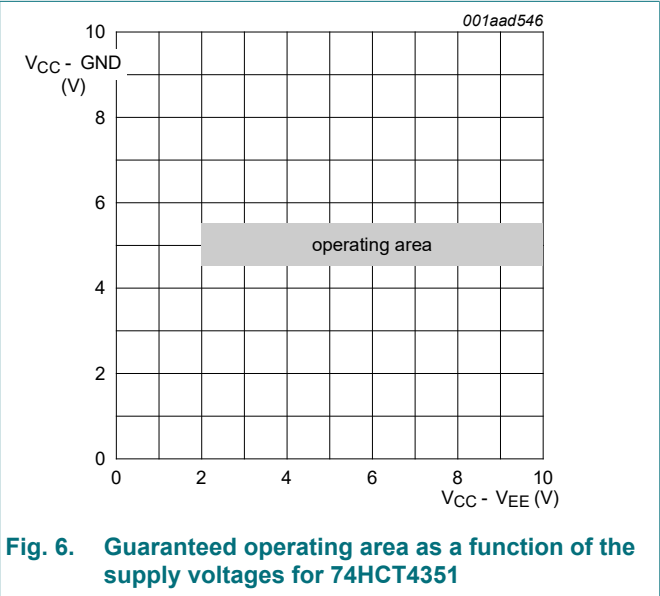


Fig. 6. Guaranteed operating area as a function of the supply voltages for 74HCT4351

10. Static characteristics

Table 6. R_{ON} resistance per latch for 74HC4351 and 74HCT4351

For test circuit, see Fig. 7

For 74HC4351: V_I = V_{IH} or V_{IL}; V_{CC} - GND or V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

For 74HCT4351: V_I = V_{IH} or V_{IL}; V_{CC} - GND = 4.5 V and 5.5 V, V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _{is} = V _{CC} to V _{EE} [1]								
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 µA [2]	-	-	-	-	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	100	180	-	225	-	270	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	90	160	-	200	-	240	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 µA	-	70	130	-	165	-	195	Ω
R _{ON(rail)}	ON resistance (rail)	V _{is} = V _{EE} [1]								
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 µA [2]	-	150	-	-	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	80	140	-	175	-	210	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	70	120	-	150	-	180	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 µA	-	60	105	-	130	-	160	Ω
		V _{is} = V _{CC} [1]								
		V _{CC} = 2.0 V; V _{EE} = 0 V; I _{SW} = 100 µA [2]	-	150	-	-	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	90	160	-	200	-	240	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V; I _{SW} = 1000 µA	-	80	140	-	175	-	210	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V; I _{SW} = 1000 µA	-	65	120	-	150	-	180	Ω
ΔR _{ON}	ON resistance mismatch between channels	V _{is} = V _{CC} to V _{EE} [1]								
		V _{CC} = 2.0 V; V _{EE} = 0 V [2]	-	-	-	-	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	9	-	-	-	-	-	Ω
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	8	-	-	-	-	-	Ω
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	6	-	-	-	-	-	Ω

[1] V_{is} is the input voltage at a Yn or Z terminal, whichever is assigned as an input.
[2] When supply voltages (V_{CC} - V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.

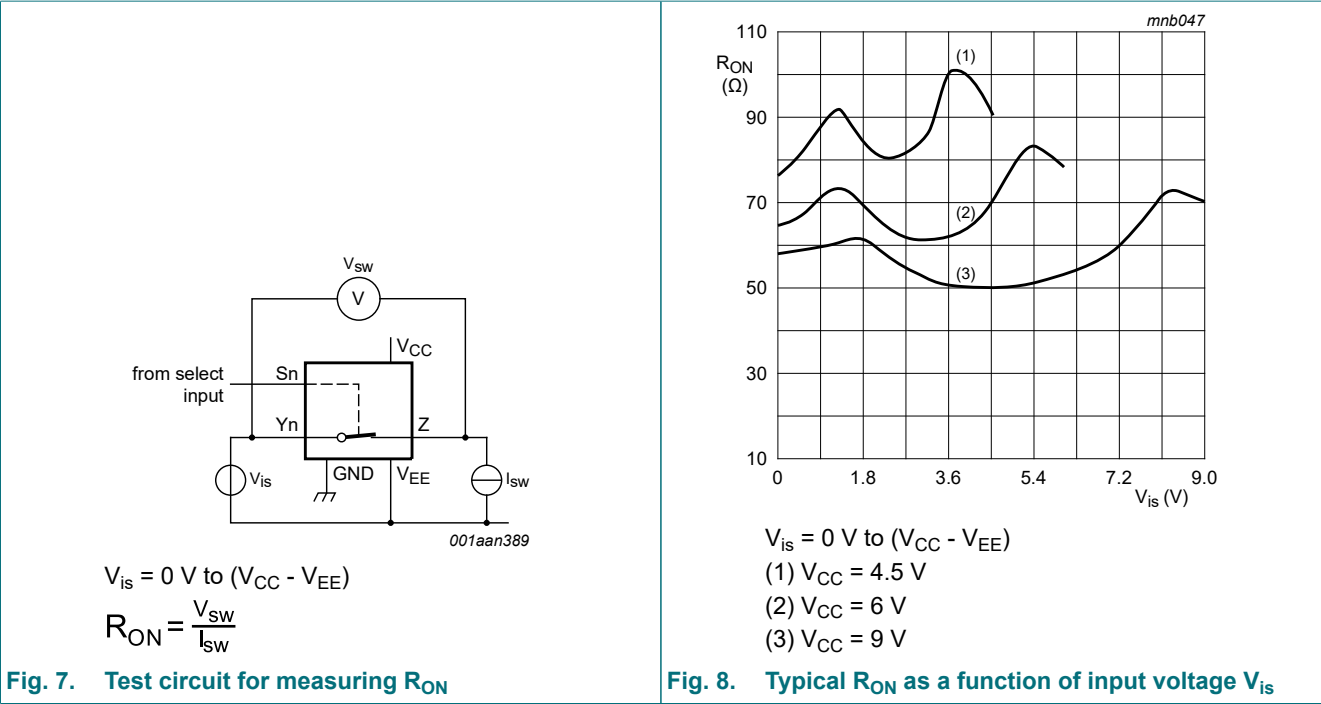


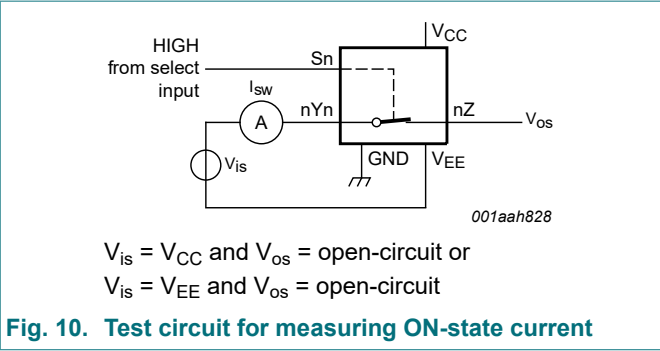
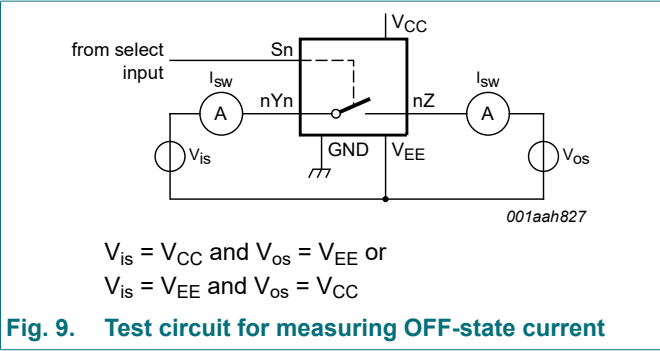
Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V);
 V_{is} is the input voltage at pins Y_n or Z , whichever is assigned as an input;
 V_{os} is the output voltage at pins Z or Y_n , whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4351										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
		V _{CC} = 9.0 V	6.3	4.7	-	6.3	-	6.3	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
		V _{CC} = 9.0 V	-	4.3	2.7	-	2.7	-	2.7	V
I _I	input leakage current	V _{EE} = 0 V; V _I = V _{CC} or GND								
		V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
		V _{CC} = 10.0 V	-	-	±0.2	-	±2.0	-	±2.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 9								
		per channel	-	-	±0.1	-	±1.0	-	±1.0	µA
		all channels	-	-	±0.4	-	±4.0	-	±4.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 10	-	-	±0.4	-	±4.0	-	±4.0	µA

8-channel analog multiplexer/demultiplexer with latch

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{CC}	supply current	V _{EE} = 0 V; V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}								
		V _{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	µA
		V _{CC} = 10.0 V	-	-	16.0	-	160.0	-	320.0	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
C _{sw}	switch capacitance	independent pins Yn	-	5	-	-	-	-	-	pF
		common pins Z	-	25	-	-	-	-	-	pF
74HCT4351										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 9								
		per channel	-	-	±0.1	-	±1.0	-	±1.0	µA
		all channels	-	-	±0.4	-	±4.0	-	±4.0	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 10.0 V; V _{EE} = 0 V; V _I = V _{IH} or V _{IL} ; V _{SW} = V _{CC} - V _{EE} ; see Fig. 10	-	-	±0.4	-	±4.0	-	±4.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{is} = V _{EE} or V _{CC} ; V _{os} = V _{CC} or V _{EE}								
		V _{CC} = 5.5 V; V _{EE} = 0 V	-	-	8.0	-	80.0	-	160.0	µA
		V _{CC} = 5.0 V; V _{EE} = -5.0 V	-	-	16.0	-	160.0	-	320.0	µA
ΔI _{CC}	additional supply current	per input; other inputs at V _{CC} or GND; V _I = V _{CC} - 2.1 V; V _{CC} = 4.5 V to 5.5 V; V _{EE} = 0 V								
		inputs $\overline{E}1$, E2 and Sn	-	50	180	-	225	-	245	µA
		input \overline{LE}	-	150	540	-	675	-	735	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
C _{sw}	switch capacitance	independent pins Yn	-	5	-	-	-	-	-	pF
		common pins Z	-	25	-	-	-	-	-	pF



11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; for test circuit see Fig. 14.
 V_{is} is the input voltage at pins Yn or Z, whichever is assigned as an input;
 V_{os} is the output voltage at pins Z or Yn, whichever is assigned as an output.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4351										
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Fig. 11 [1]								
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	5	12	-	15	-	18	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	4	10	-	13	-	15	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	4	8	-	10	-	12	ns
t _{on}	turn-ON time	E1 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	85	300	-	375	-	450	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	31	60	-	75	-	90	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	25	51	-	64	-	77	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	28	55	-	69	-	83	ns
		E2 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	85	300	-	375	-	450	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	31	60	-	75	-	90	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	25	51	-	64	-	77	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	25	55	-	69	-	83	ns
		LE to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	91	300	-	375	-	450	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	33	60	-	75	-	90	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	26	51	-	64	-	77	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	27	55	-	69	-	83	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 2.0 V; V _{EE} = 0 V	-	88	300	-	375	-	450	ns
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	32	60	-	75	-	90	ns
		V _{CC} = 6.0 V; V _{EE} = 0 V	-	26	51	-	64	-	77	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	25	50	-	63	-	75	ns

8-channel analog multiplexer/demultiplexer with latch

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{off}	turn-OFF time	$\overline{\text{E1}}$ to V_{OS} ; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 12								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	69	250	-	315	-	375	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	25	50	-	63	-	75	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	20	43	-	54	-	64	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	-	20	40	-	50	-	60	ns
		E2 to V_{OS} ; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 12								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	72	250	-	315	-	375	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	26	50	-	63	-	75	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	21	43	-	54	-	64	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	-	19	40	-	50	-	60	ns
		$\overline{\text{LE}}$ to V_{OS} ; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 12								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	83	275	-	345	-	415	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	30	55	-	69	-	83	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	24	47	-	59	-	71	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	-	26	45	-	56	-	68	ns
		Sn to V_{OS} ; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 12								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	80	275	-	345	-	415	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	29	55	-	69	-	83	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	-	23	47	-	59	-	71	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	-	24	48	-	60	-	72	ns
t_{su}	set-up time	Sn to $\overline{\text{LE}}$; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 13								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	60	17	-	-	75	-	90	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	12	6	-	-	15	-	18	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	10	5	-	-	13	-	15	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	18	9	-	-	23	-	27	ns
t_{hold}	hold time	Sn to $\overline{\text{LE}}$; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 13								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	5	-8	-	-	5	-	5	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	5	-3	-	-	5	-	5	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	5	-2	-	-	5	-	5	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	5	-4	-	-	5	-	5	ns
$t_{\text{WH(min)}}$	minimum pulse width HIGH	$\overline{\text{LE}}$; $R_{\text{L}} = 1 \text{ k}\Omega$; see Fig. 13								
		$V_{\text{CC}} = 2.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	100	11	-	-	125	-	150	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	20	1	-	-	25	-	30	ns
		$V_{\text{CC}} = 6.0 \text{ V}$; $V_{\text{EE}} = 0 \text{ V}$	17	3	-	-	21	-	26	ns
		$V_{\text{CC}} = 4.5 \text{ V}$; $V_{\text{EE}} = -4.5 \text{ V}$	25	7	-	-	31	-	38	ns
C_{pd}	power dissipation capacitance	per switch; $V_{\text{I}} = \text{GND}$ to V_{CC} [2]	-	25	-	-	-	-	-	pF
C_{sw}	switch capacitance	maximum								
		independent (Y_{n})	-	5	-	-	-	-	-	pF
		common (Z)	-	25	-	-	-	-	-	pF

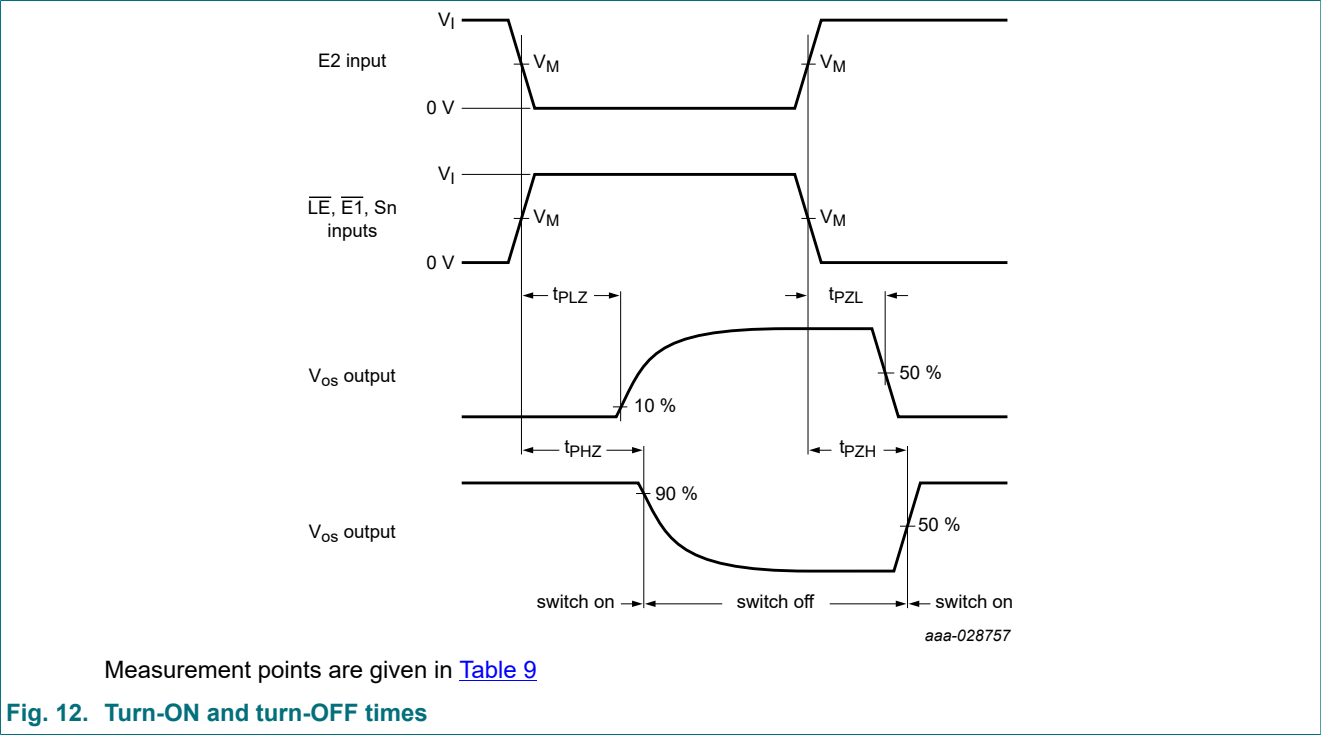
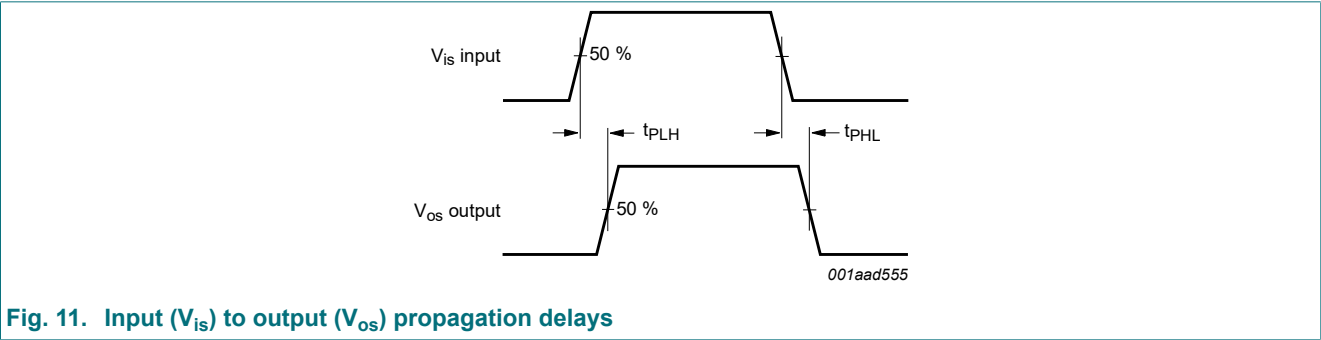
8-channel analog multiplexer/demultiplexer with latch

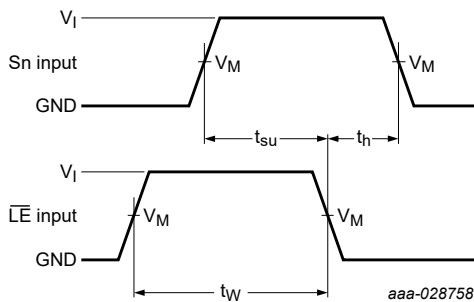
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4351										
t _{pd}	propagation delay	V _{is} to V _{os} ; R _L = ∞ Ω; see Fig. 11 [1]								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	6	12	-	15	-	18	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	4	8	-	10	-	12	ns
t _{on}	turn-ON time	E1 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	40	75	-	94	-	113	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	31	60	-	75	-	90	ns
		E2 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	35	70	-	88	-	105	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	26	50	-	63	-	75	ns
		LE to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	42	75	-	94	-	113	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	37	60	-	75	-	90	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	39	75	-	94	-	113	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	30	60	-	75	-	90	ns
t _{off}	turn-OFF time	E1 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	27	55	-	69	-	83	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	20	40	-	50	-	60	ns
		E2 to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	32	60	-	75	-	90	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	26	50	-	63	-	75	ns
		LE to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	33	60	-	75	-	90	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	30	55	-	69	-	83	ns
		Sn to V _{os} ; R _L = 1 kΩ; see Fig. 12								
		V _{CC} = 4.5 V; V _{EE} = 0 V	-	33	65	-	81	-	98	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	29	55	-	69	-	83	ns
t _{su}	set-up time	Sn to LE; R _L = 1 kΩ; see Fig. 13								
		V _{CC} = 4.5 V; V _{EE} = 0 V	12	6	-	-	15	-	18	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	14	7	-	-	18	-	21	ns
t _{hold}	hold time	Sn to LE; R _L = 1 kΩ; see Fig. 13								
		V _{CC} = 4.5 V; V _{EE} = 0 V	5	-1	-	-	5	-	5	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	5	-2	-	-	5	-	5	ns
t _{WH(min)}	minimum pulse width HIGH	LE; R _L = 1 kΩ; see Fig. 13								
		V _{CC} = 4.5 V; V _{EE} = 0 V	25	13	-	-	31	-	38	ns
		V _{CC} = 4.5 V; V _{EE} = -4.5 V	25	13	-	-	31	-	38	ns
C _{pd}	power dissipation capacitance	per switch; V _I = GND to V _{CC} - 1.5 V [2]	-	25	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{sw}	switch capacitance	maximum								
		independent (Y _n)	-	5	-	-	-	-	-	pF
		common (Z)	-	25	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 N = number of inputs switching;
 $\Sigma\{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;
 C_L = output load capacitance in pF;
 C_{sw} = switch capacitance in pF;
 V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit



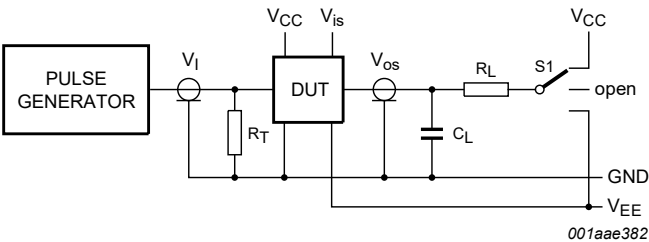
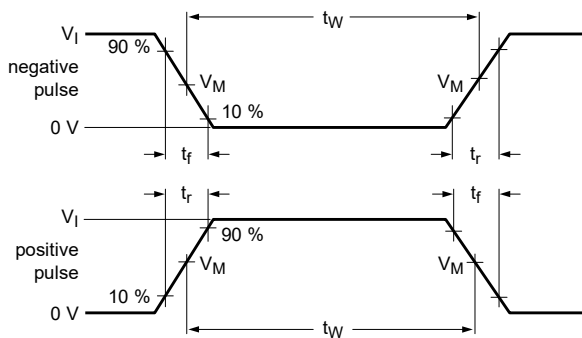


Measurement points are given in [Table 9](#)

Fig. 13. Set-up and hold times from Sn inputs to LE input, and minimum pulse width of LE.

Table 9. Measurement points

Type	Input		Output
	VI	VM	VM
74HC4351	GND to VCC	0.5 × VCC	0.5 × VCC
74HCT4351	GND to 3 V	1.3 V	1.3 V



Test data is given in [Table 10](#):

Definitions test circuit:

RT = Termination resistance should be equal to the output impedance Zo of the pulse generator;

CL = Load capacitance including jig and probe capacitance;

RL = Load resistance;

S1 = Test selection switch.

Fig. 14. Test circuit for measuring switching times

Table 10. Test data

Test	Input				Load		S1 position
	V _I	V _{is}	t _r , t _f		C _L	R _L	
			at f _{max}	other [1]			
t _{PZH} , t _{PHZ}	[2]	V _{CC}	< 2 ns	6 ns	50 pF	1 kΩ	V _{EE}
t _{PZL} , t _{PLZ}	[2]	V _{EE}	< 2 ns	6 ns	50 pF	1 kΩ	V _{CC}
Other	[2]	pulse	< 2 ns	6 ns	50 pF	1 kΩ	open

[1] t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:
For 74HC4351: V_I = V_{CC}
For 74HCT4351: V_I = 3 V

11.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics
Recommended conditions and typical values; $GND = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$ unless stated otherwise.
 V_{is} is the input voltage at pins Y_n or Z , whichever is assigned as an input.
 V_{os} is the output voltage at pins Y_n or Z , whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	$f_i = 1\text{ kHz}$; $R_L = 10\text{ k}\Omega$; see Fig. 15				
		$V_{is} = 4.0\text{ V (p-p)}$; $V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$	-	0.04	-	%
		$V_{is} = 8.0\text{ V (p-p)}$; $V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	0.02	-	%
		$f_i = 10\text{ kHz}$; $R_L = 10\text{ k}\Omega$; see Fig. 15				
		$V_{is} = 4.0\text{ V (p-p)}$; $V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$	-	0.12	-	%
		$V_{is} = 8.0\text{ V (p-p)}$; $V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	0.06	-	%
α_{iso}	isolation (OFF-state)	$R_L = 600\text{ }\Omega$; $f_i = 1\text{ MHz}$; see Fig. 16				
		$V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$ [1]	-	-50	-	dB
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$ [1]	-	-50	-	dB
V_{ct}	crosstalk voltage	between control and any switch (peak-to-peak value); $R_L = 600\text{ }\Omega$; $f_i = 1\text{ MHz}$; $\overline{E1}$, $E2$ or Sn square wave between V_{CC} and GND ; $t_r = t_f = 6\text{ ns}$; see Fig. 17				
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = 0\text{ V}$	-	120	-	mV
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$	-	220	-	mV
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 50\text{ }\Omega$; $C_L = 10\text{ pF}$ see Fig. 18				
		$V_{CC} = 2.25\text{ V}$; $V_{EE} = -2.25\text{ V}$ [2]	-	160	-	MHz
		$V_{CC} = 4.5\text{ V}$; $V_{EE} = -4.5\text{ V}$ [2]	-	170	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
[2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

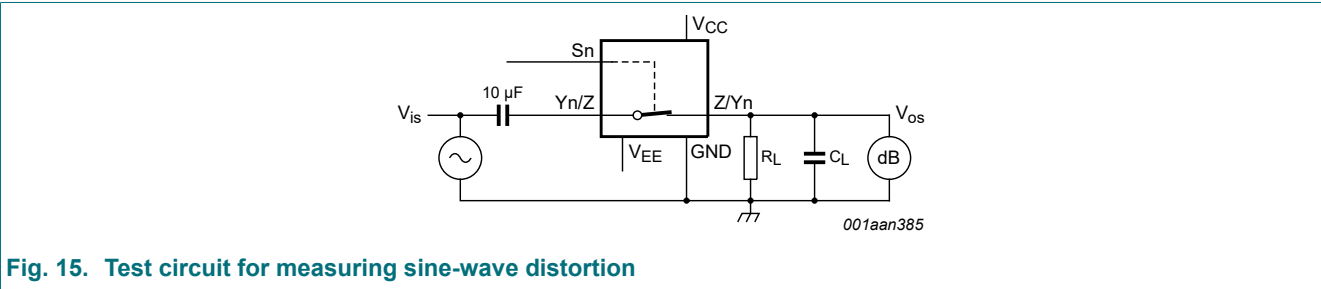
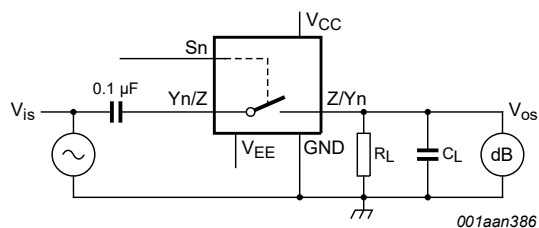
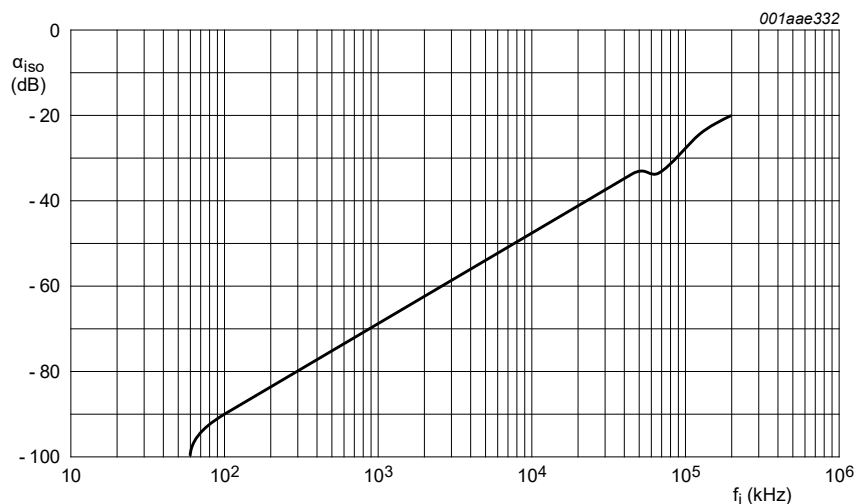


Fig. 15. Test circuit for measuring sine-wave distortion


$$V_{CC} = 4.5 \text{ V}; \text{ GND} = 0 \text{ V}; V_{EE} = -4.5 \text{ V}; R_L = 600 \text{ } \Omega; R_S = 1 \text{ k}\Omega$$

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig. 16. Test circuit for measuring isolation (OFF-state)

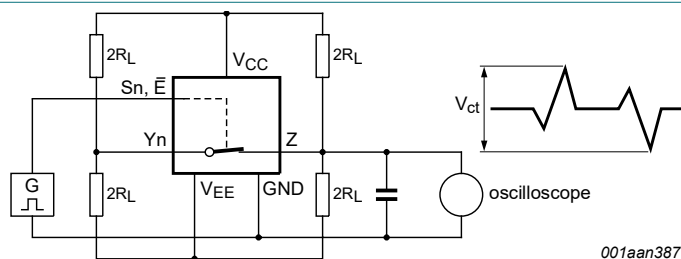
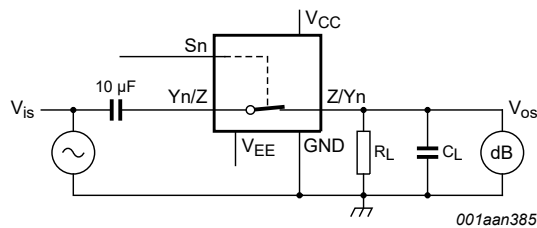
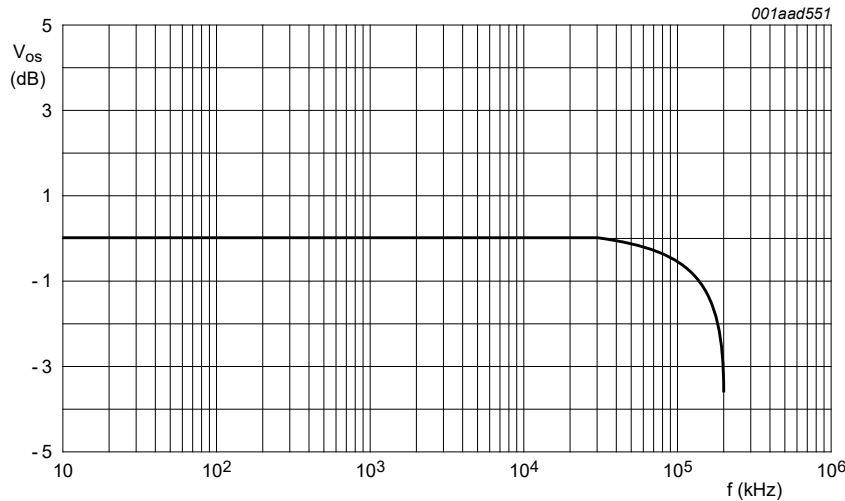


Fig. 17. Test circuit for measuring crosstalk between control input and any switch



$V_{CC} = 4.5\ \text{V}$; $\text{GND} = 0\ \text{V}$; $V_{EE} = -4.5\ \text{V}$; $R_L = 50\ \Omega$; $R_S = 1\ \text{k}\Omega$

a. Test circuit



b. Typical frequency response

Fig. 18. Test circuit for frequency response

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 19. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

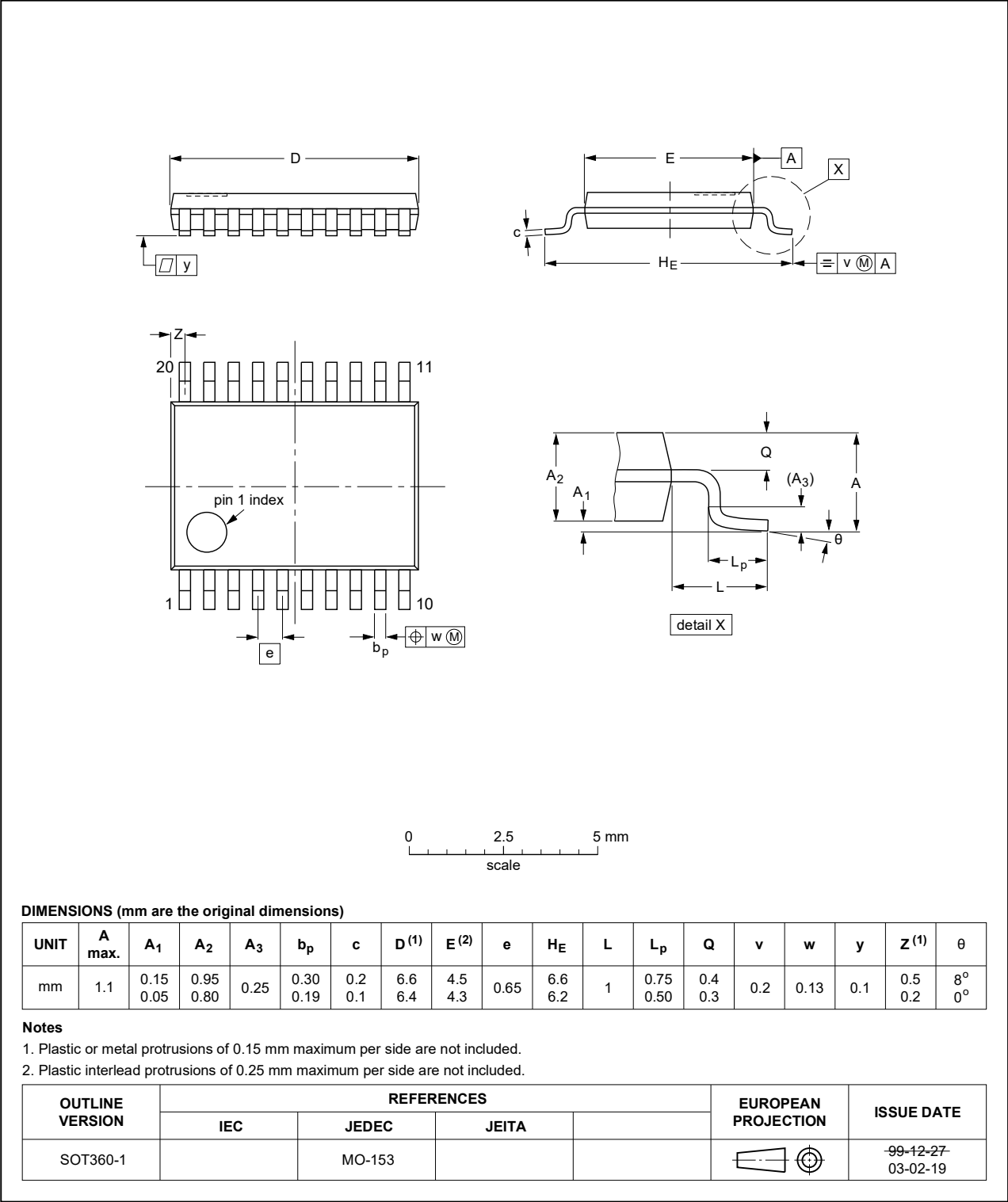


Fig. 20. Package outline SOT360-1 (TSSOP20)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4351 v.6	20240725	Product data sheet	-	74HC_HCT4351 v.5
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT4351 v.5	20231102	Product data sheet	-	74HC_HCT4351 v.4
Modifications:	<ul style="list-style-type: none">Type number 74HC4351DB (SOT339-1/SSOP20) removed.			
74HC_HCT4351 v.4	20210804	Product data sheet	-	74HC_HCT4351 v.3
Modifications:	<ul style="list-style-type: none">Type number 74HC4351PW (SOT360-1/TSSOP20) added.Type number 74HCT4351DB (SOT339-1/SSOP20) removed.Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT4351 v.3	20180709	Product data sheet	-	74HC_HCT4351 v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Type numbers 74HC4351N (SOT146-1) and 74HCT4351N (SOT146-1) removed.			
74HC_HCT4351 v.2	19901201	Product specification	-	74HC_HCT4351 v.1

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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