

# 74HC259-Q100; 74HCT259-Q100

## 8-bit addressable latch

Rev. 3 — 11 March 2024

Product data sheet

## 1. General description

The 74HC259-Q100; 74HCT259-Q100 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

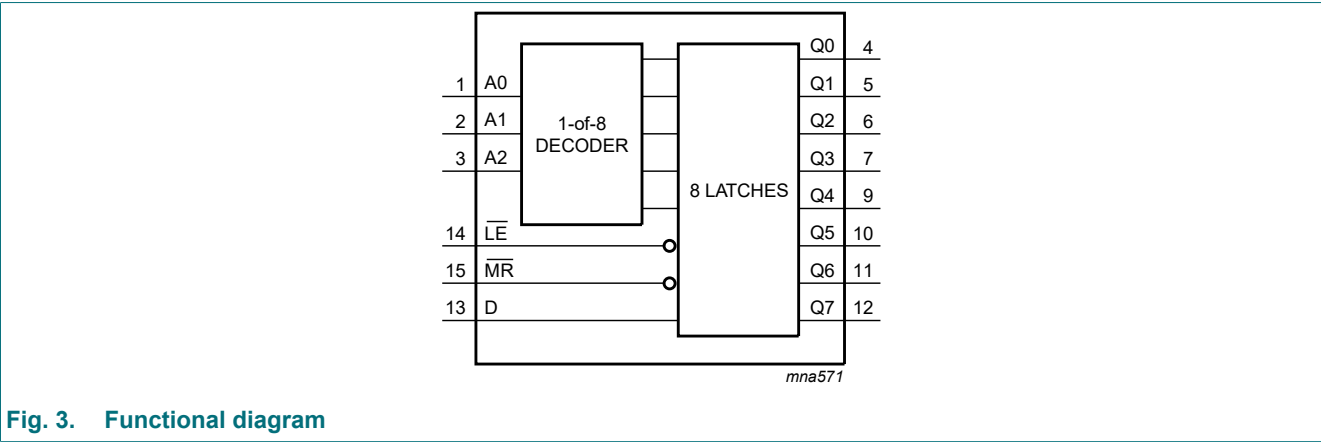
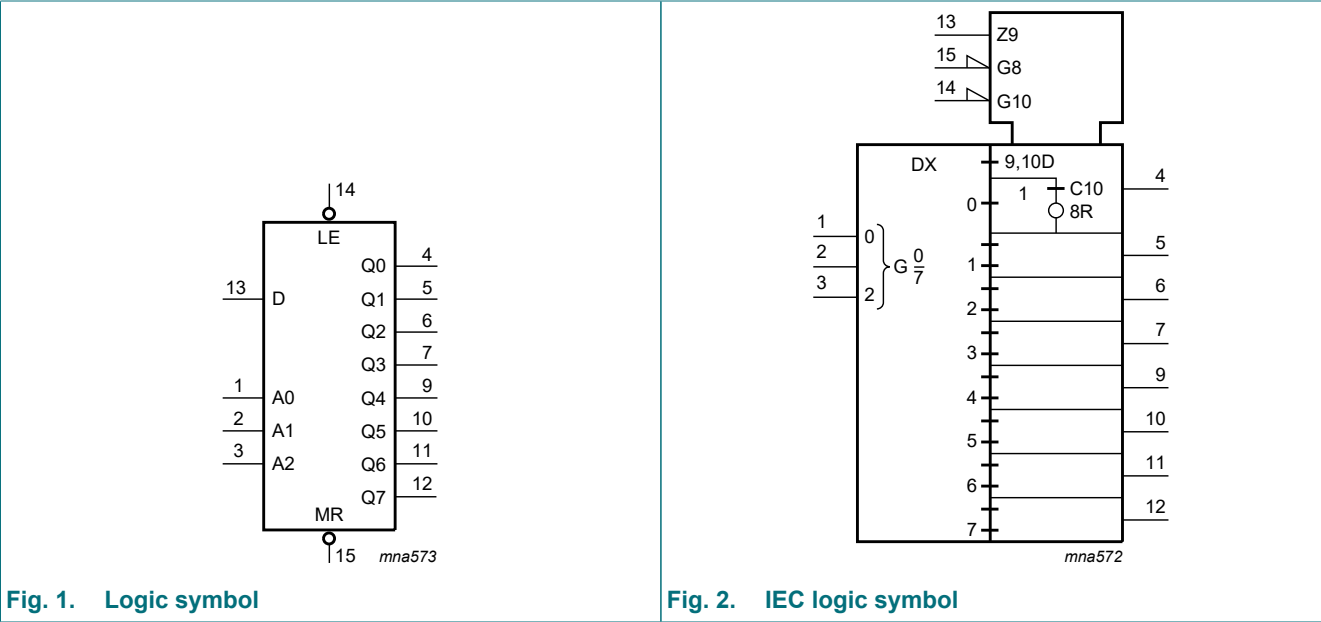
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Input levels:
  - For 74HC259-Q100: CMOS level
  - For 74HCT259-Q100: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

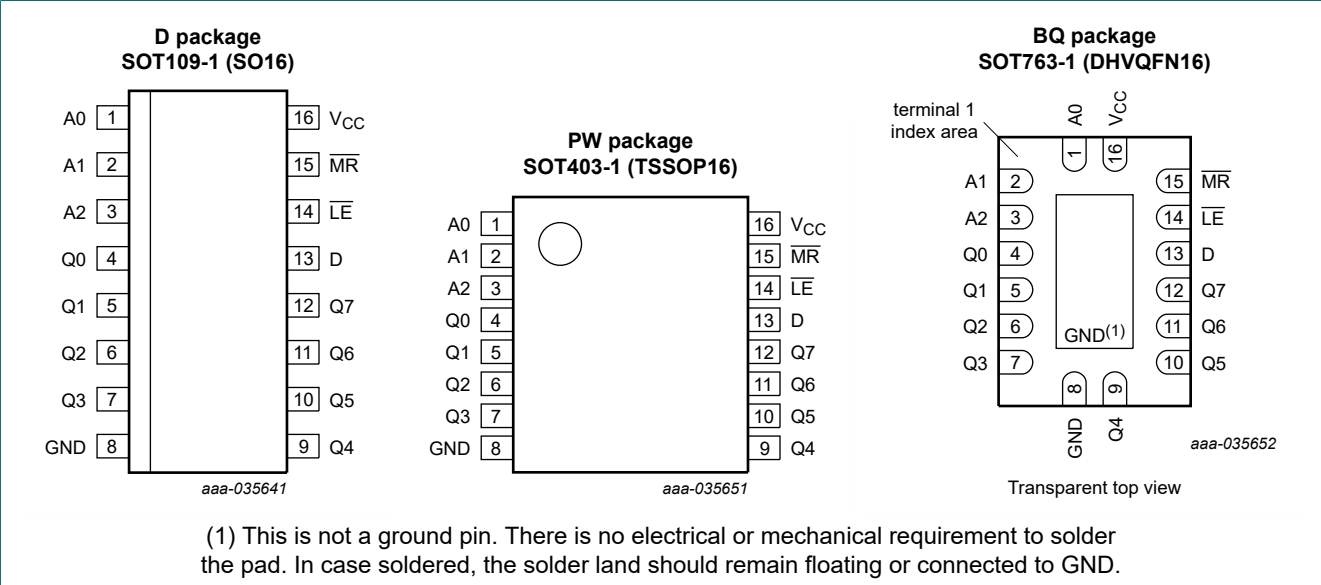
Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74HC259D-Q100</a> <a href="#">74HCT259D-Q100</a>	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">74HC259PW-Q100</a> <a href="#">74HCT259PW-Q100</a>	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>
<a href="#">74HC259BQ-Q100</a> <a href="#">74HCT259BQ-Q100</a>	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	<a href="#">SOT763-1</a>

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	address input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	4, 5, 6, 7, 9, 10, 11, 12	latch output
GND	8	ground (0 V)
D	13	data input
LE	14	latch enable input (active LOW)
MR	15	conditional reset input (active LOW)
VCC	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;  
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH  $\overline{LE}$  transition;  
q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Operating mode	Input						Output							
	MR	LE	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q = d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q = d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q = d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q = d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Memory (no action)	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
Addressable latch	H	L	d	L	L	L	Q = d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	L	q <sub>0</sub>	Q = d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q = d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q = d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q = d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q = d	q <sub>6</sub>	q <sub>7</sub>
	H	L	d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	Q = d	q <sub>7</sub>
	H	L	d	H	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	Q = d

Table 4. Operating mode select table

H = HIGH voltage level; L = LOW voltage level.

LE	MR	Mode
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	+70	mA
I <sub>GND</sub>	ground current		-70	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		SOT109-1 (SO16) [2]	-	500	mW
		SOT403-1 (TSSOP16) [3]			
		SOT763-1 (DHVQFN16) [4]			

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
[2] For SOT109-1 (SO16) package: P<sub>tot</sub> derates linearly with 12.4 mW/K above 110 °C.  
[3] For SOT403-1 (TSSOP16) package: P<sub>tot</sub> derates linearly with 8.5 mW/K above 91 °C.  
[4] For SOT763-1 (DHVQFN16) package: P<sub>tot</sub> derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC259-Q100			74HCT259-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC259-Q100										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-	160	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT259-Q100										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		pin An, $\overline{\text{LE}}$	-	150	540	-	675	-	735	µA
		pin D	-	120	432	-	540	-	588	µA
		pin MR	-	75	270	-	338	-	368	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74HC259-Q100										
t <sub>pd</sub>	propagation delay	D to Qn; see Fig. 4 [2]								
		V <sub>CC</sub> = 2.0 V	-	58	185	-	230	-	280	ns
		V <sub>CC</sub> = 4.5 V	-	21	37	-	46	-	56	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	18	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	17	31	-	39	-	48	ns
		An to Qn; see Fig. 5 [2]								
		V <sub>CC</sub> = 2.0 V	-	58	185	-	230	-	280	ns
		V <sub>CC</sub> = 4.5 V	-	21	37	-	46	-	56	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	17	31	-	39	-	48	ns
		LE to Qn; see Fig. 6 [2]								
		V <sub>CC</sub> = 2.0 V	-	55	170	-	215	-	255	ns
		V <sub>CC</sub> = 4.5 V	-	20	34	-	43	-	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	16	29	-	37	-	43	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Qn; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	-	50	155	-	195	-	235	ns
		V <sub>CC</sub> = 4.5 V	-	18	31	-	39	-	47	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	-	33	-	40	ns
t <sub>t</sub>	transition time	see Fig. 6 [3]								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	119	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>w</sub>	pulse width	LE HIGH or LOW; see Fig. 6								
		V <sub>CC</sub> = 2.0 V	70	17	-	90	-	105	-	ns
		V <sub>CC</sub> = 4.5 V	14	6	-	18	-	21	-	ns
		V <sub>CC</sub> = 6.0 V	12	5	-	15	-	18	-	ns
		MR LOW; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	70	17	-	90	-	105	-	ns
		V <sub>CC</sub> = 4.5 V	14	6	-	18	-	21	-	ns
		V <sub>CC</sub> = 6.0 V	12	5	-	15	-	18	-	ns
t <sub>su</sub>	set-up time	D, An to LE; see Fig. 8 and Fig. 9								
		V <sub>CC</sub> = 2.0 V	80	19	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns

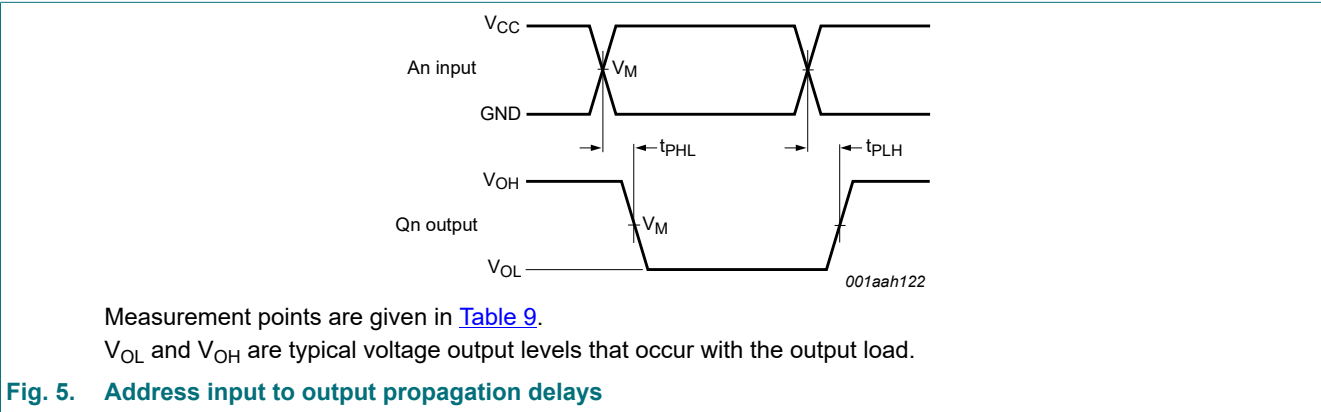
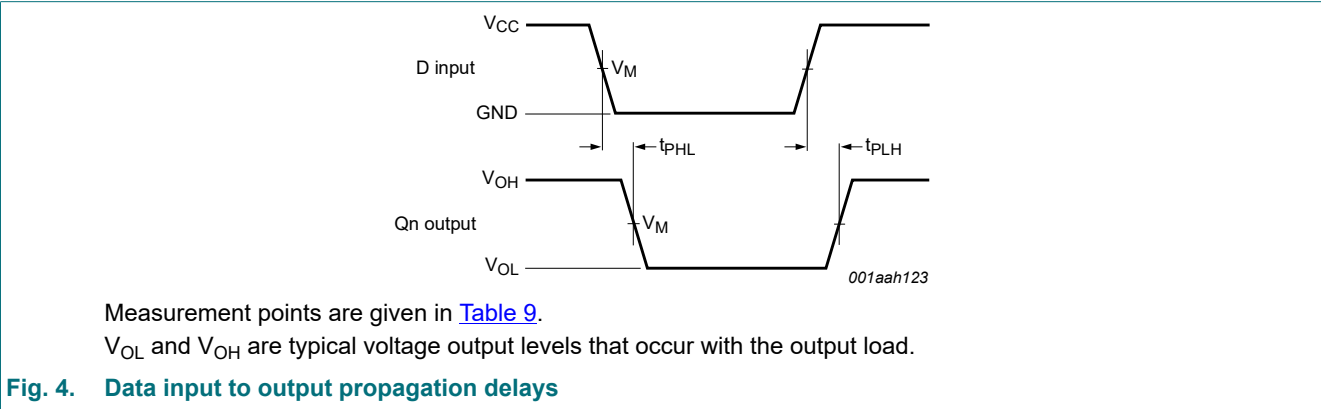
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>h</sub>	hold time	D to $\overline{\text{LE}}$ ; see Fig. 8 and Fig. 9								
		V <sub>CC</sub> = 2.0 V	0	-19	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-6	-	0	-	0	-	ns
		V <sub>CC</sub> = 6.0 V	0	-5	-	0	-	0	-	ns
		An to $\overline{\text{LE}}$ ; see Fig. 8 and Fig. 9								
		V <sub>CC</sub> = 2.0 V	2	-11	-	2	-	2	-	ns
		V <sub>CC</sub> = 4.5 V	2	-4	-	2	-	2	-	ns
		V <sub>CC</sub> = 6.0 V	2	-3	-	2	-	2	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [4]	-	19	-	-	-	-	-	pF
74HCT259-Q100										
t <sub>pd</sub>	propagation delay	D to Q <sub>n</sub> ; see Fig. 4 [2]								
		V <sub>CC</sub> = 4.5 V	-	23	39	-	49	-	59	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	20	-	-	-	-	-	ns
		An to Q <sub>n</sub> ; see Fig. 5 [2]								
		V <sub>CC</sub> = 4.5 V	-	25	41		51		62	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	20	-	-	-	-	-	ns
		$\overline{\text{LE}}$ to Q <sub>n</sub> ; see Fig. 6 [2]								
		V <sub>CC</sub> = 4.5 V	-	22	38	-	48	-	57	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	20	-	-	-	-	-	ns
		MR to Q <sub>n</sub> ; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	-	23	39	-	49	-	59	ns
t <sub>t</sub>	transition time	V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	20	-	-	-	-	-	ns
		see Fig. 6 [3]								
t <sub>W</sub>	pulse width	V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		LE HIGH or LOW; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	19	11	-	24	-	29	-	ns
t <sub>su</sub>	set-up time	MR LOW; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	18	10	-	23	-	27	-	ns
		D, An to $\overline{\text{LE}}$ ; see Fig. 8 and Fig. 9								
t <sub>h</sub>	hold time	V <sub>CC</sub> = 4.5 V	17	10	-	21	-	26	-	ns
		D to $\overline{\text{LE}}$ ; see Fig. 8 and Fig. 9								
		V <sub>CC</sub> = 4.5 V	0	-8	-	0	-	0	-	ns
		An to $\overline{\text{LE}}$ ; see Fig. 8 and Fig. 9								
t <sub>h</sub>	hold time	V <sub>CC</sub> = 4.5 V	0	-4	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-4	-	0	-	0	-	ns

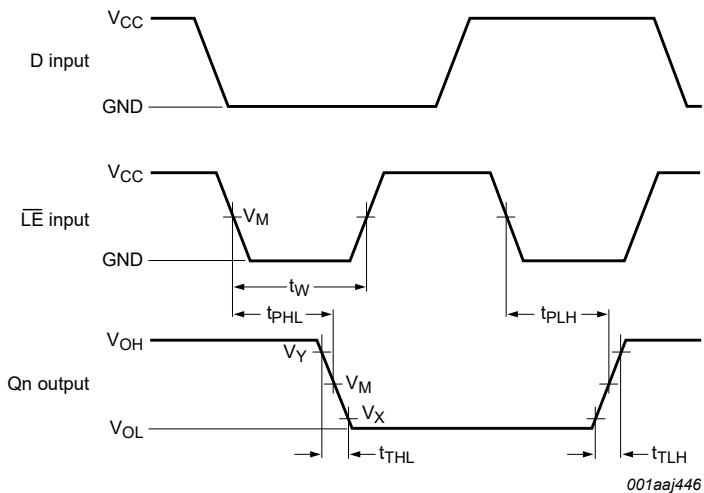


Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [4]	-	19	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] t<sub>i</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
f<sub>i</sub> = input frequency in MHz;  
f<sub>o</sub> = output frequency in MHz;  
C<sub>L</sub> = output load capacitance in pF;  
V<sub>CC</sub> = supply voltage in V;  
N = number of inputs switching;  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

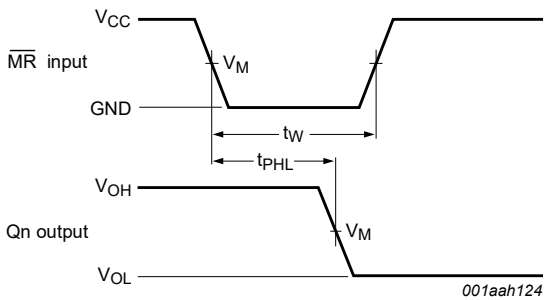
10.1. Waveforms and test circuit





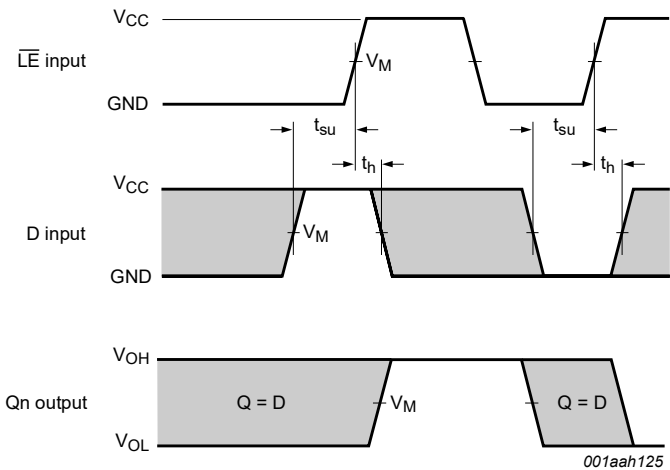
Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 6. Enable input to output propagation delays and pulse width**



Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 7. Master reset input to output propagation delays**



Measurement points are given in [Table 9](#).  
The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 8. Data input to latch enable input set-up and hold times**

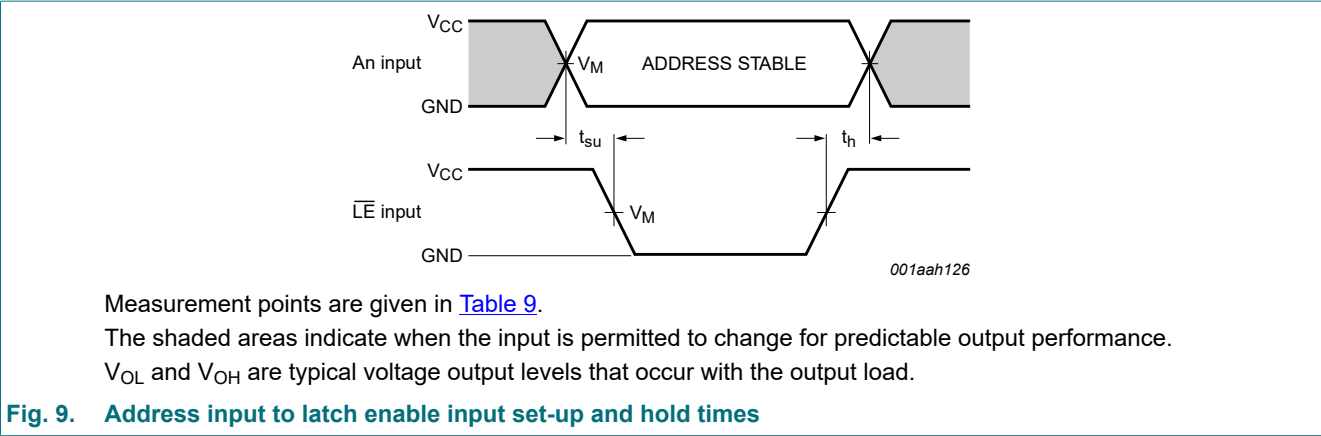


Table 9. Measurement points

Type	Input	Output		
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
74HC259-Q100	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.1 × V <sub>CC</sub>	0.9 × V <sub>CC</sub>
74HCT259-Q100	1.3 V	1.3 V	0.1 × V <sub>CC</sub>	0.9 × V <sub>CC</sub>

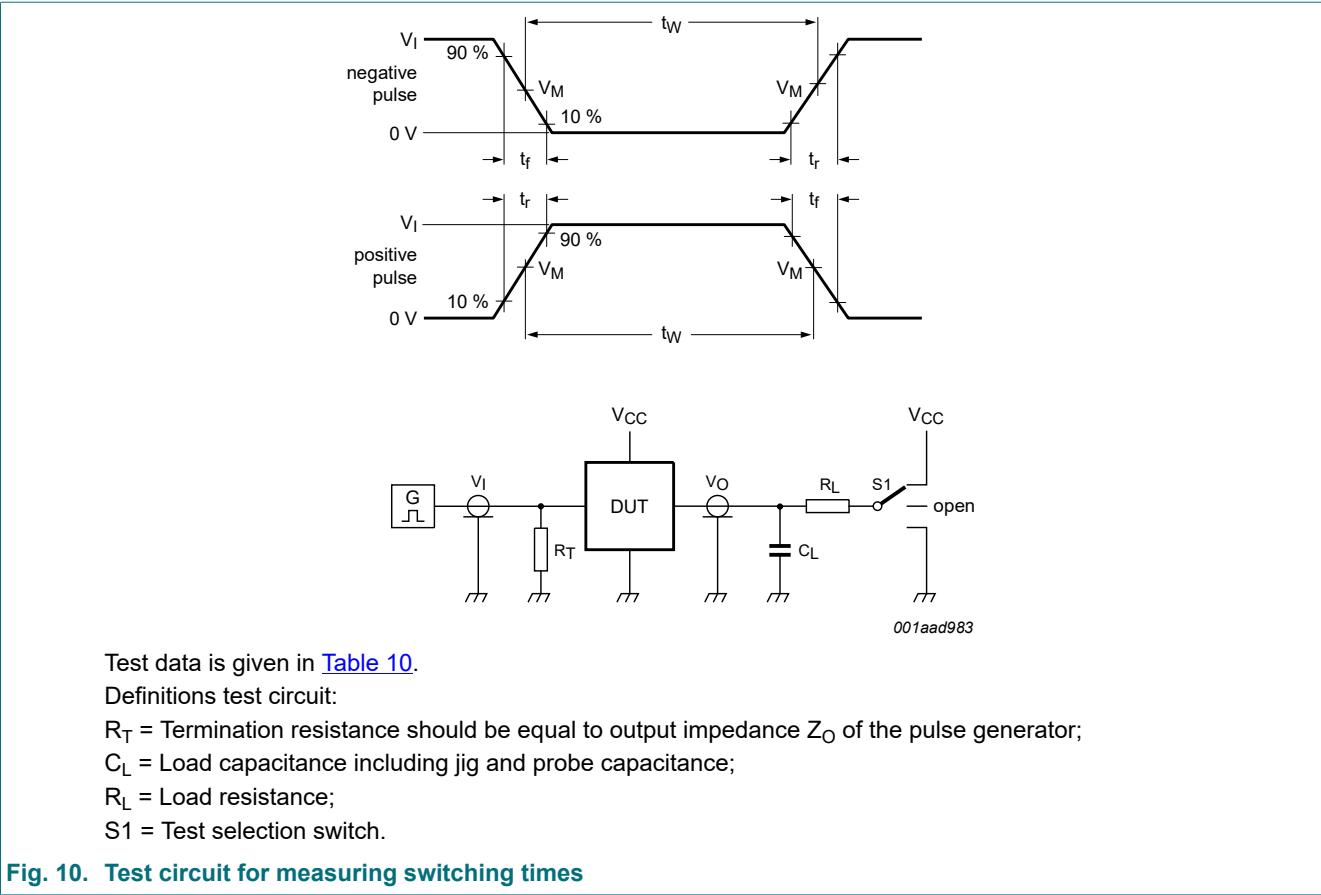


Table 10. Test data

Type	Input		Load		S1 position
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>pHL</sub> , t <sub>pLH</sub>
74HC259-Q100	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT259-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

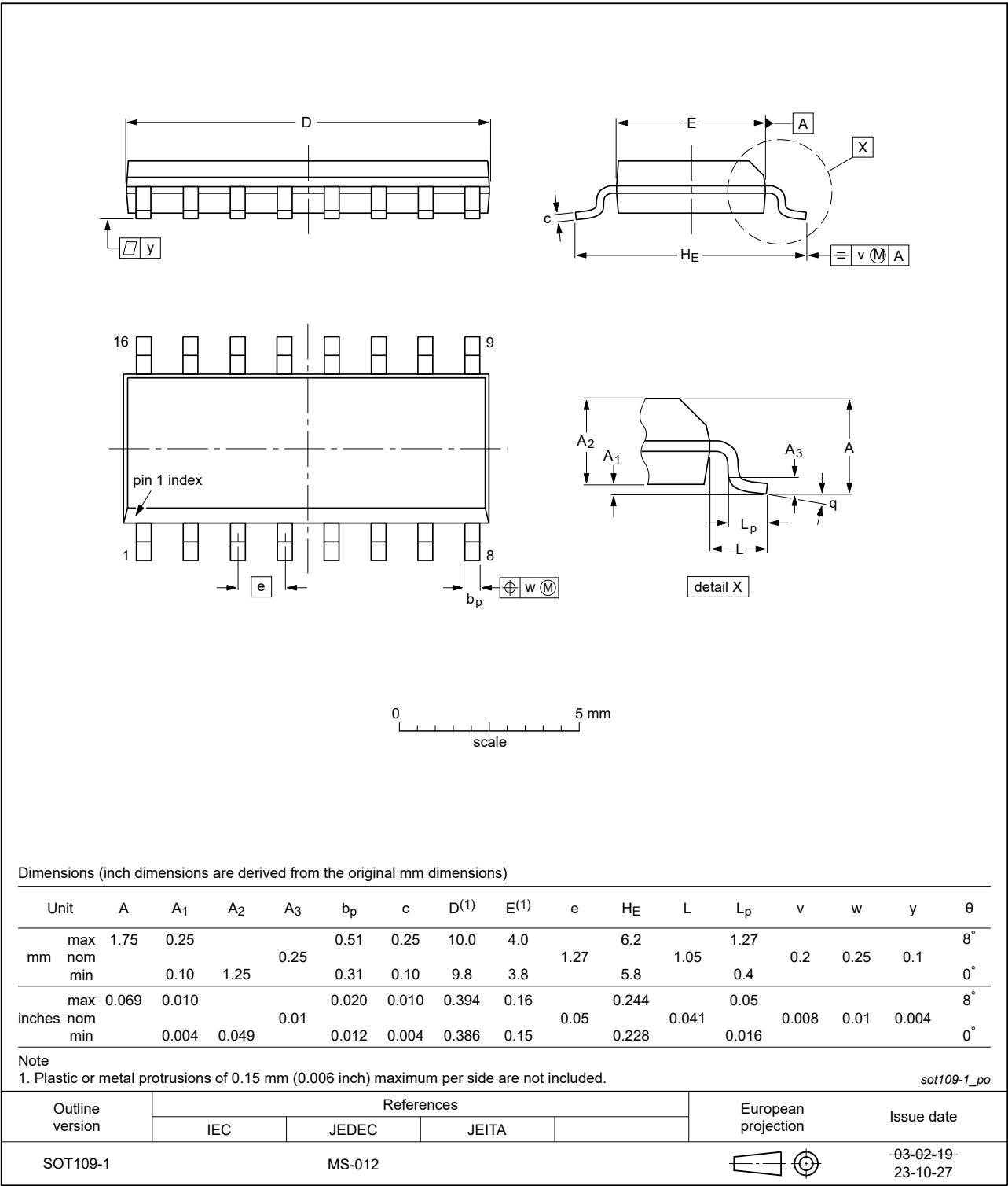


Fig. 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

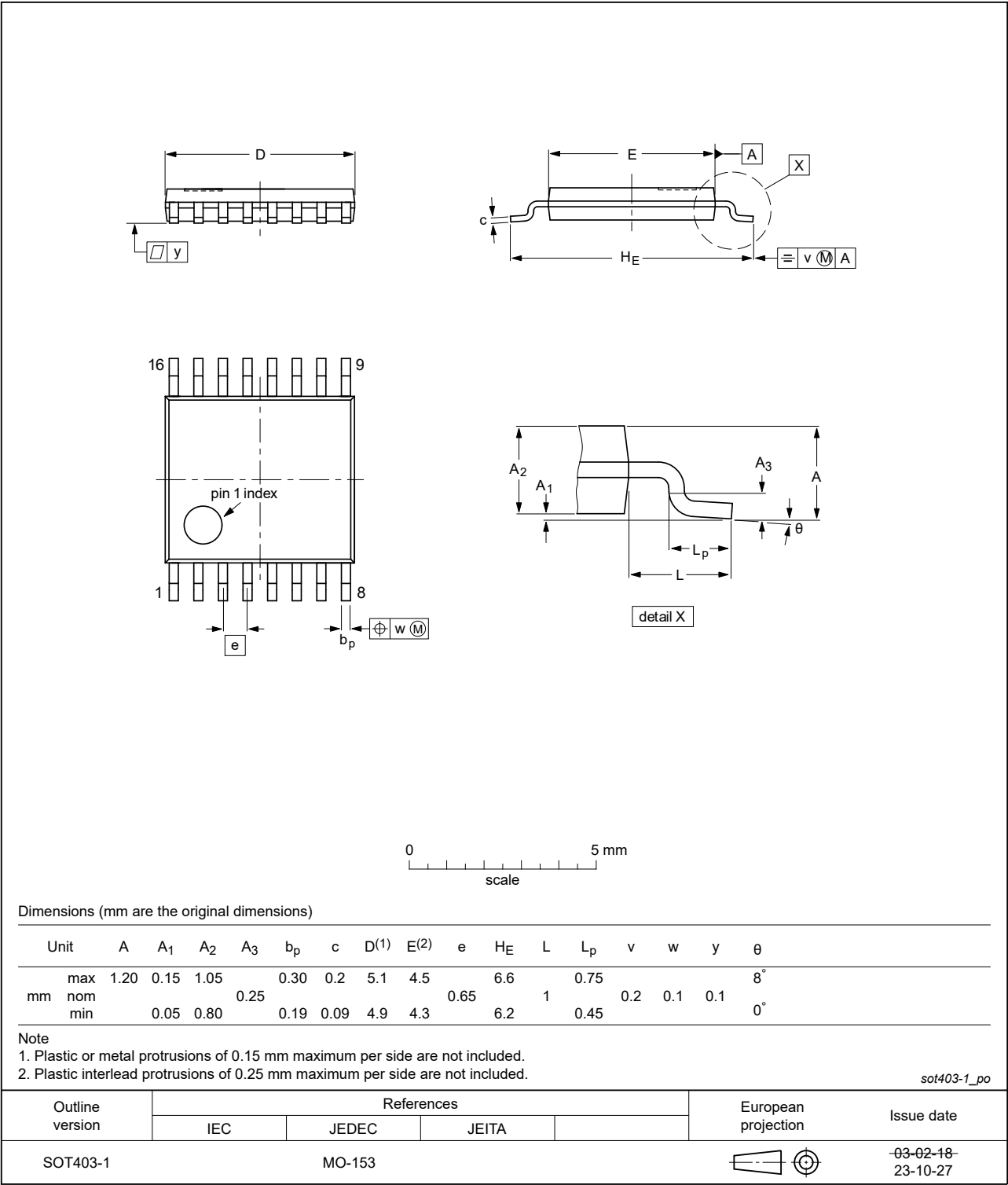


Fig. 12. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

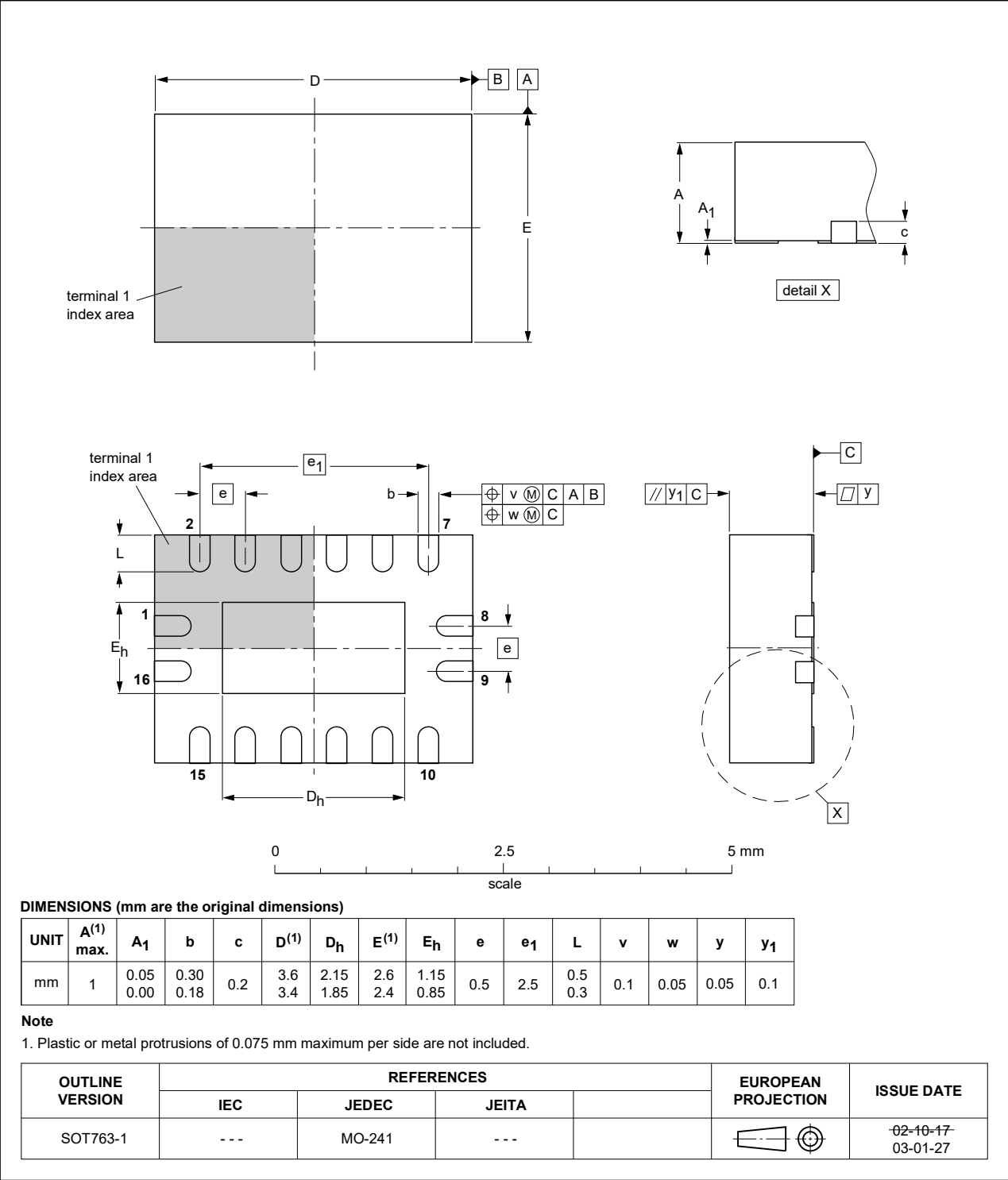


Fig. 13. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT259_Q100 v.3	20240311	Product data sheet	-	74HC_HCT259_Q100 v.2
Modifications:	<ul style="list-style-type: none"><li><a href="#">Fig. 11</a>, <a href="#">Fig. 12</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li><li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li></ul>			
74HC_HCT259_Q100 v.2	20200902	Product data sheet	-	74HC_HCT259_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li><li><a href="#">Table 5</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li></ul>			
74HC_HCT259_Q100 v.1	20120730	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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