# 74HC165-Q100; 74HCT165-Q100

# 8-bit parallel-in/serial out shift register

Rev. 3 — 23 April 2020

**Product data sheet** 

### 1. General description

The 74HC165-Q100; 74HCT165-Q100 are 8-bit serial or parallel-in/serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and  $\overline{\text{Q7}}$ ). When the parallel load input ( $\overline{\text{PL}}$ ) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When  $\overline{\text{PL}}$  is HIGH data enters the register serially at DS. When the clock enable input ( $\overline{\text{CE}}$ ) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on  $\overline{\text{CE}}$  will disable the CP input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Asynchronous 8-bit parallel load
- · Synchronous serial input
- · Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC165-Q100: CMOS level
  - For 74HCT165-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

# 3. Applications

Parallel-to-serial data conversion

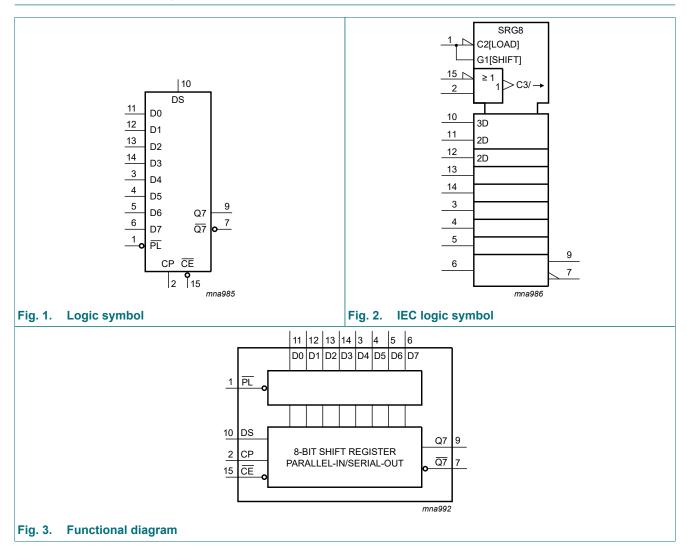


# 4. Ordering information

**Table 1. Ordering information** 

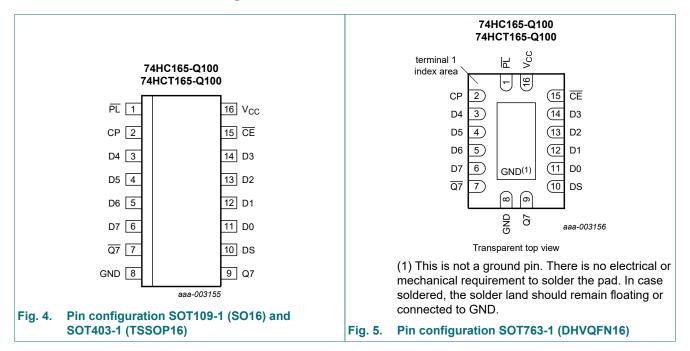
Type number	Package									
	Temperature range	Name	Description	Version						
74HC165D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads;	SOT109-1						
74HCT165D-Q100			body width 3.9 mm							
74HC165PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads;	SOT403-1						
74HCT165PW-Q100			body width 4.4 mm							
74HC165BQ-Q100	-40 °C to +125 °C									
74HCT165BQ-Q100			very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm							

# 5. Functional diagram



# 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
PL	1	asynchronous parallel load input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
<del>Q7</del>	7	complementary output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs (also referred to as Dn)
CE	15	clock enable input (active LOW)
V <sub>CC</sub>	16	positive supply voltage

# 7. Functional description

#### Table 3. Function table

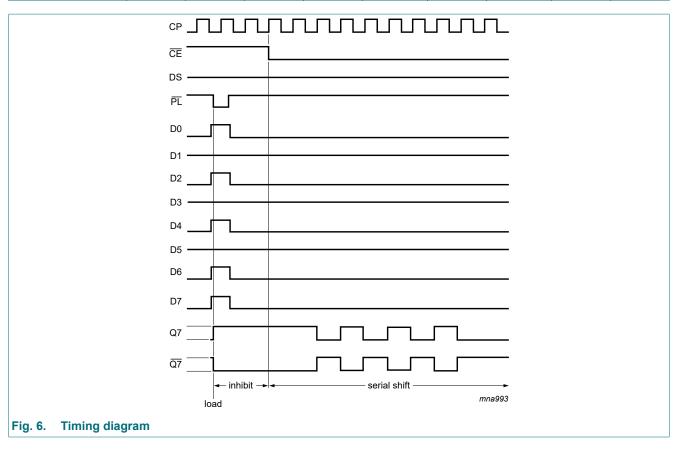
H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

 $X = don't care; \uparrow = LOW-to-HIGH clock transition.$ 

Operating modes	Inputs					Qn reg	isters	Outputs	
	PL	CE	СР	DS	D0 to D7	Q0	Q1 to Q6	Q7	Q7
parallel load	L	Х	Х	Х	L	L	L to L	L	Н
	L	Х	Х	Х	Н	Н	H to H	Н	L
serial shift	Н	L	1	I	Х	L	q0 to q5	q6	q6
	Н	L	1	h	Х	Н	q0 to q5	q6	q6
	Н	1	L	I	Х	L	q0 to q5	q6	q6
	Н	1	L	h	Х	Н	q0 to q5	q6	q6
hold "do nothing"	Н	Н	Х	Х	Х	q0	q1 to q6	q7	q <del>7</del>
	Н	Х	Н	Х	Х	q0	q1 to q6	q7	<del>q</del> 7



# 8. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_1 < -0.5 \text{ V or } V_1 > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC165-Q100		74H	CT165-C	100	Unit	
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

### 10. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC16	5-Q100									
$V_{IH}$	HIGH-level input	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

<sup>[2]</sup> For SOT109-1 (SO16) package: Ptot derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: Ptot derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package: Ptot derates linearly with 11.2 mW/K above 106 °C.

Symbol	Parameter	Conditions		25 °C		-	°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	٧
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	٧
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	٧
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	٧
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	٧
V <sub>OL</sub>	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	٧
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	٧
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	٧
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT1	65-Q100		•	'	<b>'</b>	'	'	'	'	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 V$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	٧
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	٧
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	٧
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V								
		Dn and DS inputs	-	35	126	-	157.5	-	171.5	μΑ
		CP, CE, and PL inputs	-	65	234	-	292.5	-	318.5	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

# 11. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit, see Fig. 12

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC16	5-Q100									
t <sub>pd</sub>	propagation	CP or CE to Q7, Q7; see Fig. 7 [1]								
	delay	V <sub>CC</sub> = 2.0 V	-	52	165	-	205	-	250	ns
		V <sub>CC</sub> = 4.5 V	-	19	33	-	41	-	50	ns
		V <sub>CC</sub> = 6.0 V	-	15	28	-	35	-	43	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	16	-	-	-	-	-	ns
		PL to Q7, Q7; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	-	50	165	-	205	-	250	ns
		V <sub>CC</sub> = 4.5 V	-	18	33	-	41	-	50	ns
		V <sub>CC</sub> = 6.0 V	-	14	28	-	35	-	43	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	-	-	ns
		D7 to Q7, Q7; see Fig. 9								
		V <sub>CC</sub> = 2.0 V	-	36	120	-	150	-	180	ns
		V <sub>CC</sub> = 4.5 V	-	13	24	-	30	-	36	ns
		V <sub>CC</sub> = 6.0 V	-	10	20	-	26	-	31	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	11	-	-	-	-	-	ns
t <sub>t</sub>	transition time	Q7, Q7 output; see Fig. 7 [2]								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
t <sub>W</sub>	pulse width	CP input HIGH or LOW; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	80	17	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	5	-	17	-	20	-	ns
		PL input LOW; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	80	14	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	5	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	4	-	17	-	20	-	ns
t <sub>rec</sub>	recovery time	PL to CP, CE; see Fig. 8								
		V <sub>CC</sub> = 2.0 V	100	22	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	20	8	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	17	6	-	21	-	26	-	ns

Symbol	Parameter	Conditions		25 °C			°C to 5 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>su</sub>	set-up time	DS to CP, CE; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	80	11	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	4	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	3	-	17	-	20	-	ns
		CE to CP and CP to CE; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	80	17	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	5	-	17	-	20	-	ns
		Dn to PL; see Fig. 11								
		V <sub>CC</sub> = 2.0 V	80	22	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>h</sub>	hold time	DS to CP, CE and Dn to PL; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	5	2	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	2	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	2	-	5	-	5	-	ns
		CE to CP and CP to CE; see Fig. 10								
		V <sub>CC</sub> = 2.0 V	5	-17	-	5	-	5	-	ns
		V <sub>CC</sub> = 4.5 V	5	-6	-	5	-	5	-	ns
		V <sub>CC</sub> = 6.0 V	5	-5	-	5	-	5	-	ns
f <sub>max</sub>	maximum	CP input; see Fig. 7								
	frequency	V <sub>CC</sub> = 2.0 V	6	17	-	5	-	4	-	MHz
		V <sub>CC</sub> = 4.5 V	30	51	-	24	-	20	-	MHz
		V <sub>CC</sub> = 6.0 V	35	61	-	28	-	24	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	56	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC}$ [3]	-	35	-	-	-	-	-	pF
74HCT1										
t <sub>pd</sub>	propagation	CE, CP to Q7, Q7; see Fig. 7 [1]								T
-pa	delay	V <sub>CC</sub> = 4.5 V	_	17	34	_	43	_	51	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	_	14	_	_	-	_	_	ns
		PL to Q7, Q7; see Fig. 8		1 7						
		V <sub>CC</sub> = 4.5 V	_	20	40	_	50	_	60	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$		17	-	_	-	_	-	ns
				.,						1
		D7 to Q7, Q7; see <u>Fig. 9</u> V <sub>CC</sub> = 4.5 V		14	28	_	35	_	42	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	11	-	-	-	_	-	ns

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>t</sub>	transition time	Q7, Q7 output; see Fig. 7 [2]								
	V <sub>CC</sub> = 4.5 V		-	7	15	-	19	-	22	ns
t <sub>W</sub>	pulse width	CP input; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	16	6	-	20	-	24	-	ns
		PL input; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	9	-	25	-	30	-	ns
t <sub>rec</sub>	recovery time	PL to CP, CE; see Fig. 8								
		V <sub>CC</sub> = 4.5 V	20	8	-	25	-	30	-	ns
t <sub>su</sub>	set-up time	DS to CP, CE; see Fig. 10								
		V <sub>CC</sub> = 4.5 V	20	2	-	25	-	30	-	ns
		CE to CP and CP to CE; see Fig. 10								
		V <sub>CC</sub> = 4.5 V	20	7	-	25	-	30	-	ns
		Dn to PL; see Fig. 11								
		V <sub>CC</sub> = 4.5 V	20	10	-	25	-	30	-	ns
t <sub>h</sub>	hold time	DS to CP, CE and Dn to PL; see Fig. 10								
		V <sub>CC</sub> = 4.5 V	7	-1	-	9	-	11	-	ns
		CE to CP and CP to CE; see Fig. 10								
		V <sub>CC</sub> = 4.5 V	0	-7	-	0	-	0	-	ns
f <sub>max</sub>	maximum	CP input; see Fig. 7								
	frequency	V <sub>CC</sub> = 4.5 V	26	44	-	21	-	17	-	MHz
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	48	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	per package; [3] V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	-	35	-	-	-	-	-	pF

f<sub>i</sub> = input frequency in MHz;

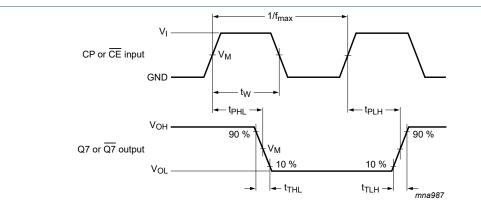
f<sub>o</sub> = output frequency in MHz;

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs};$ 

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

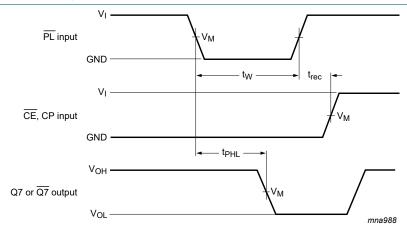
#### 11.1. Waveforms and test circuit



Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

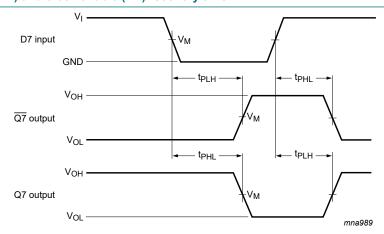
Fig. 7. The clock (CP) or clock enable (CE) to output (Q7 or Q7) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig. 8. The parallel load (PL) pulse width, the parallel load to output (Q7 or Q7) propagation delays, the parallel load to clock (CP) and clock enable (CE) recovery time

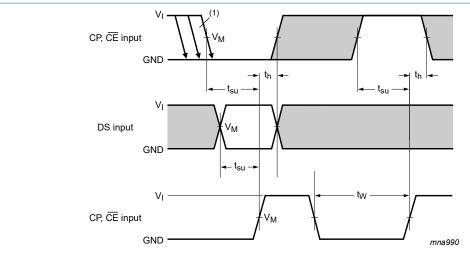


Measurement points are given in Table 8.

 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 9. The data input (D7) to output (Q7 or  $\overline{Q7}$ ) propagation delays when  $\overline{PL}$  is LOW

Product data sheet

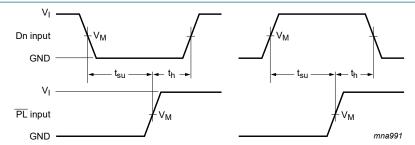


(1)  $\overline{\text{CE}}$  may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance Measurement points are given in <u>Table 8</u>.

 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 10. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable (CE) inputs, from the clock enable input (CE) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE)



Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

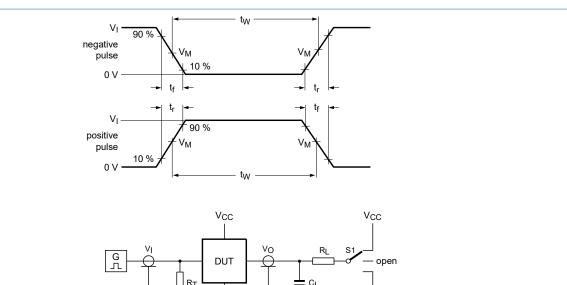
Fig. 11. The set-up and hold times from the data inputs (Dn) to the parallel load input (PL)

**Table 8. Measurement points** 

Туре	Input	Output							
	VI	V <sub>M</sub>	V <sub>M</sub>						
74HC165-Q100	V <sub>CC</sub>	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>						
74HCT165-Q100	3 V	1.3 V	1.3 V						

001aad983

### 8-bit parallel-in/serial out shift register



Test data is given in Table 9.

Definitions for test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

 $R_{l}$  = Load resistance.

S1 = Test selection switch

Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load		S1 position
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	$R_L$	t <sub>PHL</sub> , t <sub>PLH</sub>
74HC165-Q100	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT165-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

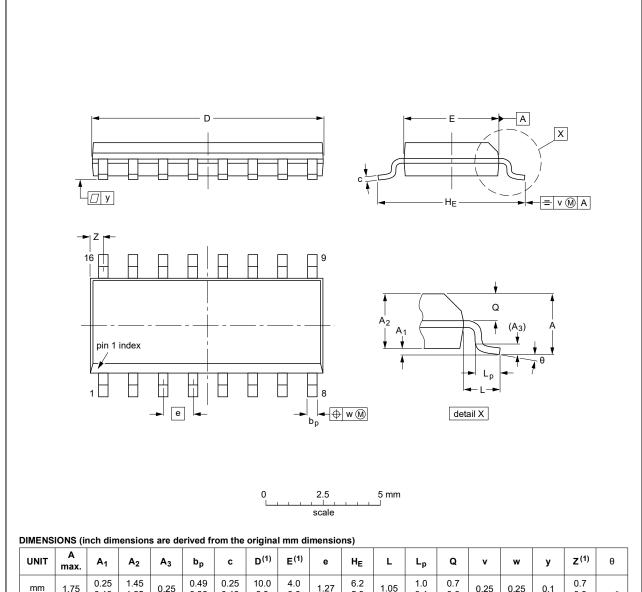
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# 12. Package outline

#### SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

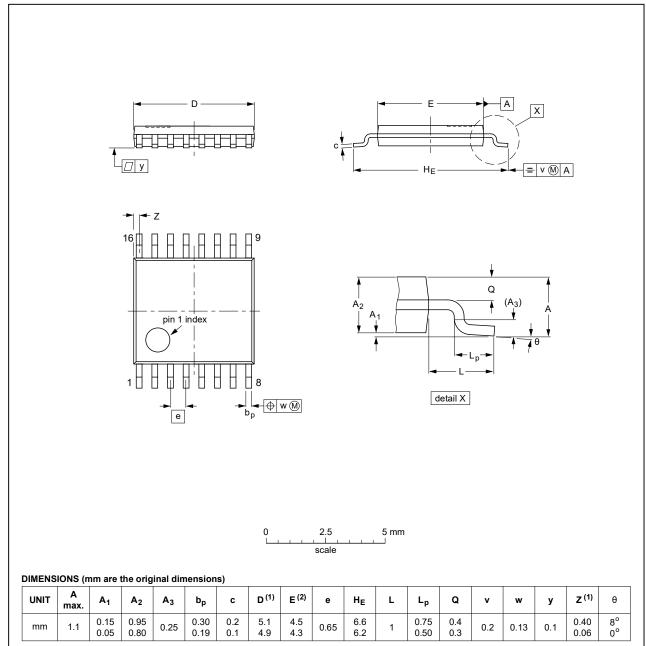
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012				<del>99-12-27</del> 03-02-19	

Fig. 13. Package outline SOT109-1 (SO16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				<del>99-12-27</del> 03-02-18	

Fig. 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

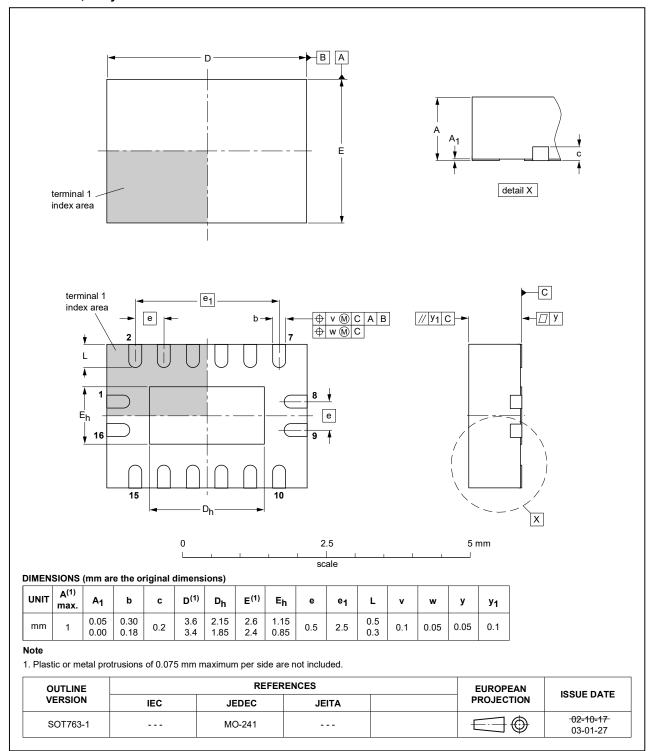


Fig. 15. Package outline SOT763-1 (DHVQFN16)

# 13. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT165_Q100 v.3	20200423	Product data sheet	-	74HC_HCT165_Q100 v.2
Modifications:	<ul><li><u>Section 2</u> upda</li><li><u>Table 4</u>: Derati</li></ul>	ng values for P <sub>tot</sub> total power c	lissipation updated.	
74HC_HCT165_Q100 v.2	20170821	Product data sheet	-	74HC_HCT165_Q100 v.1
Modifications:	<ul> <li>The format of t Nexperia.</li> </ul>	ated. ime for 74HC165 has been up this data sheet has been redes we been adapted to the new co	igned to comply with	
74HC_HCT165_Q100 v.1	20120717	Product data sheet	-	-

### 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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