74HC194

4-bit bidirectional universal shift register

Rev. 4 — 16 March 2021 Product data sheet

1. General description

The 74HC194 is a 4-bit bidirectional universal shift register. The synchronous operation of the device is determined by the mode select inputs (S0, S1). In parallel load mode (S0 and S1 HIGH) data appearing on the D0 to D3 inputs, when S0 and S1 are HIGH, is transferred to the Q0 to Q3 outputs. When S0 is HIGH and S1 is LOW data is entered serially via DSL and shifted from left to right; when S0 is LOW and S1 is HIGH data is entered serially via DSR and shifted from right to left. DSR and DSL allow multistage shift right or shift left data transfers without interfering with parallel load operation. If both S0 and S1 are LOW, existing data is retained in a hold mode. Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse. When LOW, the asynchronous master reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- CMOS input levels
- Shift-left and shift right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold (‘do nothing’) mode
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC194DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1

4. Functional diagram

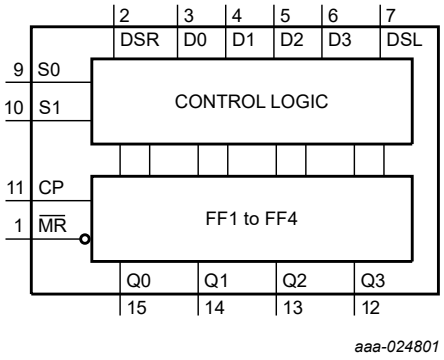


Fig. 1. Functional diagram

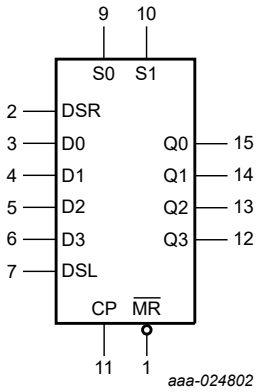


Fig. 2. Logic symbol

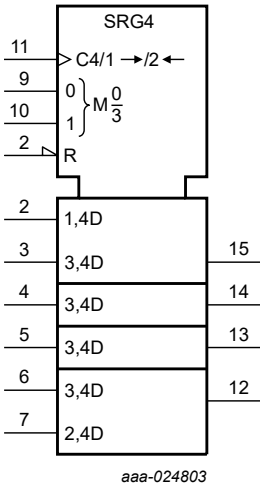


Fig. 3. IEC logic symbol

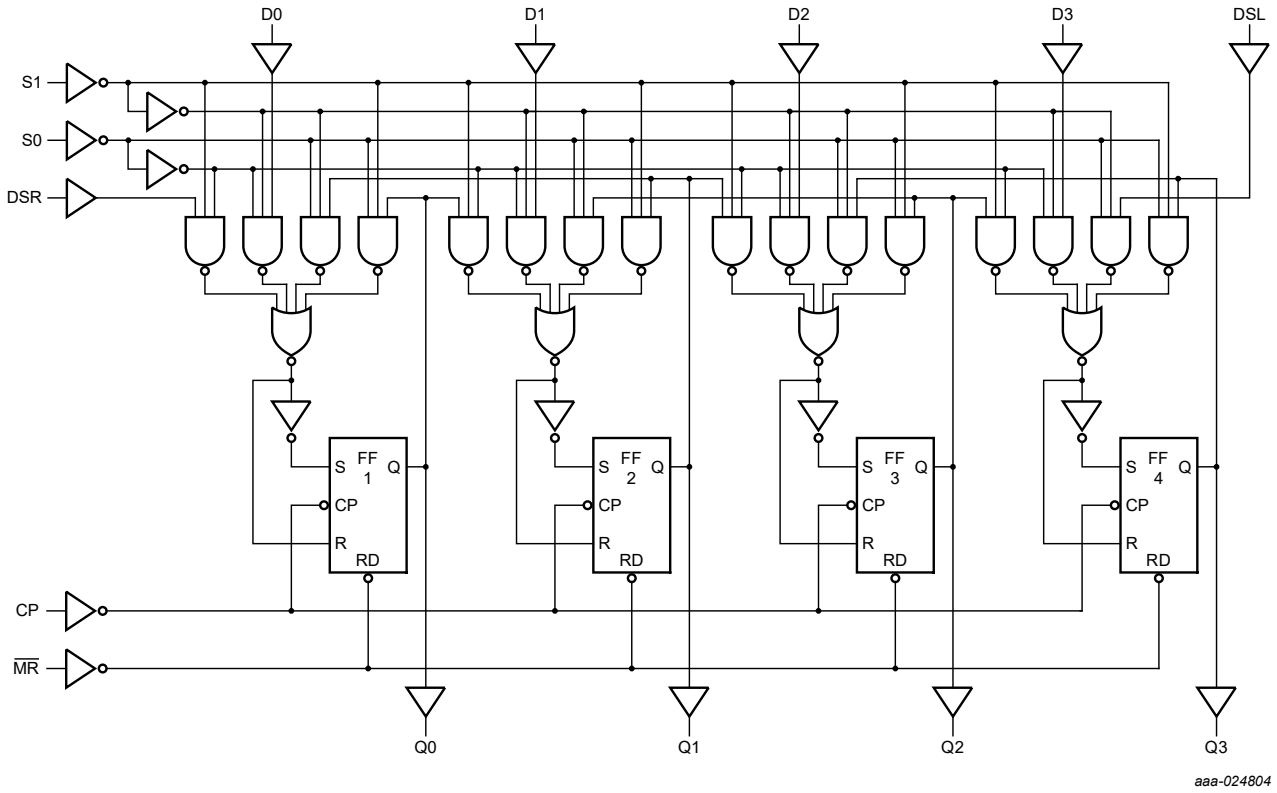


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

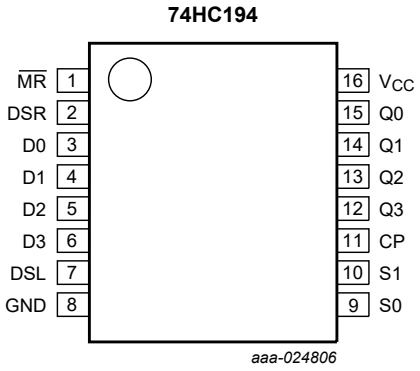


Fig. 5. Pin configuration SOT338-1 (SSOP16)

5.2. Pin description

Table 2. Pin description

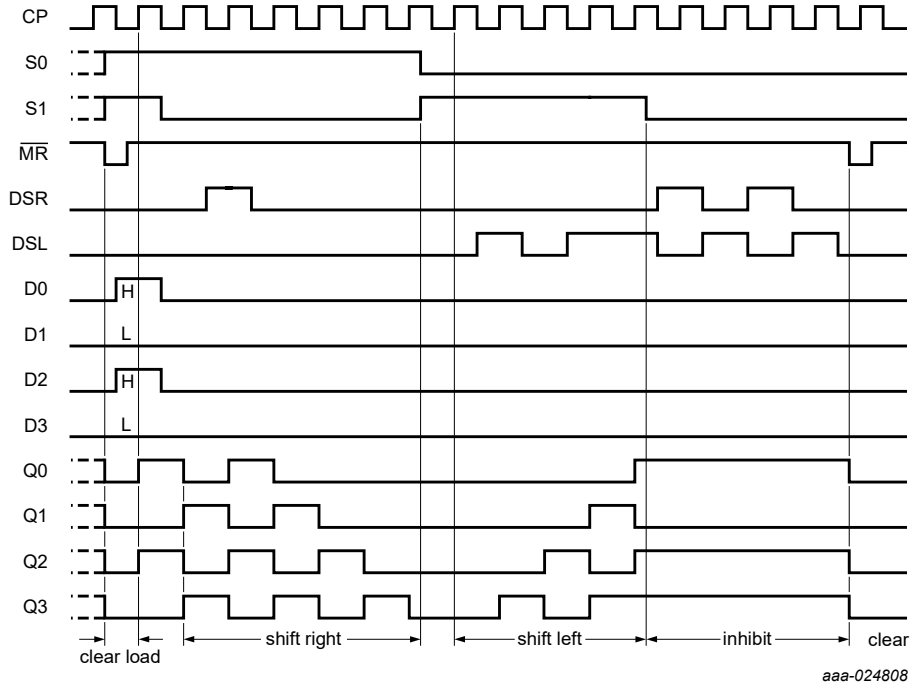
Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset (active LOW)
DSR	2	serial data input (shift right)
D0, D1, D2, D3	3, 4, 5, 6	parallel data inputs
DSL	7	serial data input (shift left)
GND	8	ground (0 V)
S0, S1	9, 10	mode control inputs
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q0, Q1, Q2, Q3	15, 14, 13, 12	parallel outputs
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition; X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating mode	Inputs							Outputs			
	CP	$\overline{MR}$	S1	S0	DSR	DSL	Dn	Q0	Q1	Q2	Q3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q0	q1	q2	q3
Shift left	↑	H	h	l	X	l	X	q1	q2	q3	L
	↑	H	h	l	X	h	X	q1	q2	q3	H
Shift right	↑	H	l	h	l	X	X	L	q0	q1	q2
	↑	H	l	h	h	X	X	H	q0	q1	q2
Parallel load	↑	H	h	h	X	X	dn	d0	d1	d2	d3



Typical timing sequence:

Typical clear-load; shift-right; shift-left; inhibit and clear timing sequences.

Fig. 6. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

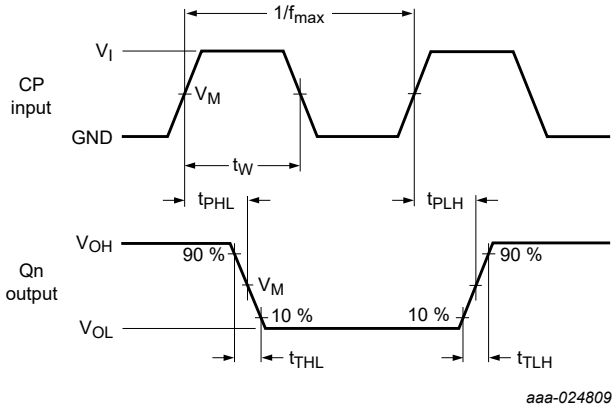
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 7 [1]								
		V_{CC} = 2.0 V	-	47	145	-	180	-	220	ns
		V_{CC} = 4.5 V	-	17	29	-	36	-	44	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	25	-	31	-	38	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 8								
		V_{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V_{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t_t	transition time	Qn; see Fig. 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 7								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		$\overline{MR}$ pulse width LOW; see Fig. 8								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 8								
		V_{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	5	-	13	-	15	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	Dn to CP; see Fig. 9								
		V_{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	5	-	15	-	18	-	ns
		S0, S1 to CP; see Fig. 10								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	12	6	-	17	-	20	-	ns
		DSR, DSL to CP; see Fig. 9								
		V_{CC} = 2.0 V	70	19	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	7	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	6	-	15	-	18	-	ns
t_h	hold time	Dn to CP; see Fig. 9								
		V_{CC} = 2.0 V	0	-14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-4	-	0		0	-	ns
		S0, S1 to CP; see Fig. 10								
		V_{CC} = 2.0 V	0	-11	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-4	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-3	-	0		0	-	ns
		DSR, DSL to CP; see Fig. 9								
		V_{CC} = 2.0 V	0	-17	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-6	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-5	-	0		0	-	ns
f_{max}	maximum frequency	CP; see Fig. 7								
		V_{CC} = 2.0 V	6	31	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	93	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	102	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	111	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; f_i = 1 MHz [3]	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

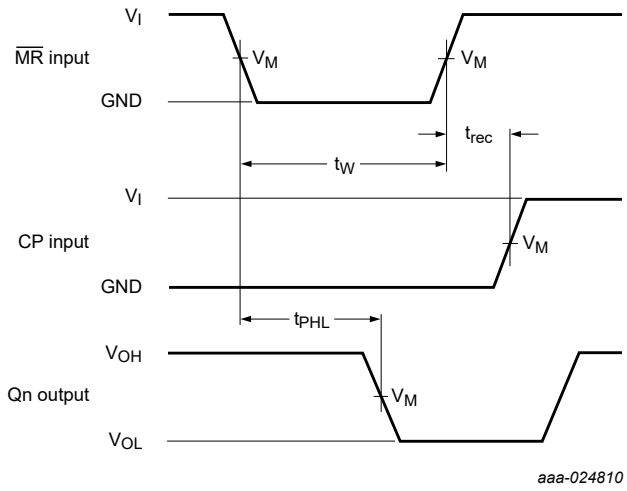
10.1. Waveforms



Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

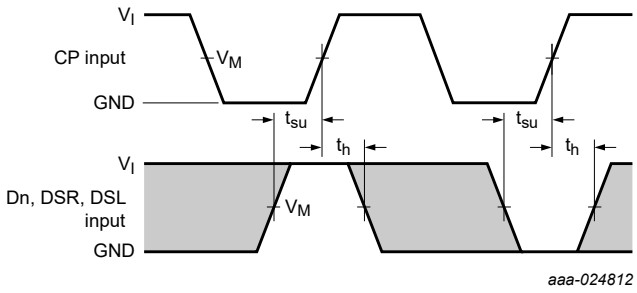
Fig. 7. The clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

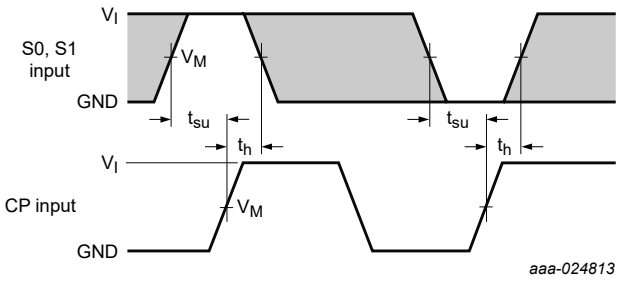
Fig. 8. The master reset ($\overline{MR}$) pulse width, master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery times



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. The set-up and hold times from the data inputs (Dn, DSR and DSL) to the clock (CP)



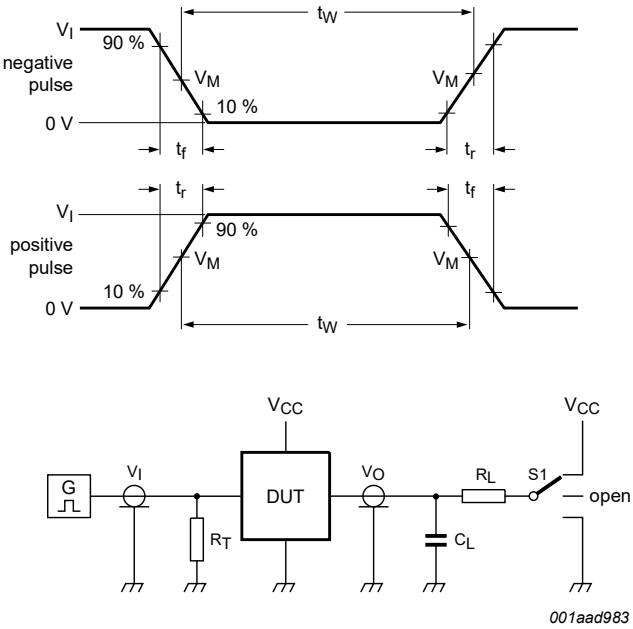
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 10. The set-up and hold times from the mode control inputs (Sn) to the clock input

Table 8. Measurement points

Input		Output
V_M	V_I	V_M
0.5 × V_{CC}	GND to V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.

Test circuit definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance.

S1 = Test selection switch

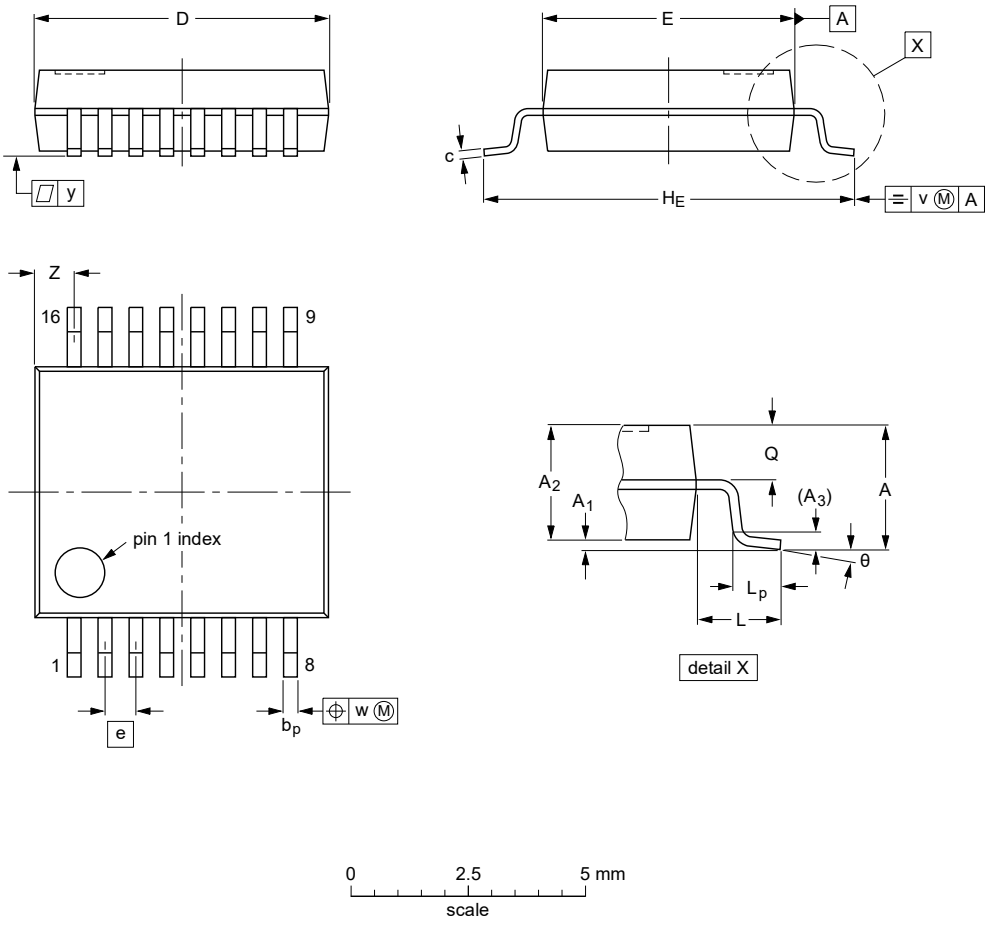
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 12. Package outline SOT338-1 (SSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC194 v.4	20210316	Product data sheet	-	74HC_HCT194 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74HC194D (SOT109-1 / SO16) removed.			
74HC194 v.3	20161129	Product data sheet	-	74HC_HCT194 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC194N, 74HCT194N and 74HCT194D removed.			
74HC_HCT194 v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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