74ALVCH16543

16-bit D-type registered transceiver; 3-state

Rev. 3 — 15 December 2017 Product data sheet

1 General description

The 74ALVCH16543 is a dual octal registered transceiver. Each section contains two sets of D-type latches for temporary storage of the data flow in either direction.

Separate latch enable (n$\overline{\text{LEAB}}$, n$\overline{\text{LEBA}}$) and output enable (n$\overline{\text{OEAB}}$, n$\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of the data flow.

The 74ALVCH16543 contains two sections each consisting of two sets of eight D-type latches with separate inputs and controls for each set. For data flow from A to B, for example, the A-to-B enable (n$\overline{\text{EAB}}$) inputs must be LOW in order to enter data from nA0 to nA7, or take data from nB0 to nB7, as indicated in the function table. With n$\overline{\text{EAB}}$ LOW, a LOW signal on the A-to-B latch enable (n$\overline{\text{LEAB}}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the n$\overline{\text{LEAB}}$ signal stores the A data into the latches. With n$\overline{\text{EAB}}$ and n$\overline{\text{OEAB}}$ both LOW, the 3-state B output buffers are active and display the data present at the output of the A latches. Similarly, the n$\overline{\text{EBA}}$, n$\overline{\text{LEBA}}$ and n$\overline{\text{OEBA}}$ signals control the data flow from B-to-A.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

2 Features and benefits

- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE flow-through standard pin-out architecture
- Back-to-back registers for storage
- Output drive capability 50 Ω transmission lines at 85 °C
- All data inputs have bushold
- Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce
- Current drive ±24 mA at V_{CC} = 3.0 V.
- 3-state non-inverting outputs for bus oriented applications
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

nexperia

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16543DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4 Functional diagram

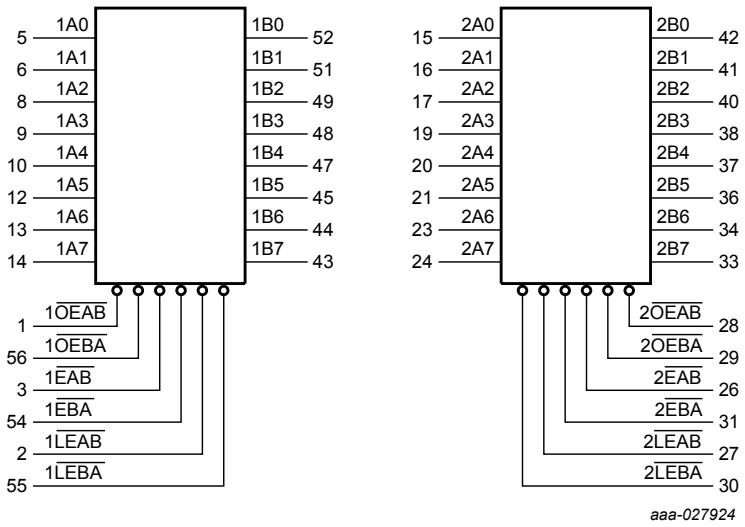


Figure 1. Logic symbol

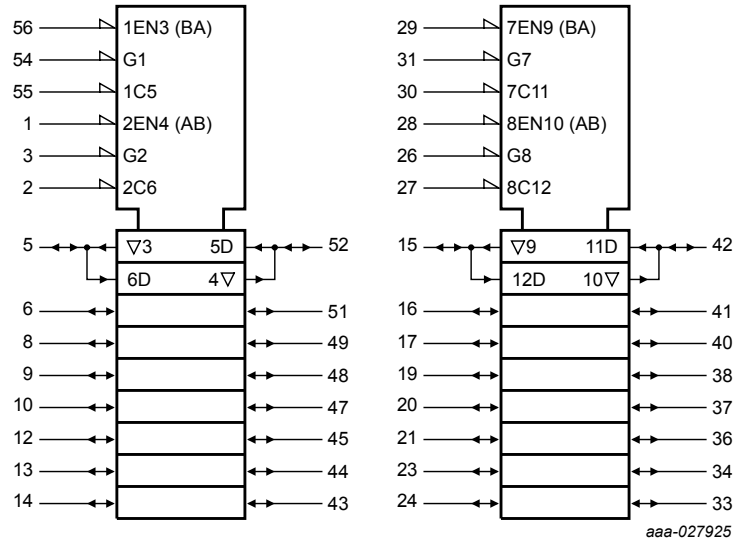


Figure 2. IEC logic symbol

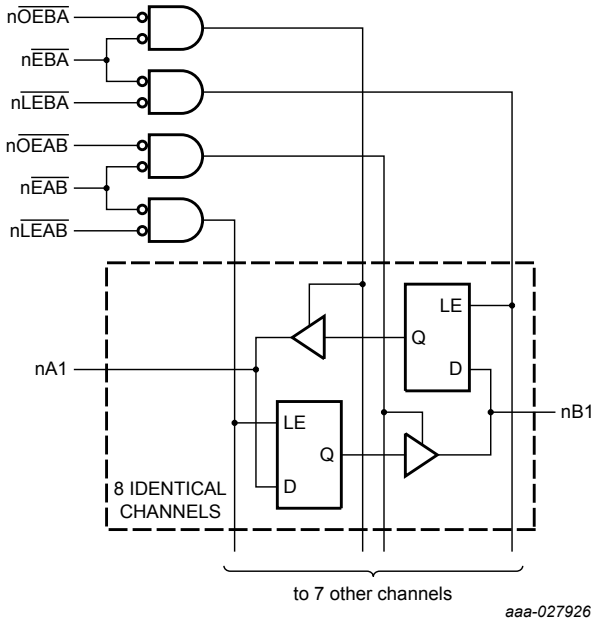


Figure 3. Logic diagram

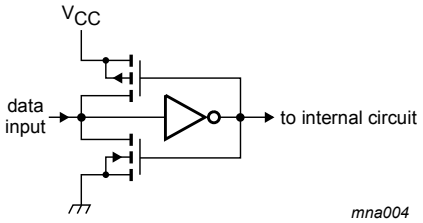


Figure 4. Bushold circuit

5 Pinning information

5.1 Pinning

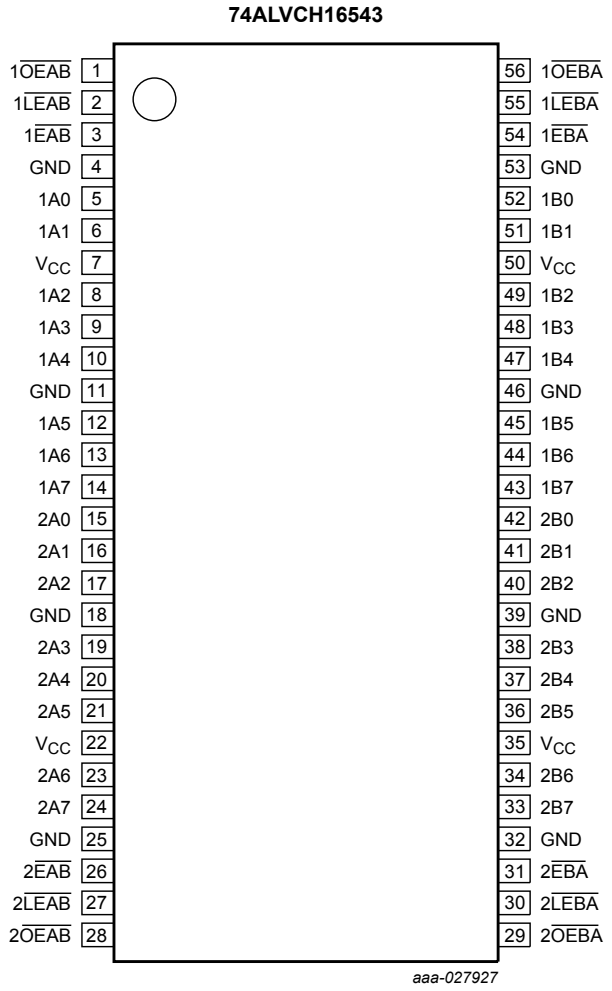


Figure 5. Pin configuration for TSSOP56

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	5, 6, 8, 9, 10, 12, 13, 14	data inputs/outputs
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	15, 16, 17, 19, 20, 21, 23, 24	data inputs/outputs
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	52, 51, 49, 48, 47, 45, 44, 43	data inputs/outputs
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	42, 41, 40, 38, 37, 36, 34, 33	data inputs/outputs
1$\overline{OEAB}$, 2$\overline{OEAB}$	1, 28	A to B output enable inputs (active LOW)
1$\overline{OEBA}$, 2$\overline{OEBA}$	56, 29	B to A output enable inputs (active LOW)
1$\overline{EAB}$, 2$\overline{EAB}$	3, 26	A to B enable inputs (active LOW)
1$\overline{EBA}$, 2$\overline{EBA}$	54, 31	B to A enable inputs (active LOW)
1$\overline{LEAB}$, 2$\overline{LEAB}$	2, 27	A to B latch enable inputs (active LOW)
1$\overline{LEBA}$, 2$\overline{LEBA}$	55, 30	B to A latch enable inputs (active LOW)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6 Functional description

Table 3. Function selection [1]

Inputs				Outputs	Status
nOEAB or nOEBA	nEAB or nEBA	nLEAB or nLEBA	nAn or nBn	nBn or nAn	
H	X	X	X	Z	disabled
X	H	X	X	Z	disabled
L	↑	L	h	Z	disabled + latch
L	↑	L	l	Z	disabled + latch
L	L	↑	h	H	latch + display
L	L	↑	l	L	latch + display
L	L	L	H	H	transparent
L	L	L	L	L	transparent
L	L	H	X	NC	hold

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH transition of nLEAB, nLEBA, nEAB or nEBA;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH transition of nLEAB, nLEBA, nEAB or nEBA;
X = don't care;
↑ = LOW-to-HIGH transition of nLEAB, nLEBA, nEAB or nEBA;
NC = no change;
Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+4.6	V
V_O	output voltage	[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V	-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C [2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		C_L = 30 pF	2.3	2.5	2.7	V
		C_L = 50 pF	3.0	3.3	3.6	V
		low-voltage applications	1.2	2.4	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	-	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	-	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	per data I/O pin; V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	-500	-	-	µA
C_I	input capacitance		-	4.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10 Dynamic characteristics

Table 7. Dynamic characteristics

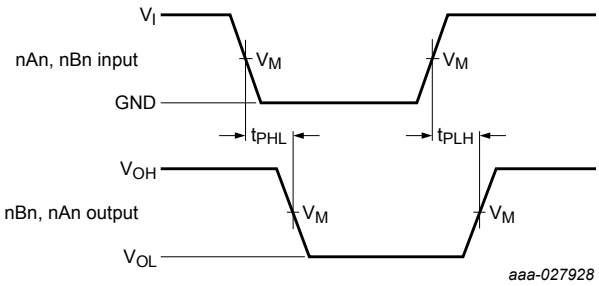
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10. T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{pd}	propagation delay	nAn to nBn; nBn to nAn; see Figure 6 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.4	5.1	ns
		V_{CC} = 2.7 V	-	2.9	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.8	4.3	ns
		$n\overline{LEAB}$ to nBn; $n\overline{LEBA}$ to nAn; see Figure 7				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.3	6.5	ns
		V_{CC} = 2.7 V	-	3.6	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	3.1	5.0	ns
t_{en}	enable time	$n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn; see Figure 8 [3]				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.3	6.8	ns
		V_{CC} = 2.7 V	-	3.4	6.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	5.3	ns
		$n\overline{EBA}$ to nAn; $n\overline{EAB}$ to nBn; see Figure 8				
		V_{CC} = 2.3 V to 2.7 V	1.0	3.3	7.2	ns
		V_{CC} = 2.7 V	-	3.5	6.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0	5.6	ns
t_{dis}	disable time	$n\overline{OEBA}$ to nAn; $n\overline{OEAB}$ to nBn; see Figure 8 [4]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.9	5.7	ns
		V_{CC} = 2.7 V	-	3.3	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.6	ns
		$n\overline{EBA}$ to nAn; $n\overline{EAB}$ to nBn; see Figure 8				
		V_{CC} = 2.3 V to 2.7 V	1.3	3.3	6.1	ns
		V_{CC} = 2.7 V	-	3.5	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	3.3	5.1	ns
t_W	pulse width	$n\overline{LEAB}$, $n\overline{LEBA}$ LOW; see Figure 7				
		V_{CC} = 2.3 V to 2.7 V	3.3	1.2	-	ns
		V_{CC} = 2.7 V	3.3	1.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.3	0.9	-	ns
t_{su}	set-up time	nAn to $n\overline{LEAB}$; nBn to $n\overline{LEBA}$; nAn to $n\overline{EAB}$; nBn to $n\overline{EBA}$; see Figure 9				
		V_{CC} = 2.3 V to 2.7 V	1.2	0.2	-	ns
		V_{CC} = 2.7 V	0.8	0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.1	-	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_h	hold time	nAn to n$\overline{LEAB}$; nBn to n$\overline{LEBA}$; nAn to n$\overline{EAB}$; nBn to n$\overline{EBA}$; see Figure 9				
		V_{CC} = 2.3 V to 2.7 V	1.2	0.2	-	ns
		V_{CC} = 2.7 V	0.4	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	0.2	-	ns
C_{PD}	power dissipation capacitance	per latch; V_I = GND to V_{CC} [5]				
		outputs enabled	-	44	-	pF
		outputs disabled	-	14	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZL} and t_{PZH}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

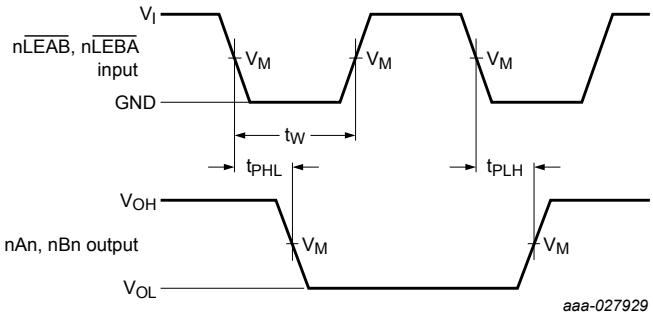
10.1 Waveforms and test circuit



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

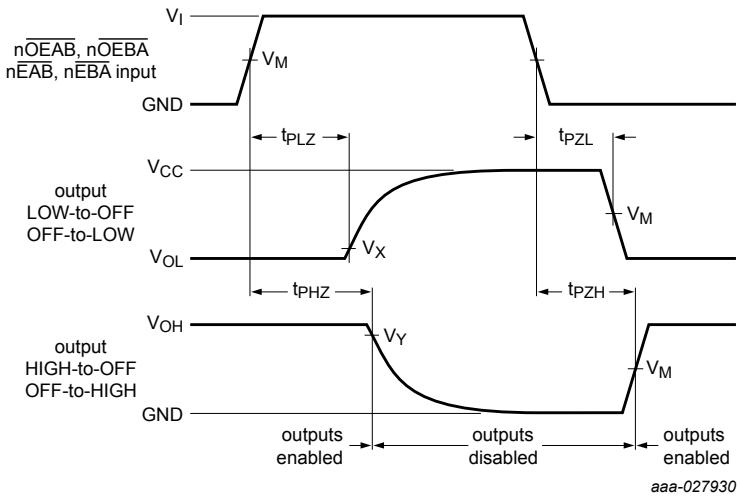
Figure 6. Input (nAn, nBn) to output (nBn, nAn) propagation delays



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

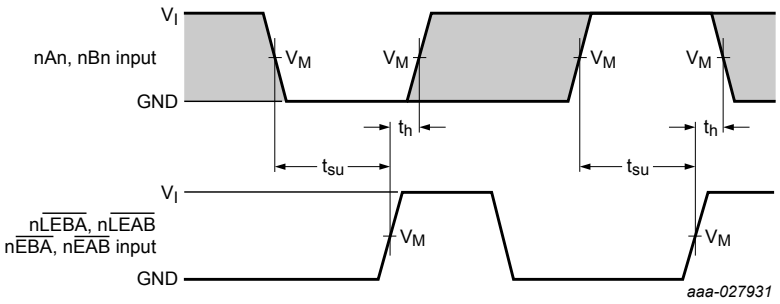
Figure 7. Input ($n\overline{LEAB}$, $n\overline{LEBA}$) to output (nBn, nAn) propagation delays and ($n\overline{LEAB}$, $n\overline{LEBA}$) pulse width



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 8. 3-state output enable and disable times



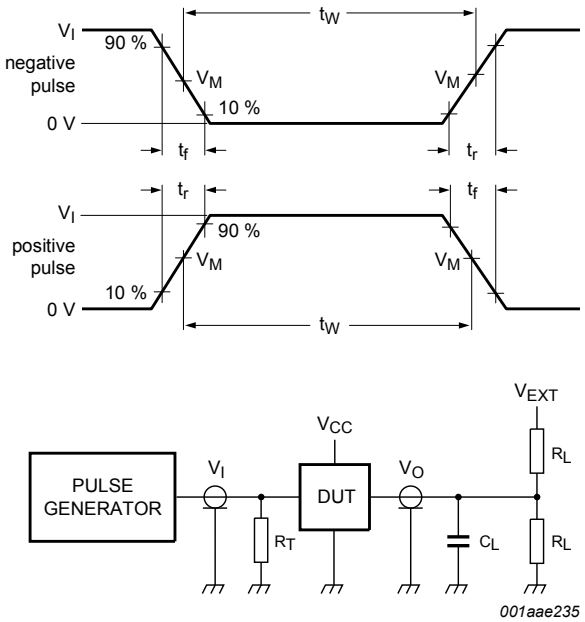
See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 9. Data set-up and hold times for nAn, nBn inputs to nLEBA, nLEAB, nEBA and nEAB inputs

Table 8. Measurement points

Input			Output		
V_{CC}	**V_I**	**V_M**	**V_M**	**V_x**	**V_y**
2.3 V to 2.7 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

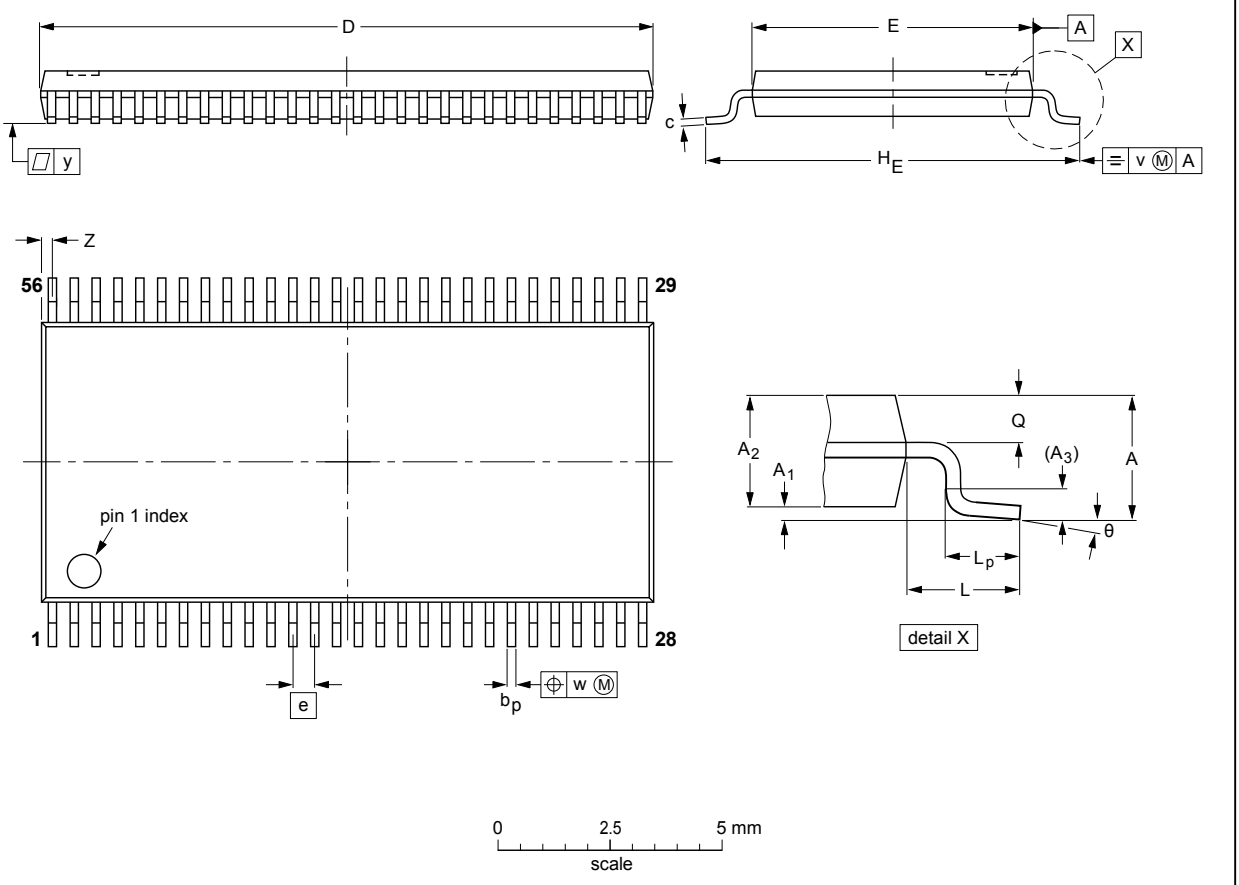
Figure 10. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V_{CC}	open
2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V_{CC}	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V_{CC}	open

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Figure 11. Package outline SOT364-1 (TSSOP56)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16543 v.3	20171215	Product data sheet	-	74ALVCH16543 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVCH16543 v.2	19991123	Product specification	-	74ALVCH16543 v.1
74ALVCH16543 v.1	19980831	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

14.2 Definitions

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