Product data sheet

1. General description

The 74ALVC14 is a hex inverter with Schmitt-trigger inputs.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- · CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

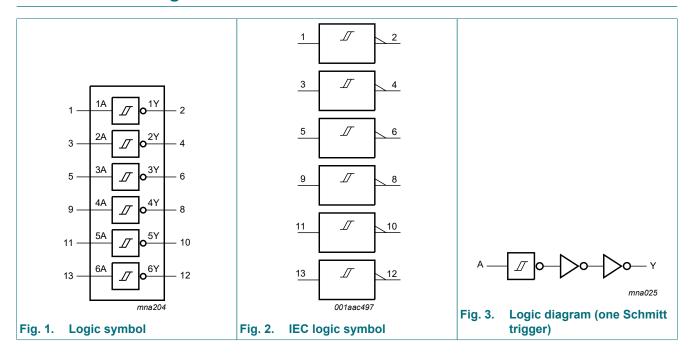
Table 1. Ordering information

Type number	Package	Package						
Temperature range Name		Name	Description	Version				
74ALVC14D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				
74ALVC14PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1				
74ALVC14BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1				



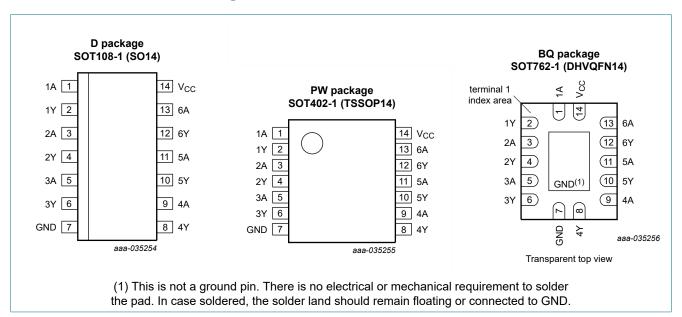
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4. Functional diagram



5. Pinning information

5.1. Pinning



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5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level.$

Input nA	Output nY
L	Н
Н	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
VI	input voltage		[1]	-0.5	+4.6	V
Vo	output voltage	active mode	[1]	-0.5	V _{CC} + 0.5	V
		power-down mode; V _{CC} = 0 V		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V		-	-50	mA
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
I _{O(sink/source)}	output sink or source current	$V_O = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	V _{CC} = 1.65 to 3.6 V	0	V _{CC}	V
		power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature	in free air	-40	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{OH} HIGH-level output		V _I = V _{IH} or V _{IL}						
	voltage	I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.2	-	V
		I _O = -6 mA; V _{CC} = 1.65 V	1.25	1.51	-	1.25	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	1.8	2.10	-	1.8	-	V
		I _O = -18 mA; V _{CC} = 2.3 V	1.7	2.01	-	1.7	-	V
		I _O = -12 mA; V _{CC} = 2.7 V;	2.2	2.53	-	2.2	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	2.76	-	2.4	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	2.68	-	2.2	-	V
V _{OL}	LOW-level output	V _I = V _{IH} or V _{IL}						
	voltage	I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.2	V
		I _O = 6 mA; V _{CC} = 1.65 V	-	0.11	0.3	-	0.3	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.17	0.4	-	0.4	V
		I _O = 18 mA; V _{CC} = 2.3 V	-	0.25	0.6	-	0.6	V
		I _O = 12 mA; V _{CC} = 2.7 V;	-	0.16	0.4	-	0.4	V
		I _O = 18 mA; V _{CC} = 3.0 V	-	0.23	0.4	-	0.45	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.30	0.55	-	0.55	V
I _I	input leakage current	$V_{CC} = 3.6 \text{ V}; V_{I} = 3.6 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 3.6 \text{ V}$	-	±0.1	±10	-	±80	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = V_{CC} \text{ or GND}; I_{O} = 0 \text{ A}$	-	0.2	10	-	80	μΑ
Δl _{CC}	additional supply current	per input pin; $V_{CC} = 3.0 \text{ V}$ to 3.6 V; $V_{I} = V_{CC} - 0.6 \text{ V}$; $I_{O} = 0 \text{ A}$	-	5	750	-	750	μΑ
C _I	input capacitance		-	3.5	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C.

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Hex inverting Schmitt trigger

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 5.

Symbol	Symbol Parameter Conditions			40 °C to +85 °C			-40 °C to +125 °C	
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	2.9	4.4	1.0	5.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.2	3.7	1.0	4.3	ns
		V _{CC} = 2.7 V	1.0	2.8	3.9	1.0	4.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	3.4	1.0	3.9	ns
C _{PD}	power dissipation capacitance	per inverter; V_I = GND to V_{CC} ; [3] V_{CC} = 3.3 V	-	25	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

fo = output frequency in MHz;

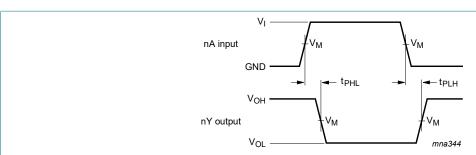
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

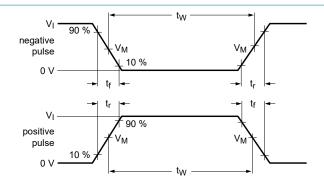
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

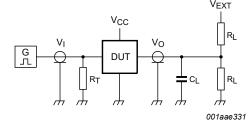
Fig. 4. Input (nA) to output (nY) propagation delays

Table 8. Measurement points

Supply voltage Input			Output
V _{CC}	V _I	V _M	V _M
1.65 V to 1.95 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
2.3 V to 2.7 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V

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Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

 C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

 V_{EXT} = Test voltage for switching times.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Supply voltage Input		Load	Load		
V _{CC}	Vı	t _r , t _f	CL	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

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11. Transfer characteristics

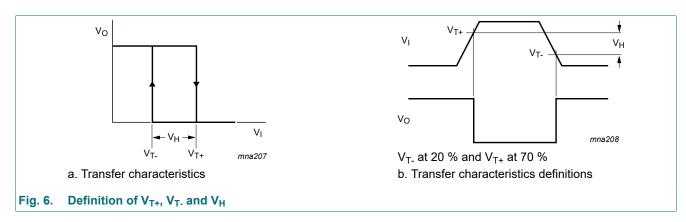
Table 10. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{T+}	positive-going	V _{CC} = 1.65 V	0.7	0.98	1.24	0.7	1.24	V
	threshold voltage	V _{CC} = 1.95 V	0.75	1.12	1.46	0.75	1.46	V
		V _{CC} = 2.3 V	0.9	1.27	1.7	0.9	1.7	V
		V _{CC} = 2.7 V	1.0	1.43	2.0	1.0	2.0	V
		$V_{CC} = 3.0 \text{ V}$ [2]	1.1	1.56	2.0	1.1	2.0	V
		V _{CC} = 3.6 V	1.1	1.81	2.0	1.1	2.0	V
V_{T-}	negative-going threshold voltage	V _{CC} = 1.65 V	0.41	0.64	0.9	0.41	0.9	V
		V _{CC} = 1.95 V	0.49	0.76	1.1	0.49	1.1	V
		V _{CC} = 2.3 V	0.6	0.90	1.3	0.6	1.3	V
		V _{CC} = 2.7 V	0.7	1.06	1.4	0.7	1.4	V
		$V_{CC} = 3.0 \text{ V}$ [2]	0.8	1.19	1.5	0.8	1.5	V
		V _{CC} = 3.6 V	0.8	1.42	1.7	0.8	1.7	V
V _H	hysteresis voltage	V _{CC} = 1.65 V	0.25	0.34	0.62	0.25	0.62	V
		V _{CC} = 1.95 V	0.25	0.36	0.62	0.25	0.62	V
		V _{CC} = 2.3 V	0.3	0.36	1.0	0.3	1.0	V
		V _{CC} = 2.7 V	0.3	0.38	1.1	0.3	1.1	V
		$V_{CC} = 3.0 \text{ V}$ [2]	0.3	0.37	1.2	0.3	1.2	V
		V _{CC} = 3.6 V	0.3	0.40	1.2	0.3	1.2	V

- [1] All typical values are measured at T_{amb} = 25 °C.
 [2] The typical transfer characteristic is displayed in Fig. 7.

11.1. Transfer characteristics waveforms



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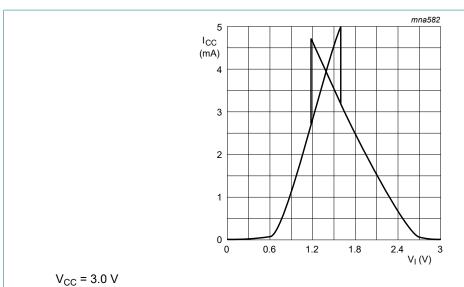
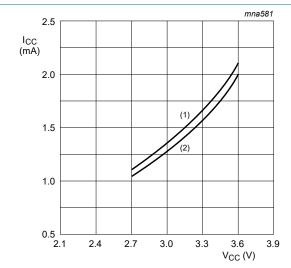


Fig. 7. Typical transfer characteristic

12. Application information

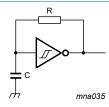


- (1) Positive-going edge.
- (2) Negative going-edge.

Linear change of V_I between 0.8 V to 2.0 V.

All values given are typical unless otherwise specified.

Fig. 8. Average supply current as a function of supply voltage



$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$
 at $V_{CC} = 3.0 \text{ V}$.

Fig. 9. Relaxation oscillator

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13. Package outline

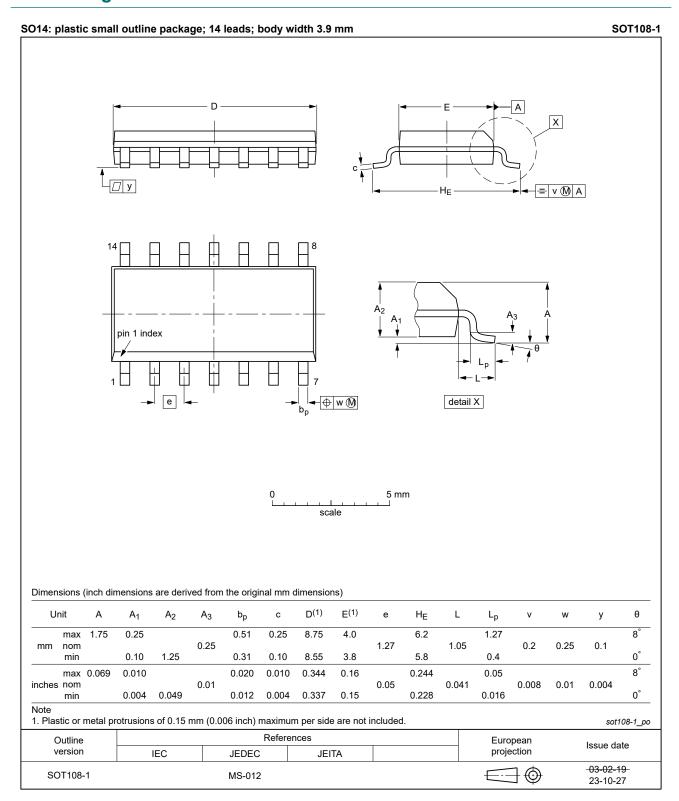


Fig. 10. Package outline SOT108-1 (SO14)

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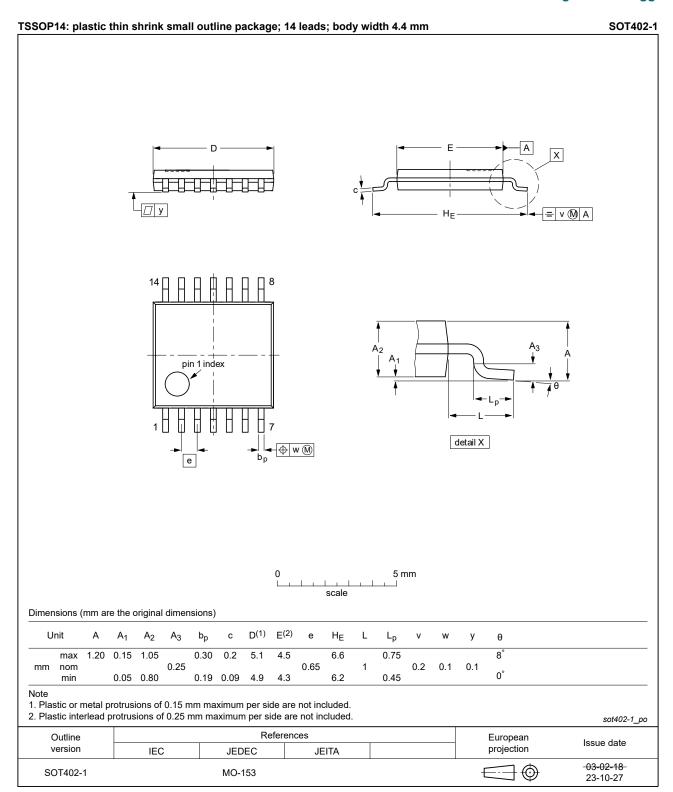


Fig. 11. Package outline SOT402-1 (TSSOP14)

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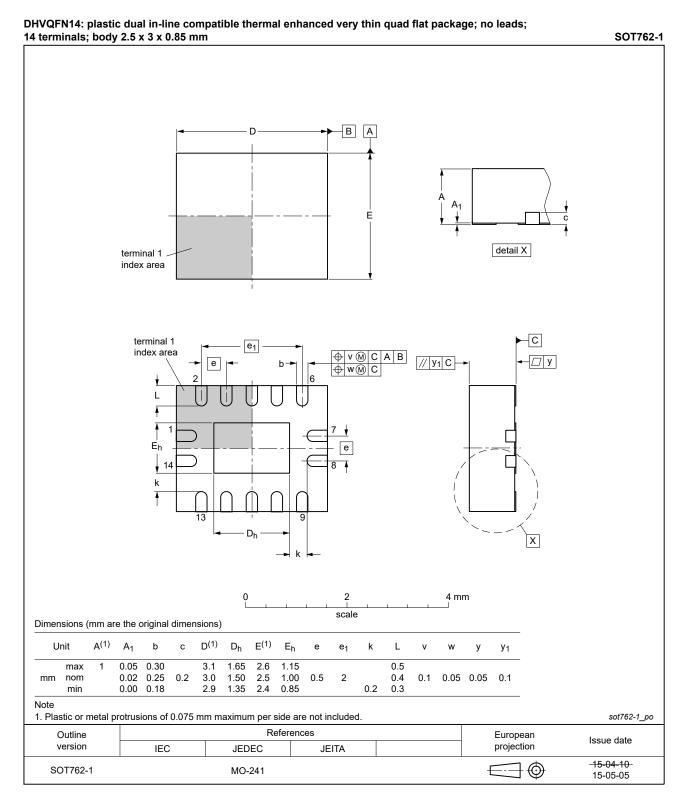


Fig. 12. Package outline SOT762-1 (DHVQFN14)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74ALVC14 v.7	20240112	Product data sheet	-	74ALVC14 v.6.1					
Modifications:	• Fig. 10, Fig. 1 and MO-153	 Fig. 10, Fig. 11: Aligned SO and TSSOP package outline drawings to JEDEC MS-01: and MO-153 							
74ALVC14 v.6.1	20230714	Product data sheet	-	74ALVC14 v.5					
Modifications:		ated; ESD specification up added for T _{amb} = -40 °C t	_	o the latest JEDEC standard.					
74ALVC14 v.5	20210430	Product data sheet	-	74ALVC14 v.4					
Modifications:	• Section 2: Re	 <u>Section 1</u> updated. <u>Section 2</u>: Reference to JESD36 removed. <u>Section 7</u>: Derating values for P_{tot} total power dissipation have been updated. 							
74ALVC14 v.4	20180814	Product data sheet	-	74ALVC14 v.3					
Modifications:	of Nexperia.	this data sheet has been ave been adapted to the no		ply with the identity guidelines where appropriate.					
74ALVC14 v.3	20050215	Product data sheet	-	74ALVC14 v.2					
Modifications:	information st	information standard of Philips Semiconductors.							
74ALVC14 v.2	20030514	Product specification	-	74ALVC14 v.1					
74ALVC14 v.1	20030203	Product specification	-	-					

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16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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