# **74AHC3GU04**

# Triple unbuffered inverter Rev. 6 — 27 February 2019

**Product data sheet** 

# 1. General description

The 74AHC3GU04 is a high-speed Si-gate CMOS device. This device provides three inverter gates with unbuffered outputs.

#### 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101D exceeds 1000 V
- Low power dissipation
- · Balanced propagation delays
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

# 3. Ordering information

#### Table 1. Ordering information

	Table II of acting information						
Type number Package							
		Temperature range	Name	Description	Version		
	74AHC3GU04DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2		
	74AHC3GU04DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1		

### 4. Marking

#### Table 2. Marking codes

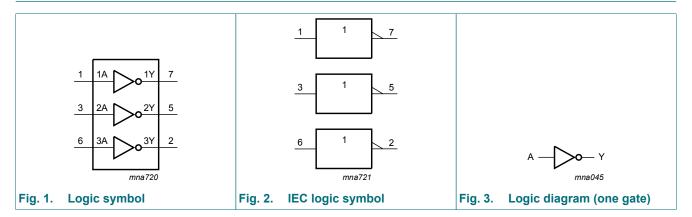
Type number	Marking code [1]
74AHC3GU04DP	AU4
74AHC3GU04DC	AU4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.



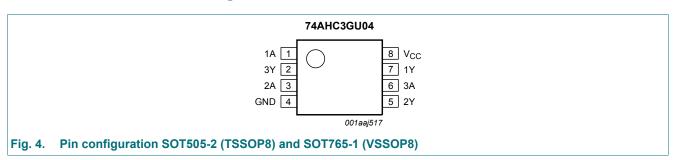
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# 5. Functional diagram



# 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V <sub>CC</sub>	8	supply voltage

# 7. Functional description

#### **Table 4. Function table**

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Υ
L	Н
Н	L

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# 8. Limiting values

#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V}$ [1]	-20	-	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>O</sub>	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$ [2]	-	250	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

#### Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	ns/V

<sup>[2]</sup> For TSSOP8 package: above 55 °C the value of  $P_{tot}$  derates linearly with 2.5 mW/K. For VSSOP8 package: above 110 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

**Triple unbuffered inverter** 

# 10. Static characteristics

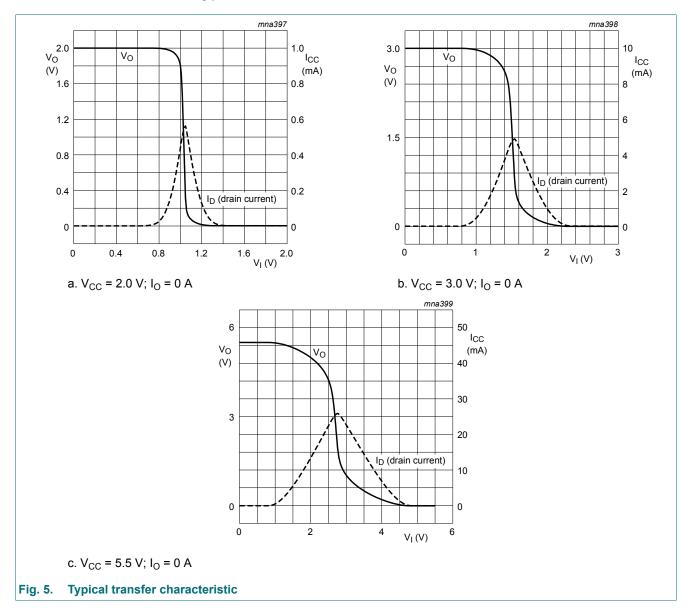
#### **Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

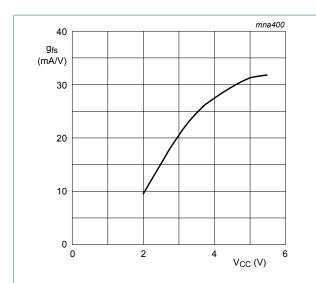
Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C	
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V <sub>CC</sub> = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V <sub>CC</sub> = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O}$ = -4.0 mA; $V_{CC}$ = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		$I_{O}$ = -8.0 mA; $V_{CC}$ = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	μΑ
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

#### Triple unbuffered inverter

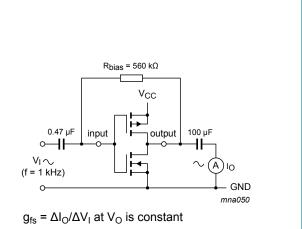
# 10.1. Typical transfer characteristics



#### Triple unbuffered inverter



Typical forward transconductance gfs as a function of the supply voltage at T<sub>amb</sub> = 25 °C



Test set-up for measuring forward Fig. 7. transconductance

# 11. Dynamic characteristics

#### **Table 8. Dynamic characteristics**

GND = 0 V; For test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation	nA to nY; see Fig. 8 [1]								
	delay	V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF [2]	-	3.0	7.1	1.0	8.5	1.0	10.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF [2]	_	4.3	10.6	1.0	12.0	1.0	13.5	ns
		$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 15 pF [3]	-	2.5	5.5	1.0	6.0	1.0	7.0	ns
		$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 50 pF [3]	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C <sub>PD</sub>	power dissipation capacitance	per buffer; $V_1$ = GND to $V_{CC}$ [4]	-	4	-	-	-	-	-	pF

- $t_{\text{pd}}$  is the same as  $t_{\text{PLH}}$  and  $t_{\text{PHL}}.$
- Typical values are measured at  $V_{CC}$  = 3.3 V.
- [2] [3]
- Typical values are measured at  $V_{CC}$  = 5.0 V.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz;

 $f_0$  = output frequency in MHz;

C<sub>1</sub> = output load capacitance in pF;

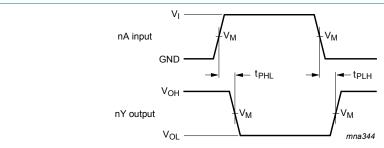
V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of the outputs.

#### Triple unbuffered inverter

#### 11.1. Waveforms and test circuit



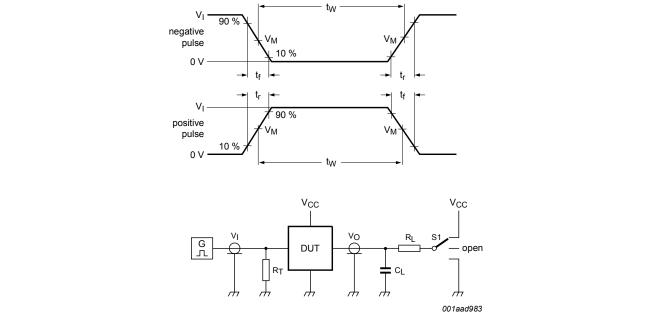
Measurement points are given in Table 9.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig. 8. The input (nA) to output (nY) propagation delays.

**Table 9. Measurement points** 

Input	Output
$V_{M}$	$V_{M}$
0.5V <sub>CC</sub>	0.5V <sub>CC</sub>



Test data is given in Table 10.

Definitions test circuit:

 $R_{T}$  = Termination resistance should be equal to output impedance  $Z_{o}$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

S1 = Test selection switch.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Input		Load		S1 position		
V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
$V_{CC}$	≤ 3 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>

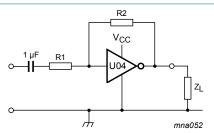
#### Triple unbuffered inverter

# 12. Application information

Some applications are:

- Linear amplifier (see <u>Fig. 10</u>)
- In crystal oscillator design (see Fig. 11)

Remark: All values given are typical unless otherwise specified.



Maximum  $V_{o(p-p)} = V_{CC}$  - 1.5 V centered at 0.5 ×  $V_{CC}$ .

$$G_v = -\frac{G_{\text{ol}}}{1 + \frac{\text{R1}}{\text{R2}} \left(1 + G_{\text{ol}}\right)}$$

Gol = open loop gain

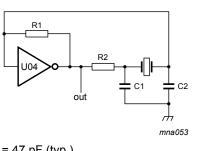
 $G_v$  = voltage gain

 $R1 \ge 3 \text{ k}\Omega, R2 \le 1 \text{ M}\Omega$ 

 $Z_L > 10 \text{ k}\Omega$ ;  $G_{ol} = 20 \text{ (typ.)}$ 

Typical unity gain bandwidth product is 5 MHz.

Fig. 10. Used as a linear amplifier



C1 = 47 pF (typ.)

C2 = 22 pF (typ.)

R1 = 1 M $\Omega$  to 10 M $\Omega$  (typ.)

R2 optimum value depends on the frequency and required stability against changes in  $V_{CC}$  or average minimum  $I_{CC}$  ( $I_{CC}$  is typically 2 mA at  $V_{CC}$  = 3 V and f = 1 MHz).

Fig. 11. Crystal oscillator configuration

Table 11. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 ΜΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 ΜΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 ΜΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 ΜΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 ΜΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	22 ΜΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	22 ΜΩ	47 kΩ	47 pF	5 pF

Table 12. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I <sub>CC</sub>
	8.0 kΩ	minimum influence due to change in V <sub>CC</sub>
6 kHz	1.0 kΩ	minimum required I <sub>CC</sub>
	4.7 kΩ	minimum influence by V <sub>CC</sub>
10 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	2.0 kΩ	minimum influence by V <sub>CC</sub>
14 kHz	0.5 kΩ	minimum required I <sub>CC</sub>
	1.0 kΩ	minimum influence by V <sub>CC</sub>
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

# 13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

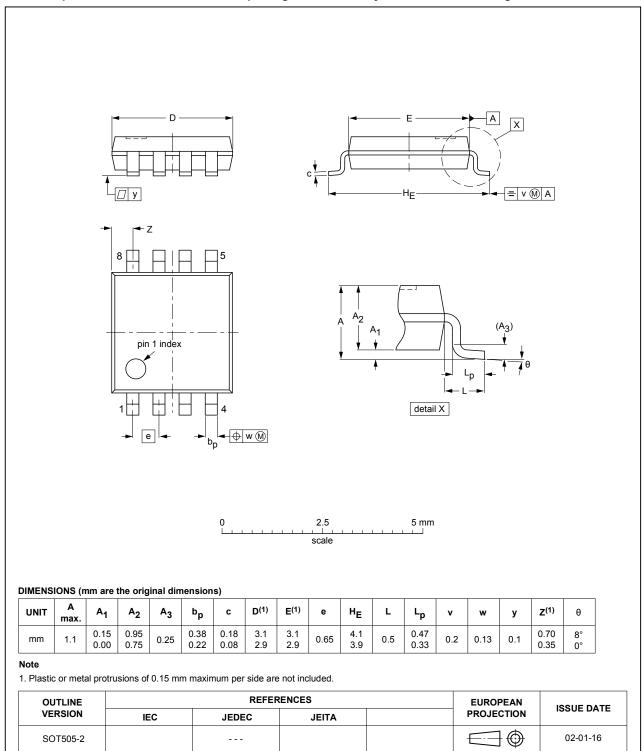


Fig. 12. Package outline SOT505-2 (TSSOP8)

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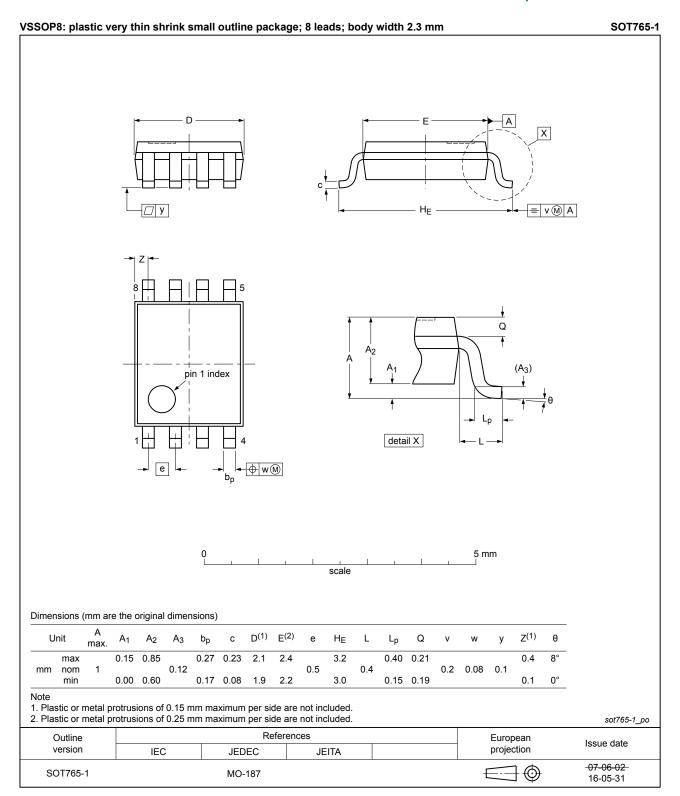


Fig. 13. Package outline SOT765-1 (VSSOP8)

**Triple unbuffered inverter** 

# 14. Abbreviations

#### **Table 13. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 15. Revision history

#### **Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74AHC3GU04 v.6	20190227	Product data sheet	-	74AHC3GU04 v.5	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74AHC3GU04GD (SOT996-2) removed.</li> <li>Package outline drawing SOT765-1 (VSSOP8) updated</li> </ul>				
74AHC3GU04 v.5	20130508	Product data sheet	-	74AHC3GU04 v.4	
Modifications:	For type number 74AHC3GU04GD XSON8U has changed to XSON8.				
74AHC3GU04 v.4	20100107	Product data sheet	-	74AHC3GU04 v.3	
	Marking code for 74AHC3GU04DP package changed from AU04 to AU4				
74AHC3GU04 v.3	20090126	Product data sheet	-	74AHC3GU04 v.2	
74AHC3GU04 v.2	20040923	Product specification	-	74AHC3GU04 v.1	
74AHC3GU04 v.1	20040305	Product specification	-	-	

#### Triple unbuffered inverter

### 16. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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