FEATURES

- **Intel Arria 10 SX Processor**
  - Dual ARM Cortex- A9 MPU
  - Up to 1500 MHz Max clock speed
  - Dual NEON SIMD Coprocessors
  - 32 KB L1 Program Cache (per core)
  - 32 KB L1 Data Cache (per core)
  - 512 KB L2 Cache (shared)
  - 256 KB on-chip RAM
  - Up to 138 User FPGA I/O Pins
  - Up to 30 Shared HPS/FPGA I/O Pins
  - Up to 4 additional HPS Only Pins
  - Twelve 8 Gbps Transceiver Pairs

- **Memory Interfaces**
  - Bank 1 : Up to 4 GB DDR4
    - 32 bits wide
    - 8.5 GB/sec burst transfer rate
    - Shared with HPS
  - Bank 2 : Up to 2 GB DDR4
    - 16 bits wide
    - 4.24 GB/sec burst transfer rate

- Integrated Power Management
- JTAG connector on-module
- On Board USB 2.0 PHY
- On Board MicroSD Card Interface
- Optional eMMC
- On Board RTC
- 2 On Board Temperature Sensors
- Power, Reset and Clock Management

- **FPGA Fabric**
  - Up To 480K Logic Elements (LE)
  - 460Mhz Global Clock
  - Up To 28Mb M20K Memory
  - Up To 4.3Mb MLAB Memory
  - Up To 1368 Floating Point Multipliers
  - Up To 2736 Fixed Point Multipliers
  - 32 Global Clock Networks

- **Serial Transceivers**
  - Twelve 8 Gbps Transceivers
  - 1 x8 PCIe Hard IP Block (Up to Gen 3)
  - 1 x4 Bonded Set

- **Mechanical**
  - 101.5mm (4”) x 101.5mm (4”) size
  - 1 Samtec 320 pin board to board connector
  - 1 Hirose 144 Pin board to board connector
  - 2 Fan Connectors

- **Hard Processor System (HPS)**
  - Up to 3 10/100/1000 Mbps Ethernet MACs
  - 1 USB 2.0 OTG Port
  - Up to 2 UARTs
  - 1 MMC/SD/SDIO
  - Up to 2 SPI Masters and 2 SPI Slaves
  - Up to 5 I2C controllers

APPLICATIONS

- Machine Vision
- Life Science Vision applications
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- Medical Instrumentation

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- Supports OpenCL and HLS acceleration
- High Level OS Support
  - Embedded Linux

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DESCRIPTION

The MitySOM-A10S is a highly configurable, medium form-factor System-on-Module (SOM) featuring an Intel Arria 10 System-on-Chip (SoC). In addition to the processor, the module includes on-board power supplies, two DDR4 RAM memory subsystems, optional eMMC, micro SD card, a fan controller, RTC, a USB 2.0 on the go (OTG) port, and a temperature sensor. The MitySOM-A10S provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-A10S is available with a 270 K Logic Element (KLE) Arria 10 SX which provides Dual-core Cortex-A9 32-bit RISC processors with dual NEON SIMD coprocessors. Options for 160 and 480 KLE devices are also available. This MPU can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux.

Figure 1 illustrates a block diagram of the MitySOM-A10S. As shown in the figure, the primary interface to the MitySOM-A10S is through a 320 Pin and a 144 Pin vertical board-to-board mezzanine connector. The MitySOM-A10S is intended to interface to a carrier card base module for applications development. Details of the board-to-board interfaces are included in the Interface Description section.

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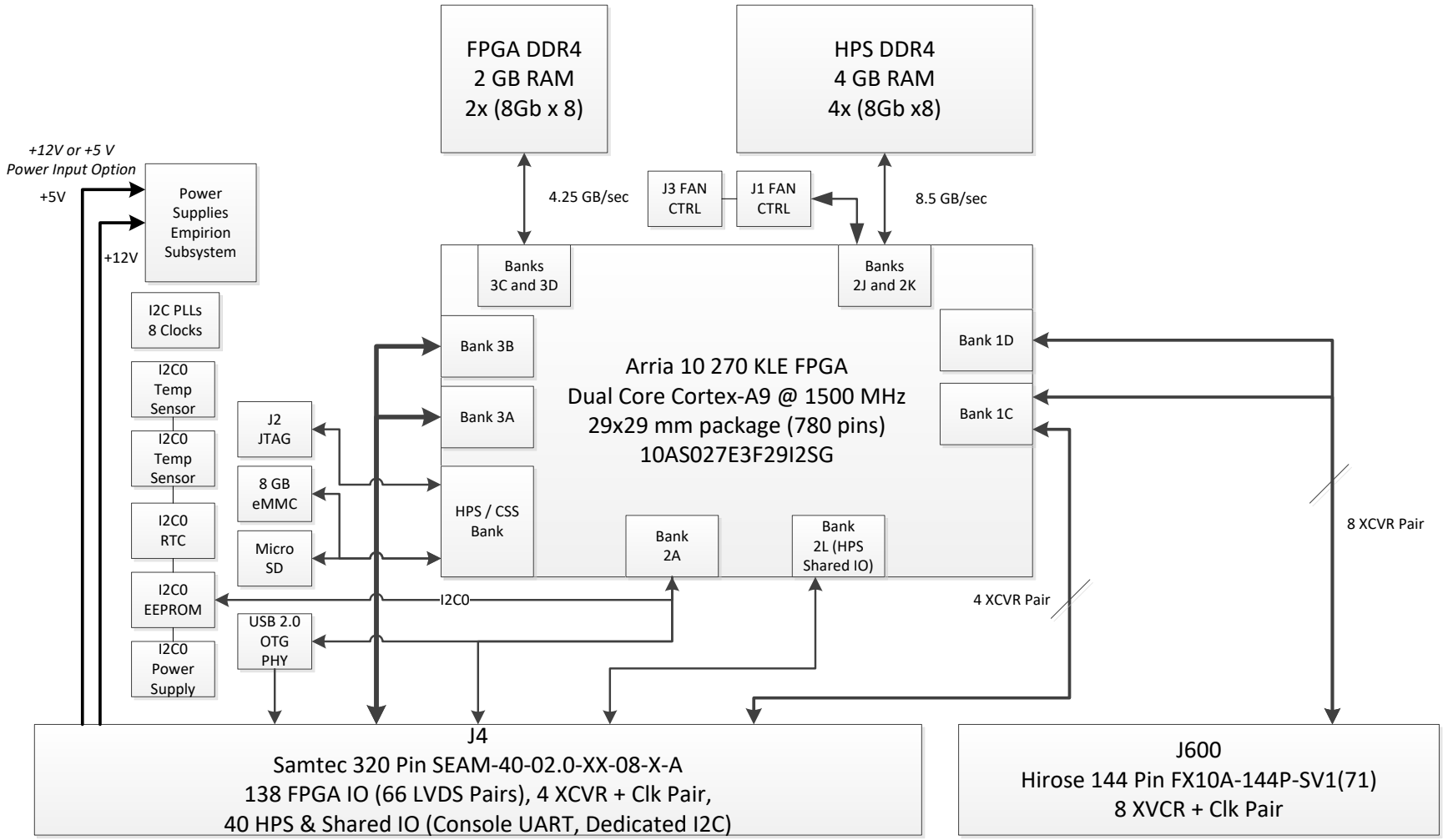

Figure 1 MitySOM-A10S Block Diagram

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DDR4 Memory – HPS Shared Memory

The MitySOM-A10S includes a dedicated 32-bit DDR4 memory interface that can address a maximum of 4GB of RAM. This DDR4 memory is available for both the HPS (Cortex-A9 ARM cores) as well as the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Arria 10.

The MitySOM-A10S family adheres to Intel's Arria 10 maximum memory speeds. The HPS memory is clocked at 1033Mhz by default.

DDR4 Memory – FPGA Memory

The MitySOM-A10S includes a dedicated 16-bit DDR4 memory interface that can address a maximum of 2GB of RAM. This DDR4 memory is available for the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Arria 10. Using an appropriate arbiter is possible to allow HPS access to this memory region.

The MitySOM-A10S family adheres to Intel's Arria 10 maximum memory speeds. The FPGA memory is clocked at 1033Mhz by default.

HPS-FPGA AXI

The high bandwidth HPS-FPGA AXI bridges provided by Intel in the Arria 10 SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® II processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including DDR4 Memory – HPS Shared Memory.

Configuration EEPROM

MitySOM-A10S modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the Arria 10 using the I2C0 interface. This EEPROM contains information such as the module type, Serial Number, and MAC addresses for the Ethernet interface(s). This EEPROM is not available for customer use.

Dedicated HPS Interfaces

The following HPS interfaces have been dedicated as fixed function in order to support proper operation. The module was designed to allow as many HPS fixed and Shared IO pins to be user accessible as possible. See the J4 connector interface description for information on HPS and FPGA Shared IO pins that may be user defined.

Console Serial port

The console serial port (UART1) is supported on pins F40 (RX) and E40 (TX) of the (J4) with 1.8V compatible asynchronous UART I/O. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

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I2C0 Interface

The I2C0 peripheral is consumed local to the module. It is used for the Real Time Clock, Temperature Sensors, and Configuration EEPROM.

Table 1: I2C0 Peripherals

Address	Device	Feature
1010XXX	FT24C16A	16Kbit EEPROM for factory configuration parameters
0110010	AB-RTCMK	Real Time Clock
0011000	LM94235	A10 CPU Temperature sensor
1001000	AT30TS750A	Ambient Board Temperature sensor
1000000	EM2140	Power Supply

I2C EMAC2 Interface

The I2C EMAC 2 peripheral is consumed local to the module. It is used for two quad programmable differential clock generators. The clock generators are used to provide stable clock sources (266 MHz) for the HPS EMIF DDR4 PLL as well as the FPGA EMIF DDR4 PLL.

Table 2: I2C EMAC 2 Peripherals

Address	Device	Feature
1110000	SI5338B	Quad Differential Clock Generator
1110001	SI5338B	Quad Differential Clock Generator

USB-2.0 OTG PHY

The USB1 interface of the Arria 10 processor is connected directly to a USB 2.0 OTG Physical Interface (PHY) on the PCA. The necessary USB ID, power and data pins are available on J4 of the module.

eMMC / MicroSD Card

The MitySOM-A10S HPS SD/MMC controller peripheral is connected via the HPS Bank to a micro-SD (J103) media interface for booting. An option exists for on-board eMMC as well. The eMMC and micro-SD card share the bus using an onboard multiplexed interface. This is the primary interface for booting the module. The default boot device is the microSD card. The A10 can control the selected device via a GPIO control pin to support accessing both devices, one-at-a-time, while running. In addition, the default boot media can be changed to use the eMMC device by default by tying the BOOT_MEDIA_SELECT pin on J4(B) pin 40 to ground.

Debug JTAG

The JTAG interface signals for the Arria 10 FPGA fabric processor have been brought out to a 10-pin dual row TSM-105-01-L-DH-A right angle header, J2. The connector is intended for use with a standard USB 2 Blaster JTAG adapter.

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External Interfaces

The Arria 10 makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go (OTG) port
- Up to 3 Gigabit Ethernet MAC's (10/100/1000 Mbps)
- Up to 4 Serial Peripheral (SPI) ports
- 2 Universal Asynchronous Receive/Transmit (UART) ports
- 3 Inter-Integrated Circuit (I2C) ports (I2C1, I2C EMAC0, I2C EMAC1)
    - I2C0 is connected to on-board devices only including an EEPROM, Power Supply, Temperature Sensors, and RTC and is not available on the external connector interface.
    - I2C EMAC2 is connected to on-board devices only include two SI5338 PLLs and it not available on the external connector interface.
    - I2C1 is dedicated for use on J4(F38/F39) with 2.0k ohm pull-up resistors at 1.8V

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

FPGA Interfaces

GPIO

Up to 138 general FPGA IO pins are available externally to the module. Of these pins, up to 66 LVDS pairs may be configured as transmitters or receivers.

The FPGA IO pins provided on J4(A to H) are connected to Banks 2A, 3A and 3B of the Arria 10 FPGA. All of the I/O banks are connected to 1.8V, and can support mixed standards including LVDS, 1.8V HSTL, and 1.8V single ended logic.

8 Gbps Transceivers

A total of twelve high speed transceiver pairs are available on the module for supporting high speed serial interfaces. 4 of the pairs are routed to J4(A) and J4(B). These 4 pairs may be bonded to support protocols such as HDMI, CoaXpress, etc. The remaining 8 pairs, which may be bonded to a hard Gen 3 compliant PCIe controller core, are routed to J600. There is one hard Gen 3 compliant PCIe controller. The controller may be bonded to either the 8 pairs or 4 pairs or not at all. The module includes a local PLL clock circuit that may be used for a reference clock source for use with the transceiver logic, or a reference clock may be provided externally.

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Configuration and Boot Modes

The Arria 10 has two groups of pins, documented below, that are read during reset to determine which media to boot from for the HPS (BSEL pins) and one group of pins that is used to configure the FPGA (MSEL pins). On the MitySOM-A10S, the BSEL, and MSEL pins are strapped to fixed settings on board as described below. There is also a set of user-programmable fuses stored in the HPS_fusesec register of the Arria 10. The HPS_fusesec fuses are not modified by Critical Link and will be at the default values outlined in the Intel Arria 10 Hard Processor System Technical Reference Manual. The MitySOM provides a local 50 MHz clock source to the HPS_CLK1 pin for HPS booting purposes.

Boot Media Configuration

The Arria 10 is configurated to boot from its MMC/SD interface, which is a BSEL of 0x4. This will be the MicroSD card or eMMC based on how the BOOT_MEDIA_SELECT pin is strapped on start up. For boot from MicroSD card this is already pulled up on the MitySOM. To boot from the eMMC this signal will need to be pulled down on the carrier card.

FPGA MSEL [2:0] Configuration Pins

The FPGA MSEL configuration input pins are set to [2:0] ‘001’b. They are pulled up/down to 1.8V or ground with 1.0K resistors on the MitySOM-A10S, selecting the Fast Passive Parallel (FPP) x16 mode. The FPGA should be configured using either the HPS internal FPGA manager or optionally using the JTAG interface.

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Debug LEDs

There are 4 debug LEDs on the MitySOM-A10S module.

Power Status LEDs

D1 illuminates when there is power applied to the MitySOM-A10S.

D4 indicates the MitySOM-A10S on-module power supplies have been enabled in sequence and are operating correctly.

Configuration Debug

D2 is connected to the nSTATUS pin on the FPGA. When lit, it indicates a programming error occurred during FPGA fabric configuration.

D3 is connected to the CONF_DONE pin on the FPGA. When lit, it indicates that FPGA configuration is not complete by lighting a yellow LED. This is only a warning rather than an error because the HPS can still boot and load the FPGA. This LED should turn on during initial power up until the FPGA is programmed.

Power Interfaces

The MitySOM-A10S is powered using the +5V DC (+5VIN) input and ground pins on J4. The MitySOM-A10S processor generates +3.3V, +2.5V, +1.8V, +1.2V, +0.6V, 0.9V and +0.95V core voltages.

An option exists to power using the +12V DC (+12VIN) input and ground pins on J4. If interested in this option contact Critical Link at info@criticallink.com. . When +12VIN is used, the MitySOM-A10S processor generates +5V, +3.3V, +2.5V, +1.8V, +1.2V, +0.6V, 0.9V and +0.95V core voltages. ***NOTE***: +12V and +5V inputs must not be supplied to the module at the same time.

The state of the local power supplies is provided on J4 (F2) via the POK signal. Until this signal is asserted the local FPGA power supplies should not be assumed to be on and stable. This signal should be used to sequence or enable any user IO to the module.

Software and FPGA Development Support

Users of the MitySOM-A10S are encouraged to develop applications using the GCC based MitySOM-A10S software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Intel platform support package for the Arria 10 and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

FPGA developers should use the Intel FPGA Quartus Design Suite when working with the MitySOM-A10S.

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Growth Options

The MitySOM-A10S has been designed to support several upgrade options. These options include a range of speed grades, FPGA density, HPS DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a configuration not listed below, please contact a Critical Link sales representative.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office (info@criticallink.com) or unit Distributors for availability and specifications.

Table 3: Absolute Maximum Ratings

Maximum Supply Voltage (+5VIN)	5.5 V
Maximum Supply Voltage (+12VIN)	13.2 V
Storage Temperature Range	-55°C to 150°C

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-A10S. For specifications not contained in this table please contact a Critical Link sales representative.

Table 4: Module Component Temperature Ratings

Temperature Range	**Component Ratings***
Commercial (-RC)	0°C to 70°C
Industrial (-RI)	-40°C to 85°C

* ***Please see the Thermal Management section below for ambient/operating temperature recommendations.***

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Thermal Management

The MitySOM-A10S module requires careful consideration of thermal management. Depending on load, different thermal management will be required for operation at room temperatures and above. The primary thermal concern is with the Arria 10 SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-A10S.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. Customers should use Intel's Early Power Estimator (EPE) for the Arria 10. This utility will assist in estimating the potential power usage of the processor for a given application. Details can be found on the PowerPlay EPE[1] page at Altera.com. To achieve reliable operation at the maximum specified operating temperatures it has been determined that some form of thermal management (e.g., forced air, heat sink, etc.) will be required.

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J1, J2 and J4 Connector Interfaces

The next sections outline the J1, J2 and J3 connector pin interfaces.

J1 Interface Description

The connector for J1, is a JST S4B-ZR-SM4A-TF(LF)(SN). The interface is designed to mate with a +5V DC cooling fan and supports pulse width modulation of the supply voltage as well as a tachometer pulse readback circuit. The interface pin out is described in the table below.

Table 5 J-1 Connector Pin Assignments

Pin	Name	I/O	Description
1	+5V	Output	+5V DC Output
2	FAN_TACH	Input	+5V logic input. Includes +1K pullup to support Open Drain Tach outputs
3	GND	Input	+5V DC Current return
4	FAN_PWM	Output	+5V logic PWM signal connected to FPGA

J2 Interface Description

The connector for J2, is a TSM-105-01-L-DH-A, a 0.1" 5x2 dual row male header interface. The interface is designed to mate with a USB Blaster II JTAG interface pod according to Intel's UG-USB81204 specifications for USB-Blaster Download Cable. The interface is described in the table below.

Table 6 J2 Connector Pin Assignments

Pin	Name	I/O	Description
1	GND	Input	Signal Ground
2	TDI	Input	Data to Device. Pulled to 1.8V via 10K resistor
3	JTAG_TRST	Input	JTAG TRST Signal. Pulled to 1.8V via 1K resistor
4	NC	-	No Connect / Key
5	NC	-	No Connect
6	TMS	Input	JTAG State Machine Control (pulled to 1.8V with 10Kresistor)
7	+1V8	Output	Target Power Supply from Module.
8	TDO	Output	Data From Device
9	GND	Input	Signal Ground
10	TCK	Input	Clock Signal (pulled to GND with 1.8K resistor)

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J3 Interface Description

The connector for J3, is a Molex 22-12-2024. The interface is designed to mate with a +5V DC cooling fan and supports pulse width modulation of the supply. The interface pin out is described in the table below.

Table 7 J-3 Connector Pin Assignments

Pin	Name	I/O	Description
1	FAN_PWM	Output	+5V logic PWM signal connected to FPGA
2	GND	Input	+5V DC Current return.

J4 and J100 Connector Interfaces

The next sections outline the connector pin interfaces. The pin interfaces are grouped into the signal classes defined in the table below.

Class	Applicable IO Standard	Description
POWER	N/A	These are module power input pins and corresponding return pins.
XCVR_TX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Transmit lanes of the Arria 10. VCCT is set to 0.95V for all transceiver banks.
XCVR_RX	CML, Differential LVPECL, LVDS, HCSL	These pins are directly connected to the Gigabit Transceiver Receive lanes of the Arria 10. CML, Differential LVPECL, and LVDS must be AC Coupled. VCCR is set to 0.95V for all transceiver banks.
XCVR_REFCLK	CML Differential LVPECL, LVDS	These pins are directly connected to the Gigabit Transceiver Reference input clocks.
IO_1V8	1.8V CMOS	These pins are directly connected to FPGA Bank IO pins, but cannot be used for LVDS IO. The Bank voltage is 1.8 V.
LVDSIO_1V8	LVDS, 1.8V CMOS, SSTL-18, HSTL-18	These pins are directly connected to FPGA Bank IO pins that may be configured for LVDS IO. The bank voltage is 1.8 volts.
SHAREDIO_1V8	1.8V CMOS	These pins are connected to shared FPGA or HPS pins in one of the Arria 10 HPS shared bank quadrants. The bank voltage for these pins are 1.8 V.
FFIO_1V8	1.8V CMOS	These are fixed function pins. See the interface description for details.
FFIO	Various	These are fixed function pins. See the interface description for details.
HPSIO_1V8	1.8V CMOS	These pins are connected to the HPS bank IO pins. The bank voltage for these pins is 1.8V.
CLKOUT	LVDS or CML	These pins are directly connected to a local si5338B phase locked loop chip output driver and may be used for external clock generation.

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J4 Interface Description

The connector used for J4 is a 320 Pin Samtec SEAM series connector, SEAM-40-03.5-S-08-2-A-K-TR, which mates with Samtec SEAF-40-06.5-L-08-1-A-K-TR (the mating height, indicated by the 06.5 in the part number may be taller if desired but must match total height of J600). The connector is logically broken up into 8 groups of 40 pins as documented below.

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Table 8 to Table 15 contain a summary of the MitySOM-A10S J4 Interface pin-mapping.

For more information about pin definitions and pin connection guidelines please refer to the Arria 10 Device Family Pin Connection Guidelines.

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Table 8: MitySOM-A10S J4(A) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
A1	POWER	+12VIN	-	-	
A2	POWER	GND	-	-	
A3	XCVR_TX	GXB_TX_3_N	1C	AA27	GXBL1C_TX_CH3n
A4	XCVR_TX	GXB_TX_3_P	1C	AA28	GXBL1C_TX_CH3p
A5	POWER	GND	-	-	
A6	POWER	GND	-	-	
A7	XCVR_TX	GXB_TX_2_N	1C	AC27	GXBL1C_TX_CH2n
A8	XCVR_TX	GXB_TX_2_P	1C	AC28	GXBL1C_TX_CH2p
A9	POWER	GND	-	-	
A10	POWER	GND	-	-	
A11	XCVR_TX	GXB_TX_1_N	1C	AE27	GXBL1C_TX_CH1n
A12	XCVR_TX	GXB_TX_1_P	1C	AE28	GXBL1C_TX_CH1p
A13	POWER	GND	-	-	
A14	POWER	GND	-	-	
A15	XCVR_TX	GXB_TX_0_N	1C	AG27	GXBL1C_TX_CH0n
A16	XCVR_TX	GXB_TX_0_P	1C	AG28	GXBL1C_TX_CH0p
A17	POWER	GND	-	-	
A18	POWER	GND	-	-	
A19	XCVR_REFCLK	GXB_REFCLK1_N	-	-	si5338B phase locked loop chip output
A20	XCVR_REFCLK	GXB_REFCLK1_P	-	-	si5338B phase locked loop chip output
A21	POWER	GND	-	-	
A22	LVDSIO_1V8	B3A_LVDS_B17_P	3A	AG1	LVDS3A_17p
A23	LVDSIO_1V8	B3A_LVDS_B17_N	3A	AF1	LVDS3A_17n
A24	POWER	GND	-	-	
A25	LVDSIO_1V8	B3A_LVDS_B2_N	3A	W7	LVDS3A_2n
A26	LVDSIO_1V8	B3A_LVDS_B2_P	3A	W8	LVDS3A_2p
A27	POWER	GND	-	-	
A28	LVDSIO_1V8	B3B_LVDS_B24_P	3B	W3	LVDS3B_24p
A29	LVDSIO_1V8	B3B_LVDS_B24_N	3B	V3	LVDS3B_24n
A30	POWER	GND	-	-	
A31	LVDSIO_1V8	B3B_LVDS_B3_N	3B	T7	LVDS3B_3n
A32	LVDSIO_1V8	B3B_LVDS_B3_P	3B	T6	LVDS3B_3p
A33	POWER	GND	-	-	
A34	LVDSIO_1V8	B3B_LVDS_B11_P	3B	K2	LVDS3B_11p/RZQ_3B
A35	LVDSIO_1V8	B3B_LVDS_B11_N	3B	J2	LVDS3B_11n
A36	POWER	GND	-	-	
A37	SHAREDIO_1V8	GPIO0_IO6	2L	E19	GPIO0_IO6,NAND_ADQ3,UART1_TX,USB0_DATA2,SDMMC_DATA4,SPIM0_MISO,EMAC2_MDIO,I2C_EMAC2_SDA
A38	SHAREDIO_1V8	GPIO1_IO17	2L	F18	GPIO1_IO17,NAND_ADQ9,UART1_RTS_N,QSPI_SS3,EMAC2_TXD1,SDMMC_DATA3,SPIM0_SS1_N
A39	SHAREDIO_1V8	GPIO1_IO15	2L	H18	GPIO1_IO15,UART1_RX,Trace_CLK,EMAC2_RX_CTL,SDMMC_DATA1
A40	SHAREDIO_1V8	GPIO0_IO7	2L	F19	GPIO0_IO7,NAND_CLE,UART1_RX,USB0_DATA3,SDMMC_DATA5,SPIM0_SS0_N,EMAC2_MDC,I2C_EMAC2_SCL

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Table 9: MitySOM-A10S J4(B) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
B1	POWER	+12VIN	-	-	
B2	POWER	GND	-	-	
B3	POWER	GND	-	-	
B4	POWER	GND	-	-	
B5	XCVR_RX	GXB_RX_3_P	1C	Y26	GXBL1C_RX_CH3p,GXBL1C_REFCLK3p
B6	XCVR_RX	GXB_RX_3_N	1C	Y25	GXBL1C_RX_CH3n,GXBL1C_REFCLK3n
B7	POWER	GND	-	-	
B8	POWER	GND	-	-	
B9	XCVR_RX	GXB_RX_2_P	1C	AB26	GXBL1C_RX_CH2p,GXBL1C_REFCLK2p
B10	XCVR_RX	GXB_RX_2_N	1C	AB25	GXBL1C_RX_CH2n,GXBL1C_REFCLK2n
B11	POWER	GND	-	-	
B12	POWER	GND	-	-	
B13	XCVR_RX	GXB_RX_1_P	1C	AD26	GXBL1C_RX_CH1p,GXBL1C_REFCLK1p
B14	XCVR_RX	GXB_RX_1_N	1C	AD25	GXBL1C_RX_CH1n,GXBL1C_REFCLK1n
B15	POWER	GND	-	-	
B16	POWER	GND	-	-	
B17	XCVR_RX	GXB_RX_0_P	1C	AF26	GXBL1C_RX_CH0p,GXBL1C_REFCLK0p
B18	XCVR_RX	GXB_RX_0_N	1C	AF25	GXBL1C_RX_CH0n,GXBL1C_REFCLK0n
B19	POWER	GND	-	-	
B20	POWER	GND	-	-	
B21	LVDSIO_1V8	B3A_LVDS_B10_N	3A	AB3	LVDS3A_10n
B22	LVDSIO_1V8	B3A_LVDS_B10_P	3A	AA2	LVDS3A_10p
B23	POWER	GND	-	-	
B24	LVDSIO_1V8	B3A_LVDS_B16_P	3A	AE2	LVDS3A_16p
B25	LVDSIO_1V8	B3A_LVDS_B16_N	3A	AD2	LVDS3A_16n
B26	POWER	GND	-	-	
B27	LVDSIO_1V8	B3A_LVDS_B1_N	3A	Y4	LVDS3A_1n
B28	LVDSIO_1V8	B3A_LVDS_B1_P	3A	W4	LVDS3A_1p
B29	POWER	GND	-	-	
B30	LVDSIO_1V8	B3B_LVDS_B5_N	3B	U5	LVDS3B_5n
B31	LVDSIO_1V8	B3B_LVDS_B5_P	3B	T4	LVDS3B_5p
B32	POWER	GND	-	-	
B33	LVDSIO_1V8	B3B_LVDS_B17_P	3B	L1	LVDS3B_17p
B34	LVDSIO_1V8	B3B_LVDS_B17_N	3B	K1	LVDS3B_17n
B35	POWER	GND	-	-	
B36	SHAREDIO_1V8	GPIO1_IO13	2L	G19	GPIO1_IO13,NAND_RB,EMAC2_TX_CTL,SDMMC_CMD,I2C1_SCL
B37	SHAREDIO_1V8	GPIO0_IO11	2L	D18	GPIO0_IO11,NAND_ADQ7,USB0_DATA7,SPIM1_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL
B38	SHAREDIO_1V8	GPIO1_IO22	2L	H17	GPIO1_IO22,NAND_ADQ14,Trace_D2,EMAC2_RXD2,SPIM0_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
B39	SHAREDIO_1V8	GPIO1_IO16	2L	F17	GPIO1_IO16,NAND_ADQ8,UART1_CTS_N,QSPI_SS2,EMAC2_TXD0,SDMMC_DATA2
B40	FFIO_1V8	BOOT_MEDIA_SELECT	-	-	connect to GND for eMMC, on SOM pull-up to default boot from SD card

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Table 10: MitySOM-A10S J4(C) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
C1	POWER	+12VIN	-	-	
C2	POWER	GND	-	-	
C3	LVDSIO_1V8	B2A_LVDS_B10_N	2A	AE20	PLL_2A_CLKOUT1n/LVDS2A_10n
C4	LVDSIO_1V8	B2A_LVDS_B10_P	2A	AE19	PLL_2A_CLKOUT1p/LVDS2A_10p
C5	POWER	GND	-	-	
C6	POWER	GND	-	-	
C7	LVDSIO_1V8	B2A_LVDS_B2_P	2A	AE15	LVDS2A_2p
C8	LVDSIO_1V8	B2A_LVDS_B2_N	2A	AE14	LVDS2A_2n
C9	POWER	GND	-	-	
C10	POWER	GND	-	-	
C11	LVDSIO_1V8	B2A_LVDS_B5_P	2A	AF12	LVDS2A_5p
C12	LVDSIO_1V8	B2A_LVDS_B5_N	2A	AF11	LVDS2A_5n
C13	POWER	GND	-	-	
C14	POWER	GND	-	-	
C15	LVDSIO_1V8	B3A_LVDS_B22_P	3A	AF6	LVDS3A_22p
C16	LVDSIO_1V8	B3A_LVDS_B22_N	3A	AE6	LVDS3A_22n
C17	POWER	GND	-	-	
C18	POWER	GND	-	-	
C19	POWER	GND	-	-	
C20	LVDSIO_1V8	B3A_LVDS_B7_P	3A	AC5	LVDS3A_7p
C21	LVDSIO_1V8	B3A_LVDS_B7_N	3A	AB4	LVDS3A_7n
C22	POWER	GND	-	-	
C23	LVDSIO_1V8	CLK3A_P	3A	AA6	LVDS3A_12p/CLK_3A_1p
C24	LVDSIO_1V8	CLK3A_N	3A	AA7	LVDS3A_12n/CLK_3A_1n
C25	POWER	GND	-	-	
C26	LVDSIO_1V8	B3A_LVDS_B5_N	3A	Y2	LVDS3A_5n
C27	LVDSIO_1V8	B3A_LVDS_B5_P	3A	Y1	LVDS3A_5p
C28	POWER	GND	-	-	
C29	LVDSIO_1V8	B3B_LVDS_B23_P	3B	W2	LVDS3B_23p
C30	LVDSIO_1V8	B3B_LVDS_B23_N	3B	V2	LVDS3B_23n
C31	POWER	GND	-	-	
C32	LVDSIO_1V8	CLK3B_N	3B	L3	LVDS3B_12n/CLK_3B_1n
C33	LVDSIO_1V8	CLK3B_P	3B	L2	LVDS3B_12p/CLK_3B_1p
C34	POWER	GND	-	-	
C35	LVDSIO_1V8	B3B_LVDS_B10_N	3B	J3	PLL_3B_CLKOUT1n/LVDS3B_10n
C36	LVDSIO_1V8	B3B_LVDS_B10_P	3B	H2	PLL_3B_CLKOUT1P/LVDS3B_10p
C37	POWER	GND	-	-	
C38	SHAREDIO_1V8	GPIO1_IO19	2L	K17	GPIO1_IO19,NAND_ADQ11,Trace_CLK,EMAC2_RXD1,SDMMC_DATA5,SPIM0_SS0_N,EMAC1_MDC,I2C_EMAC1_SCL
C39	SHAREDIO_1V8	GPIO1_IO18	2L	J17	GPIO1_IO18,NAND_ADQ10,EMAC2_RXD0,SDMMC_DATA4,SPIM0_MISO,EMAC1_MDIO,I2C_EMAC1_SDA
C40	SHAREDIO_1V8	GPIO1_IO20	2L	J18	GPIO1_IO20,NAND_ADQ12,Trace_D0,EMAC2_TXD2,SDMMC_DATA6,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA

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Table 11: MitySOM-A10S J4(D) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
D1	POWER	+5VIN	-	-	
D2	FFIO	T_ALERT	-	-	This pin is connected to the open drain active low T_CRIT output pin on a local LM95235 temperature sensor, and is asserted on Arria 10 over temperature conditions.
D3	POWER	GND	-	-	
D4	LVDSIO_1V8	B2A_LVDS_B7_N	2A	AF19	LVDS2A_7n
D5	LVDSIO_1V8	B2A_LVDS_B7_P	2A	AG18	LVDS2A_7p
D6	POWER	GND	-	-	
D7	LVDSIO_1V8	B2A_LVDS_B6_N	2A	AD14	LVDS2A_6n
D8	LVDSIO_1V8	B2A_LVDS_B6_P	2A	AD13	LVDS2A_6p
D9	POWER	GND	-	-	
D10	LVDSIO_1V8	B2A_LVDS_B1_P	2A	AE11	LVDS2A_1p
D11	LVDSIO_1V8	B2A_LVDS_B1_N	2A	AE10	LVDS2A_1n
D12	POWER	GND	-	-	
D13	LVDSIO_1V8	B3A_LVDS_B21_N	3A	AC7	LVDS3A_21n
D14	LVDSIO_1V8	B3A_LVDS_B21_P	3A	AC6	LVDS3A_21p
D15	POWER	GND	-	-	
D16	LVDSIO_1V8	B3A_LVDS_B24_P	3A	AE5	LVDS3A_24p
D17	LVDSIO_1V8	B3A_LVDS_B24_N	3A	AD5	LVDS3A_24n
D18	POWER	GND	-	-	
D19	LVDSIO_1V8	B3A_LVDS_B20_P	3A	AE4	LVDS3A_20p
D20	LVDSIO_1V8	B3A_LVDS_B20_N	3A	AD4	LVDS3A_20n
D21	POWER	GND	-	-	
D22	LVDSIO_1V8	B3A_LVDS_B8_P	3A	AB1	LVDS3A_8p
D23	LVDSIO_1V8	B3A_LVDS_B8_N	3A	AA1	LVDS3A_8n
D24	POWER	GND	-	-	
D25	LVDSIO_1V8	B3A_LVDS_B6_N	3A	AA8	LVDS3A_6n
D26	LVDSIO_1V8	B3A_LVDS_B6_P	3A	AA9	LVDS3A_6p
D27	POWER	GND	-	-	
D28	LVDSIO_1V8	B3B_LVDS_B22_N	3B	V6	LVDS3B_2n
D29	LVDSIO_1V8	B3B_LVDS_B22_P	3B	V5	LVDS3B_22p
D30	POWER	GND	-	-	
D31	LVDSIO_1V8	B3B_LVDS_B8_P	3B	K4	LVDS3B_8p
D32	LVDSIO_1V8	B3B_LVDS_B8_N	3B	L4	LVDS3B_8n
D33	POWER	GND	-	-	
D34	LVDSIO_1V8	B3B_LVDS_B7_N	3B	M4	LVDS3B_7n
D35	LVDSIO_1V8	B3B_LVDS_B7_P	3B	M3	LVDS3B_7p
D36	POWER	GND	-	-	
D37	SHAREDIO_1V8	GPIO1_IO14	2L	G18	GPIO1_IO14,NAND_CE_N,UART1_TX,EMAC2_RX-CLK,SDMMC_CCLK
D38	SHAREDIO_1V8	GPIO0_IO1	2L	D17	GPIO0_IO1,NAND_ADQ1,UART0_RTS_N,USB0_STP,SDMMC_CMD,SPIM1_SS1_N,SPIS0_MOSI
D39	SHAREDIO_1V8	GPIO1_IO21	2L	J19	GPIO1_IO21,NAND_ADQ13,Trace_D1,EMAC2_TXD3,SDMMC_DATA7,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL
D40	SHAREDIO_1V8	GPIO1_IO12	2L	G20	GPIO1_IO12,NAND_ALE,EMAC2_TX_CLK,SDMMC_DATA0,I2C1_SDA

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Table 12: MitySOM-A10S J4(E) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
E1	POWER	+5VIN	-	-	If already providing +12VIN, do not connect
E2	POWER	GND	-	-	
E3	LVDSIO_1V8	B2A_LVDS_B11_N	2A	AF16	LVDS2A_11n
E4	LVDSIO_1V8	B2A_LVDS_B11_P	2A	AG16	LVDS2A_11p
E5	POWER	GND	-	-	
E6	LVDSIO_1V8	B2A_LVDS_B8_N	2A	AF18	LVDS2A_8n
E7	LVDSIO_1V8	B2A_LVDS_B8_P	2A	AF17	LVDS2A_8p
E8	POWER	GND	-	-	
E9	LVDSIO_1V8	B2A_LVDS_B19_N	2A	AA11	LVDS2A_19N
E10	LVDSIO_1V8	B2A_LVDS_B19_P	2A	AB11	nPERSTL0/LVDS2A_19p
E11	POWER	GND	-	-	
E12	LVDSIO_1V8	B2A_LVDS_B4_N	2A	AD12	LVDS2A_4n
E13	LVDSIO_1V8	B2A_LVDS_B4_P	2A	AE12	LVDS2A_4p
E14	POWER	GND	-	-	
E15	LVDSIO_1V8	B3A_LVDS_B13_N	3A	AC3	LVDS3A_13n/CLK_3A_0n
E16	LVDSIO_1V8	B3A_LVDS_B13_P	3A	AD3	LVDS3A_13p/CLK_3A_0p
E17	POWER	GND	-	-	
E18	LVDSIO_1V8	B3A_LVDS_19_N	3A	AH3	LVDS3A_19n
E19	LVDSIO_1V8	B3A_LVDS_B19_P	3A	AH2	LVDS3A_19p
E20	POWER	GND	-	-	
E21	LVDSIO_1V8	B3A_LVDS_B15_N	3A	AC2	PLL_3A_CLKOUT0n/LVDS3A_15n
E22	LVDSIO_1V8	B3A_LVDS_B15_P	3A	AC1	PLL_3A_CLKOUT0p/LVDS3A_15p
E23	POWER	GND	-	-	
E24	LVDSIO_1V8	B3A_LVDS_B4_N	3A	Y5	LVDS3A_4n
E25	LVDSIO_1V8	B3A_LVDS_B4_P	3A	W5	LVDS3A_4p
E26	POWER	GND	-	-	
E27	LVDSIO_1V8	B3A_LVDS_B3_N	3A	Y6	LVDS3A_3n
E28	LVDSIO_1V8	B3A_LVDS_B3_P	3A	Y7	LVDS3A_3p
E29	POWER	GND	-	-	
E30	LVDSIO_1V8	B3B_LVDS_B21_P	3B	V7	LVDS3B_21n
E31	LVDSIO_1V8	B3B_LVDS_B21_N	3B	U6	LVDS3B_21p
E32	POWER	GND	-	-	
E33	LVDSIO_1V8	B3B_LVDS_B2_P	3B	T8	LVDS3B_2p
E34	LVDSIO_1V8	B3B_LVDS_B2_N	3B	T9	LVDS3B_2n
E35	POWER	GND	-	-	
E36	FFIO	HPS_RST_N	HPS	K11	HPS_nPOR
E37	SHAREDIO_1V8	GPIO1_IO23	2K	H16	
E38	SHAREDIO_1V8	GPIO0_IO10	2L	D10	GPIO0_IO10,NAND_ADQ6,USB0_DATA6,SPIM1_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
E39	SHAREDIO_1V8	GPIO0_IO0	2L	C18	GPIO0_IO0,NAND_ADQ0,UART0_CTS_N,USB0_CLK,SDMMC_DATA0,SPIM0_SS1_N,SPIS0_CLK
E40	HPSIO_1V8	UART0_TX	HPS	K15	1.8 V

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Table 13: MitySOM-A10S J4(F) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
F1	POWER	+5VIN	-	-	
F2	FFIO	POK	-	-	Indicates SOM local power supplies are properly sequenced on and operation. 5V signal is OK, 0 V signal indicates SOM is not powered up or has failed sequencing. FPGA IO should not be driven / asserted while POK is low.
F3	POWER	GND	-	-	
F4	POWER	GND	-	-	
F5	LVDSIO_1V8	B2A_LVDS_B21_P	2A	AC15	LVDS2A_21p
F6	LVDSIO_1V8	B2A_LVDS_B21_N	2A	AB15	LVDS2A_21n
F7	POWER	GND	-	-	
F8	LVDSIO_1V8	B2A_LVDS_B22_P	2A	AC13	LVDS2A_22p
F9	LVDSIO_1V8	B2A_LVDS_B22_N	2A	AB13	LVDS2A_22n
F10	POWER	GND	-	-	
F11	LVDSIO_1V8	B2A_LVDS_B20_N	2A	AA14	LVDS2A_20n
F12	LVDSIO_1V8	B2A_LVDS_B20_P	2A	AB14	LVDS2A_20p
F13	POWER	GND	-	-	
F14	LVDSIO_1V8	B2A_LVDS_B23_P	2A	AA12	DEV_OE/LVDS2A_23p
F15	LVDSIO_1V8	B2A_LVDS_B23_N	2A	AA13	INIT_DONE/LVDS2A_23n
F16	POWER	GND	-	-	
F17	LVDSIO_1V8	B3A_LVDS_B18_P	3A	AG3	LVDS3A_18p
F18	LVDSIO_1V8	B3A_LVDS_B18_N	3A	AF3	LVDS3A_18n
F19	POWER	GND	-	-	
F20	SHAREDIO_1V8	RGMII1_RX_CLK	2L	F21	RZQ_2L,GPIO1_IO2,NAND_WE_N,UART0_TX,EMAC1_RX_CLK,SPIM1_MISO,I2C0_SDA
F21	SHAREDIO_1V8	RGMII1_RX_CTL	2L	G21	GPIO1_IO3,NAND_RE_N,UART0_RX,EMAC1_RX_CTL,SPIM1_SS0_N,I2C0_SCL
F22	POWER	GND	-	-	
F23	SHAREDIO_1V8	RGMII1_RXD0	2L	E22	GPIO1_IO6,NAND_ADQ3,UART1_TX,EMAC1_RXD0,SPIS1_SS0_N,I2C1_SDA
F24	SHAREDIO_1V8	RGMII1_TXD1	2L	C22	PLL_2L_CLKOUT1n,GPIO1_IO5,NAND_ADQ2,UART1_RTS_N,EMAC1_TXD1,SPIS1_MOSI
F25	POWER	GND	-	-	
F26	LVDSIO_1V8	B3B_LVDS_B16_N	3B	T3	LVDS3B_16n
F27	LVDSIO_1V8	B3B_LVDS_B16_P	3B	T2	LVDS3B_16p
F28	POWER	GND	-	-	
F29	LVDSIO_1V8	B3B_LVDS_B6_N	3B	V8	LVDS3B_6n
F30	LVDSIO_1V8	B3B_LVDS_B6_P	3B	U8	LVDS3B_6p
F31	POWER	GND	-	-	
F32	LVDSIO_1V8	B3B_LVDS_B19_P	3B	U3	LVDS3B_19p
F33	LVDSIO_1V8	B3B_LVDS_B19_N	3B	U4	LVDS3B_19n
F34	POWER	GND	-	-	
F35	LVDSIO_1V8	B3B_LVDS_B9_P	3B	N2	LVDS3B_9p
F36	LVDSIO_1V8	B3B_LVDS_B9_N	3B	N3	LVDS3B_9n
F37	POWER	GND	-	-	
F38	FFIO_1V8	I2C1_SCL	2L	C16	
F39	FFIO_1V8	I2C1_SDA	2L	C17	
F40	HPSIO_1V8	UART0_RX	HPS	F13	1.8 V

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Table 14: MitySOM-A10S J4(G) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
G1	POWER	+5VIN	-	-	
G2	POWER	GND	-	-	
G3	POWER	GND	-	-	
G4	LVDSIO_1V8	B2A_LVDS_B3_P	2A	AE16	LVDS2A_3p
G5	LVDSIO_1V8	B2A_LVDS_B3_N	2A	AD15	LVDS2A_3n
G6	POWER	GND	-	-	
G7	LVDSIO_1V8	B2A_LVDS_B15_N	2A	AC17	LVDS2A_15n/PLL_2A_CLKOUT0n
G8	LVDSIO_1V8	B2A_LVDS_B15_P	2A	AC16	LVDS2A_15p/PLL_2A_CLKOUT0p
G9	POWER	GND	-	-	
G10	LVDSIO_1V8	B2A_LVDS_B9_N	2A	AF14	LVDS2A_9n
G11	LVDSIO_1V8	B2A_LVDS_B9_P	2A	AF13	LVDS2A_9p
G12	POWER	GND	-	-	
G13	LVDSIO_1V8	B2A_LVDS_B24_P	2A	AC12	DEV_CLRn/LVDS2A_24p
G14	LVDSIO_1V8	B2A_LVDS_B24_N	2A	AC11	CRC_ERROR/LVDS2A_24n
G15	POWER	GND	-	-	
G16	LVDSIO_1V8	B3A_LVDS_B23_P	3A	AG4	LVDS3A_23p
G17	LVDSIO_1V8	B3A_LVDS_B23_N	3A	AF4	LVDS3A_23n
G18	POWER	GND	-	-	
G19	LVDSIO_1V8	B3A_LVDS_B14_N	3A	AF2	LVDS3A_14n
G20	LVDSIO_1V8	B3A_LVDS_B14_P	3A	AE1	LVDS3A_14p
G21	POWER	GND	-	-	
G22	SHAREDIO_1V8	RGMII1_RXD1	2L	F22	GPIO1_IO7,NAND_CLE,UART1_RX,EMAC1_RXD1,SPIS1_MISO,I2C1_SCL
G23	SHAREDIO_1V8	RGMII1_TXD3	2L	E23	GPIO1_IO9,NAND_ADQ5,EMAC1_TXD3,SPIS0_MOSI,EMAC2_MDC,I2C_EMAC2_SCL
G24	POWER	GND	-	-	
G25	SHAREDIO_1V8	RGMII1_TX_CLK	2L	F23	CLK_2L_1p,GPIO1_IO0,NAND_ADQ0,UART0_CTS_N,EMAC1_TX_CLK,SPIM1_CLK
G26	SHAREDIO_1V8	RGMII1_TX_CTL	2L	G23	CLK_2L_1n,GPIO1_IO1,NAND_ADQ1,UART0_RTS_N,EMAC1_TX_CTL,SPIM1_MOSI
G27	POWER	GND	-	-	
G28	LVDSIO_1V8	B3B_LVDS_B1_N	3B	P4	LVDS3B_1n
G29	LVDSIO_1V8	B3B_LVDS_B1_P	3B	P3	LVDS3B_1p
G30	POWER	GND	-	-	
G31	LVDSIO_1V8	B3B_LVDS_B20_P	3B	V1	LVDS3B_20p
G32	LVDSIO_1V8	B3B_LVDS_B20_N	3B	U1	LVDS3B_20N
G33	POWER	GND	-	-	
G34	LVDSIO_1V8	B3B_LVDS_B15_P	3B	R2	LVDS3B_15p/PLL_3B_ClkOUT0p
G35	LVDSIO_1V8	B3B_LVDS_B15_N	3B	P2	LVDS3B_15n/PLL_3B_ClkOUT0n
G36	POWER	GND	-	-	
G37	FFIO	USB1_ID	-	-	
G38	POWER	+3VBAT	-	-	
G39	FFIO	USB1_VBUS	-	-	
G40	POWER	GND	-	-	

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Table 15: MitySOM-A10S J4(H) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux
H1	POWER	+5VIN	-	-	
H2	POWER	GND	-	-	
H3	LVDSIO_1V8	B2A_LVDS_B16_N	2A	AC18	LVDS2A_16n
H4	LVDSIO_1V8	B2A_LVDS_B16_P	2A	AD18	LVDS2A_16p
H5	POWER	GND	-	-	
H6	LVDSIO_1V8	B2A_LVDS_B17_P	2A	AE17	LVDS2A_17p
H7	LVDSIO_1V8	B2A_LVDS_B17_N	2A	AD17	LVDS2A_17n
H8	POWER	GND	-	-	
H9	LVDSIO_1V8	CLK2A_N	2A	AG15	LVDS2A_12n/CLK_2A_1n
H10	LVDSIO_1V8	CLK2A_P	2A	AG14	LVDS2A_12n/CLK_2A_1p
H11	POWER	GND	-	-	
H12	LVDSIO_1V8	B3A_LVDS_B9_P	3A	AB6	LVDS3A_9p
H13	LVDSIO_1V8	B3A_LVDS_B9_N	3A	AB5	LVDS3A_9n
H14	POWER	GND	-	-	
H15	LVDSIO_1V8	B3A_LVDS_B11_N	3A	AA4	LVDS3A_11n
H16	LVDSIO_1V8	B3A_LVDS_B11_P	3A	AA3	LVDS3A_11p/RZQ_3A
H17	POWER	GND	-	-	
H18	HPSIO_1V8	RGMII1_MDIO	HPS	H15	GPIO2_IO9,NAND_CE_N,UART1_RTS_N,SDMMC_DATA5,SPIM0_MISO,EMAC1_MDC,I2C_EMAC1_SCL
H19	HPSIO_1V8	RGMII1_MDC	HPS	F16	GPIO2_IO8,NAND_RB,UART1_TX,SDMMC_DATA4,SPIM0_MOSI,EMAC1_MDIO,I2C_EMAC1_SDA
H20	POWER	GND	-	-	
H21	SHAREDIO_1V8	RGMII1_RXD3	2L	E21	GPIO1_IO11,NAND_ADQ7,EMAC1_RXD3,SPIS0_MISO,EMAC0_MDC,I2C_EMAC0_SCL
H22	SHAREDIO_1V8	RGMII1_RXD2	2L	D22	GPIO1_IO10,NAND_ADQ6,EMAC1_RXD2,SPIS0_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
H23	POWER	GND	-	-	
H24	SHAREDIO_1V8	RGMII1_TXD2	2L	D23	GPIO1_IO8,NAND_ADQ4,EMAC1_TXD2,SPIS0_CLK,EMAC2_MDIO,I2C_EMAC2_SDA
H25	SHAREDIO_1V8	RGMII1_TXD0	2L	C23	PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1,GPIO1_IO4,NAND_WP_N,UART1_CTS_N,EMAC1_TXD0,SPIM1_SS1_N,SPIS1_CLK
H26	POWER	GND	-	-	
H27	LVDSIO_1V8	B3B_LVDS_B18_P	3B	T1	LVDS3B_18p
H28	LVDSIO_1V8	B3B_LVDS_B18_N	3B	R1	LVDS3B_18n
H29	POWER	GND	-	-	
H30	LVDSIO_1V8	B3B_LVDS_B13_P	3B	N1	LVDS3B_13p/CLK_3B_0p
H31	LVDSIO_1V8	B3B_LVDS_B13_N	3B	M1	LVDS3B_13n/CLK_3B_0n
H32	POWER	GND	-	-	
H33	LVDSIO_1V8	B3B_LVDS_B14_P	3B	H1	LVDS3B_14p
H34	LVDSIO_1V8	B3B_LVDS_B14_N	3B	G1	LVDS3B_14n
H35	POWER	GND	-	-	
H36	LVDSIO_1V8	B3B_LVDS_B4_N	3B	R4	LVDS3B_4p
H37	LVDSIO_1V8	B3B_LVDS_B4_P	3B	R5	LVDS3B_4n
H38	POWER	GND	-	-	
H39	FFIO	USB1_D_N	-	-	
H40	FFIO	USB1_D_P	-	-	

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J-600 Interface Description

The connector for the J600, is a 144 Pin Hirose FX10A-144P-SV1(71), which mates with Hirose FX10A-144S-SV (the mating height may be taller if desired but must match total height of J4). The interface consists of the following classes of signals:

Table 16 contains a summary of the MitySOM-A10S Transceiver Expansion Interface mapping.

Table 16: MitySOM-A10S J600 Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin
1	POWER	GND	-	-
2	POWER	GND	-	-
3	POWER	GND	-	-
4	XCVR_REFCLK	GXBR_REFCLK_IN_N	1D	N23
5	POWER	GND	-	-
6	XCVR_REFCLK	GXBR_REFCLK_IN_P	1D	N24
7	POWER	GND	-	-
8	POWER	GND	-	-
9	POWER	GND	-	-
10	POWER	GND	-	-
11	POWER	GND	-	-
12	CLKOUT	PLL_REFCLK_OUT_N	-	-
13	POWER	GND	-	-
14	CLKOUT	PLL_REFCLK_OUT_P	-	-
15	POWER	GND	-	-
16	POWER	GND	-	-
17	POWER	GND	-	-
18	POWER	GND	-	-
19	POWER	GND	-	-
20	XCVR_RX	GXBR_RX_7_P	1D	D26
21	POWER	GND	-	-
22	XCVR_RX	GXBR_RX_7_N	1D	D25
23	POWER	GND	-	-
24	POWER	GND	-	-
25	POWER	GND	-	-
26	POWER	GND	-	-
27	POWER	GND	-	-
28	XCVR_TX	GXBR_TX_7_P	1D	E28
29	POWER	GND	-	-
30	XCVR_TX	GXBR_TX_7_N	1D	E27
31	POWER	GND	-	-

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin
32	POWER	GND	-	-
33	POWER	GND	-	-
34	POWER	GND	-	-
35	POWER	GND	-	-
36	XCVR_RX	GXBR_RX_6_P	1D	F26
37	POWER	GND	-	-
38	XCVR_RX	GXBR_RX_6_N	1D	F25
39	POWER	GND	-	-
40	POWER	GND	-	-
41	POWER	GND	-	-
42	POWER	GND	-	-
43	POWER	GND	-	-
44	XCVR_TX	GXBR_TX_6_P	1D	G28
45	POWER	GND	-	-
46	XCVR_TX	GXBR_TX_6_N	1D	G27
47	POWER	GND	-	-
48	POWER	GND	-	-
49	POWER	GND	-	-
50	POWER	GND	-	-
51	POWER	GND	-	-
52	XCVR_RX	GXBR_RX_5_P	1D	H26
53	POWER	GND	-	-
54	XCVR_RX	GXBR_RX_5_N	1D	H25
55	POWER	GND	-	-
56	POWER	GND	-	-
57	POWER	GND	-	-
58	POWER	GND	-	-
59	POWER	GND	-	-
60	XCVR_TX	GXBR_TX_5_P	1D	J28
61	POWER	GND	-	-
62	XCVR_TX	GXBR_TX_5_N	1D	J27
63	POWER	GND	-	-
64	POWER	GND	-	-
65	POWER	GND	-	-
66	POWER	GND	-	-
67	POWER	GND	-	-
68	XCVR_RX	GXBR_RX_4_P	1D	K26
69	POWER	GND	-	-

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin
70	XCVR_RX	GXBR_RX_4_N	1D	K25
71	POWER	GND	-	-
72	POWER	GND	-	-
73	POWER	GND	-	-
74	POWER	GND	-	-
75	POWER	GND	-	-
76	XCVR_TX	GXBR_TX_4_P	1D	L28
77	POWER	GND	-	-
78	XCVR_TX	GXBR_TX_4_N	1D	L27
79	POWER	GND	-	-
80	POWER	GND	-	-
81	POWER	GND	-	-
82	POWER	GND	-	-
83	POWER	GND	-	-
84	XCVR_RX	GXBR_RX_3_P	1D	M26
85	POWER	GND	-	-
86	XCVR_RX	GXBR_RX_3_N	1D	M25
87	POWER	GND	-	-
88	POWER	GND	-	-
89	POWER	GND	-	-
90	POWER	GND	-	-
91	POWER	GND	-	-
92	XCVR_TX	GXBR_TX_3_P	1D	N28
93	POWER	GND	-	-
94	XCVR_TX	GXBR_TX_3_N	1D	N27
95	POWER	GND	-	-
96	POWER	GND	-	-
97	POWER	GND	-	-
98	POWER	GND	-	-
99	POWER	GND	-	-
100	XCVR_RX	GXBR_RX_2_P	1D	P26
101	POWER	GND	-	-
102	XCVR_RX	GXBR_RX_2_N	1D	P25
103	POWER	GND	-	-
104	POWER	GND	-	-
105	POWER	GND	-	-
106	POWER	GND	-	-
107	POWER	GND	-	-

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin
108	XCVR_TX	GXBR_TX_2_P	1D	R28
109	POWER	GND	-	-
110	XCVR_TX	GXBR_TX_2_N	1D	R27
111	POWER	GND	-	-
112	POWER	GND	-	-
113	POWER	GND	-	-
114	POWER	GND	-	-
115	POWER	GND	-	-
116	XCVR_RX	GXBR_RX_1_P	1C	T26
117	POWER	GND	-	-
118	XCVR_RX	GXBR_RX_1_N	1C	T25
119	POWER	GND	-	-
120	POWER	GND	-	-
121	POWER	GND	-	-
122	POWER	GND	-	-
123	POWER	GND	-	-
124	XCVR_TX	GXBR_TX_1_P	1C	U28
125	POWER	GND	-	-
126	XCVR_TX	GXBR_TX_1_N	1C	U27
127	POWER	GND	-	-
128	POWER	GND	-	-
129	POWER	GND	-	-
130	POWER	GND	-	-
131	POWER	GND	-	-
132	XCVR_RX	GXBR_RX_0_P	1C	V26
133	POWER	GND	-	-
134	XCVR_RX	GXBR_RX_0_N	1C	V25
135	POWER	GND	-	-
136	POWER	GND	-	-
137	POWER	GND	-	-
138	POWER	GND	-	-
139	POWER	GND	-	-
140	XCVR_TX	GXBR_TX_0_P	1C	W28
141	POWER	GND	-	-
142	XCVR_TX	GXBR_TX_0_N	1C	W27
143	POWER	GND	-	-
144	POWER	GND	-	-

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ELECTRICAL CHARACTERISTICS

Table 17: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
+5VIN	Voltage Supply, +5V input			5.0		Volts
$I_{5.0}$	Quiescent Current draw	5.0 volt input, 1033 MHz DDR4, no FPGA fabric, Linux prompt				mA
$I_{5.0\text{-}max}$	Max current draw	5.0 volt input		TBS	TBS	mA
+12VIN	Voltage supply, optional +12 volt input		10.2	12.0	13.2	Volts
$I_{12.0}$	Quiescent Current draw	12.0 volt input, 1033 MHz DDR4, no FPGA fabric, Linux prompt				mA
$I_{12.0\text{-}max}$	Max current draw	12.0 volt input		TBS	TBS	mA
	1. Power utilization of the MitySOM-A10S is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR4 RAM utilization. 2. +12V input voltage is an optional feature not available on all SOMs, please contact info@criticallink.com for additional details 3. +12V and +5V input voltages must not be supplied to the module at the same time.					

ORDERING INFORMATION

The following table lists the standard module configurations. For availability, price, and minimum order quantity of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

Table 18: Standard Model Numbers

Model / Part Number	FPGA KLE	CPU Speed Grade	HPS RAM (32-bit)	FPGA RAM (16-bit)	Component Temperature Ratings
A10S-P8-X5E-RC-SA	270	1.2GHz	4GB	2GB	0ºC to 70º C
A10S-P8-X5E-RI-SA	270	1.2GHz	4GB	2GB	-40ºC to 85º C
A10S-P9-X5E-RC-SA	480	1.2GHz	4GB	2GB	0ºC to 70º C
A10S-P9-X5E-RI-SA	480	1.2GHz	4GB	2GB	-40ºC to 85º C
A10S-P7-XXD-RC-SA	160	1.2GHz	2GB	N/A	0ºC to 70º C

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MECHANICAL INTERFACE

A top view mechanical outline of the MitySOM-A10S is illustrated in Figure 2, below. All dimensions are in mils (0.001"). The connector positions for the board to board interfaces are shown, but the connectors are actually installed on the bottom side of the board. The locations of the pads shown are as viewed from the top and through the board.

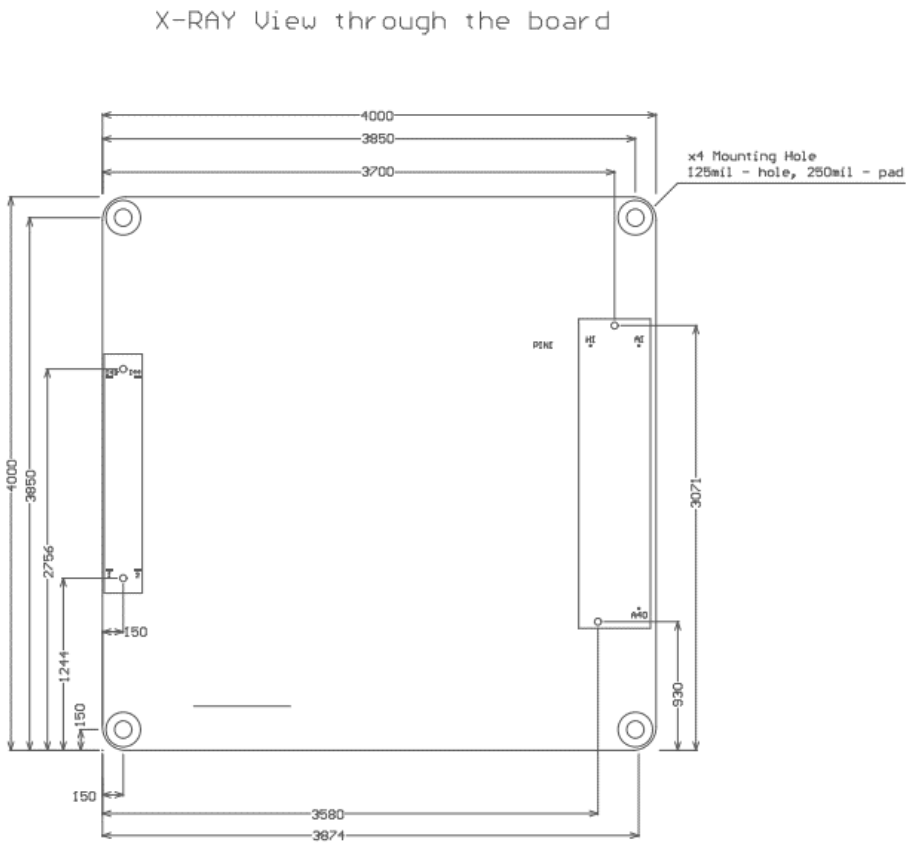

Figure 2 MitySOM-A10S Mechanical Outline, View From Top

REVISION HISTORY

Revision	Date	Change Description
A	February 15, 2018	Preliminary Release for early adopters
B	May 18, 2018	Updates to preliminary specifications
C	August 17, 2018	Revision to Table 18: Standard Model Numbers
D	August 20, 2018	Added further clarification for boot media selection, input power options, and cleaned up formatting
E	September 10, 2018	Corrected Table 10 pins C26, C27. Added CPU Speed Grade column to Table 18.

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FOOTNOTES

[1] http://www.altera.com/support/devices/estimator/pow-powerplay.jsp

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