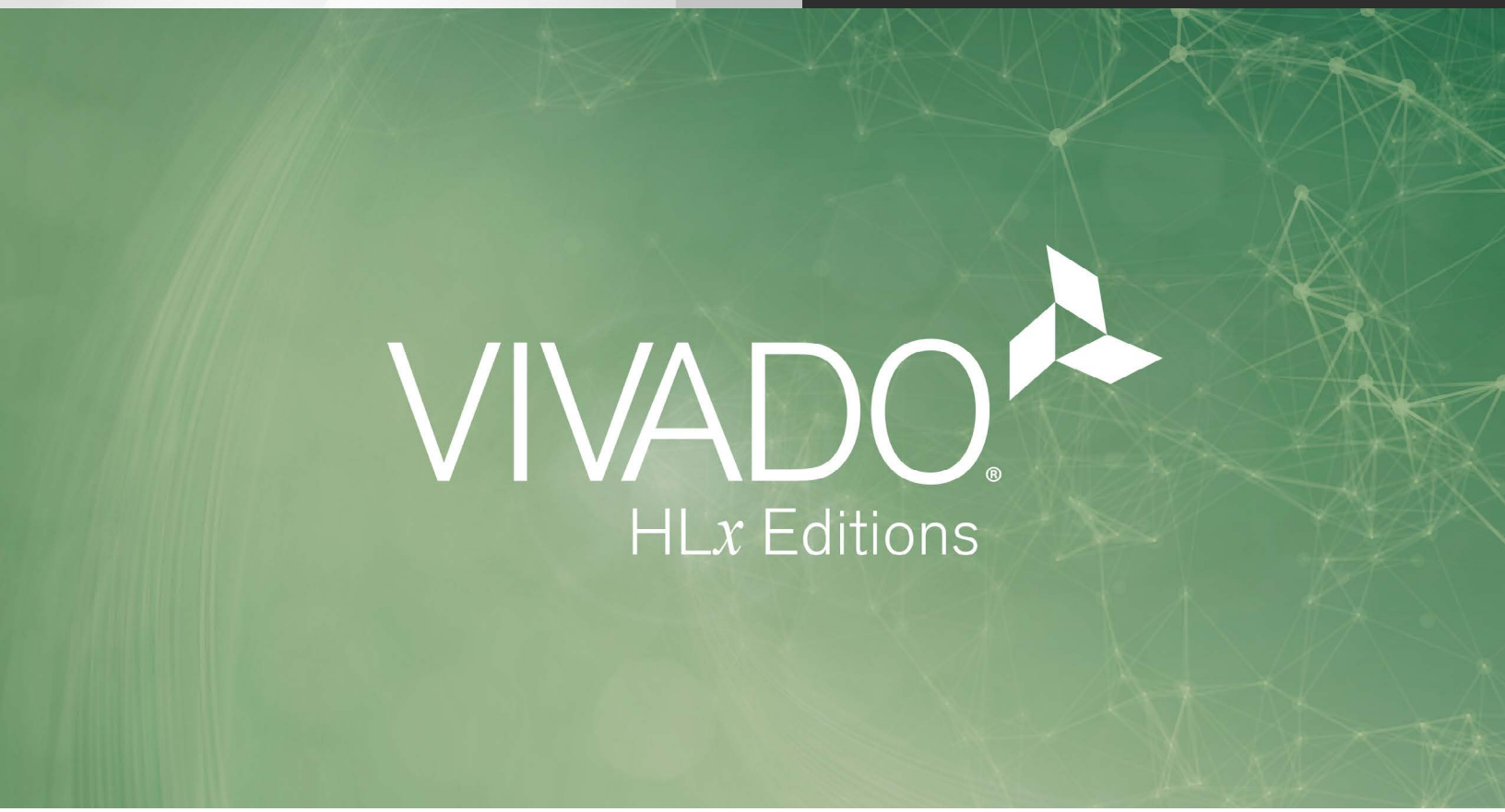
Vivado Design Suite HLx Editions



Bringing Ultra High Productivity to Mainstream Systems & Platform Designers

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Vivado Design Suite HLx Editions

15X PRODUCTIVITY GAINS WITH:

- C/C++ based design and accelerated reuse
- Domain focused libraries
- IP Subsystems
- Integration automation
- Accelerated design closure
- Enables rapid platform creation and deployment
- For Zynq SoCs and new MPSoCs, along with ASIC-class FPGAs and 3D ICs

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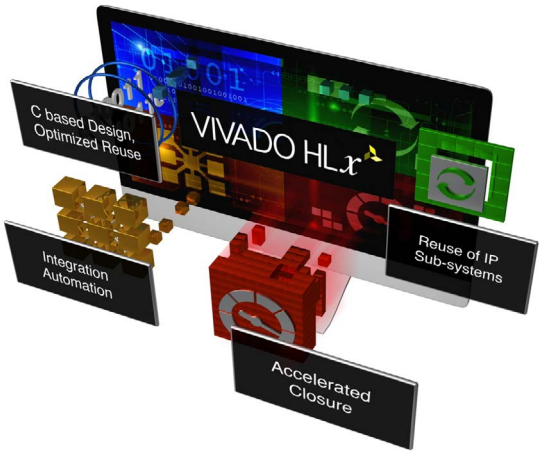
Vivado Design Suite HLx Editions

A new approach for ultra high productivity for creating and broadly deploying system platforms



The Vivado® Design Suite offers a new approach for ultra-high productivity with next generation C/C++ and IP-based design. The new HLx editions include HL System Edition, HL Design Edition and HL WebPACK™ Edition. When coupled with the new UltraFast™ High-Level Productivity Design Methodology Guide, users can realize a 10-15X productivity gain over traditional approaches.

Unlike traditional RTL-based design where the majority of the design effort is spent in the backend of the design process, C and IP-based design allows for reduced development cycles in verification, implementation and design convergence, so designers can focus on their differentiated logic. This flow includes:

- Rapid generation of the platform connectivity design, along with the necessary software stack
- Rapid differentiated logic development using high-level design. This also enables superior design reuse capabilities.
- Dramatically shortened verification times from high-level languages, compared to RTL.

Using high levels of abstraction, design teams can quickly get overall better or equal Quality of Results (performance, power, utilization).

UltraFast High-Level Productivity Design Methodology Guide

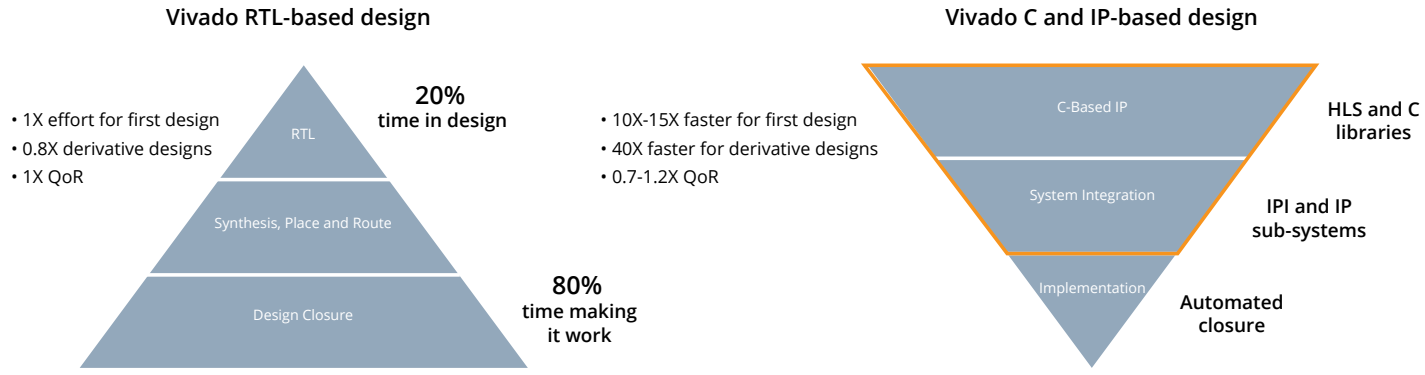
Traditional design development starts with experienced system architects estimating how their design will be implemented in a new technology, capturing both the system connectivity requirements and the value added differentiated logic in high-level modeling format. In turn, RTL designs implement those requirements. RTL design cycles typically consist verification and design closure iterations for each block, as well as for the entire design. As a consequence of this methodology, the platform connectivity design never stabilizes, as any change in the differentiated logic can cause an IO interface (e.g. DDR memory, Ethernet, PCIe...) to fail timing requirements. Also, RTL verification cycles no longer allow for exhaustive functional tests prior to hardware bring-up.

The High-Level Design Methodology turns the development effort on its head allowing designers to spend more time designing the value-add logic, and less time trying to make it work. This flow provides a 15X reduction in design cycle compared to an RTL design flow. The main attributes of this high-level methodology are:

- Separation of platform development and differentiated logic, allowing designers to focus on the company's high-value functionality.
- Rapid configuration, generation and closure of the platform connectivity, using Vivado IP Integrator with board awareness, as well as the Vivado IP systems.
- C-based simulation for the differentiated logic, decreasing simulation times by orders of magnitude over traditional RTL simulation.
- High-Level synthesis with Vivado HLS and C/C++ libraries, and well as IP Integrator for rapid implementation and system integration from C to silicon.

All steps in the UltraFast High-Level Productivity Design Methodology Guide can be performed interactively or using command line scripts. The result of all manual interactions may be saved to scripts, allowing the entire flow, from the design simulation through to programming the FPGA, to be fully automated. This highly automated flow makes it possible to generate an FPGA bitstream, and test the design on the board, often before any RTL design simulation has completed.

Even greater productivity improvements come when design derivatives are created. Targeting a different device, clock speed, or configuration of the design is as easy as editing a C parameter or a Vivado HLS option. The tools will then automatically chose a new microarchitecture that meets the requirement for the new product.



HLx speeds the creation, design modification and reuse and complements Xilinx's SDx family of software-defined environments by providing a methodology for designing custom-platforms that are software programmable.

C-based Design and Accelerated Reuse

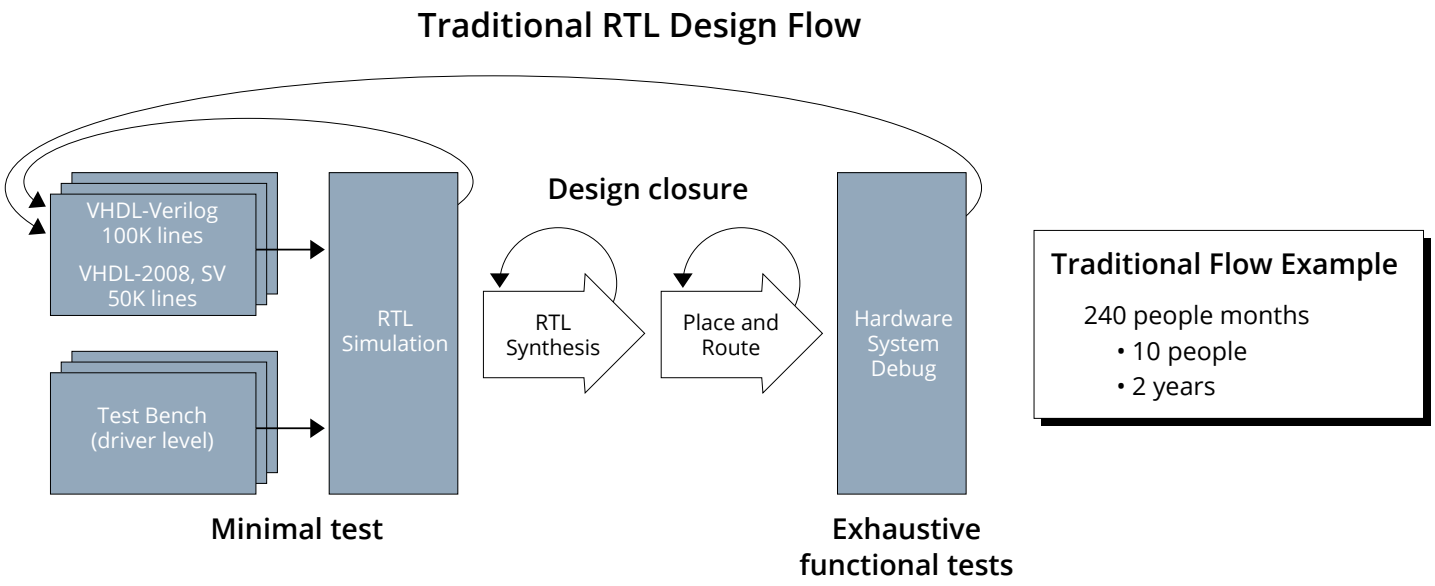
A typical system starts with a software model of the system. Whether for entertainment, gaming, communications, or medicine, most product began as a software model or prototype. This model is then distributed to the hardware and embedded software teams. Hardware design teams are tasked to choose an RTL microarchitecture that meets the system requirement.

The biggest advantage of programmable devices such as FPGAs is the ability to create custom-hardware which is optimized for any specific application. As a result, the end product has orders of magnitude better performance per watt than a pure software program running on a distributed processor-based system.

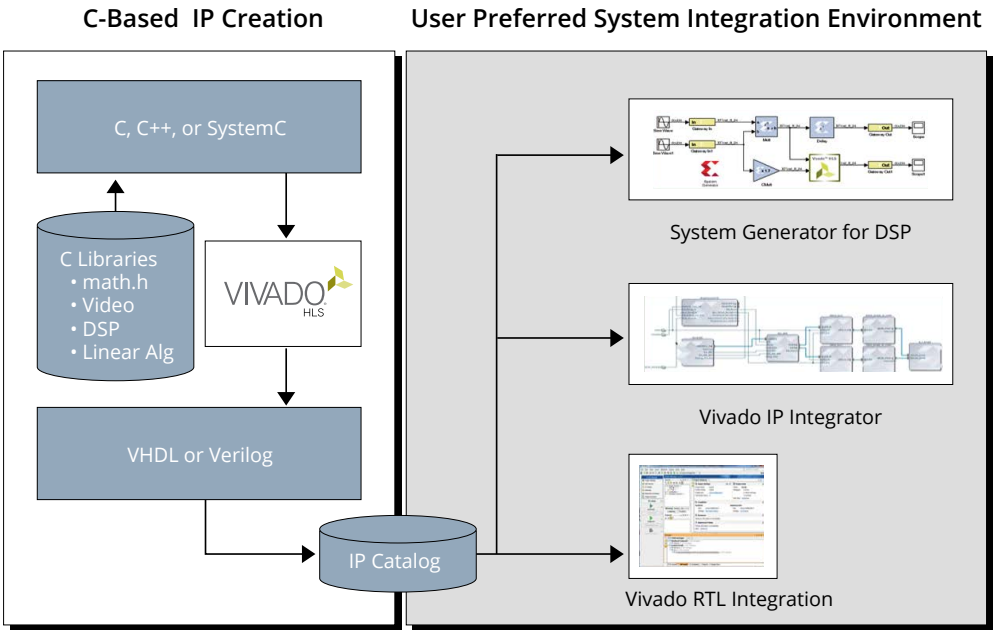
The Vivado High-Level Synthesis (HLS) compiler provides a programming environment similar to those available for processor compilers. The main difference is that Vivado HLS compiles the C code into an optimized RTL microarchitecture, while processor-based compilers generate assembly code to be executed on a fixed, GHz rate, processor architecture.

System architects, software programmers or hardware engineers can use Vivado HLS to create custom hardware optimized for throughout, power and latency. This allows for optimized implementation of high performance, low power, or low cost systems, for any application including compute, storage, or networking.

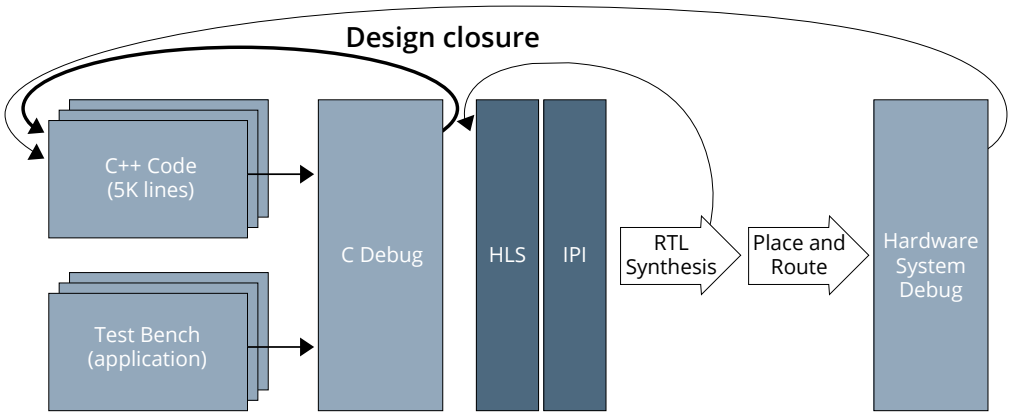
Vivado HLS accelerates design implementation and verification by enabling C/C++ specifications to be directly synthesized into VHDL or Verilog RTL, after exploring a multitude of micro-architectures based on design requirements. Functional simulation can be performed at that level, providing orders of magnitude acceleration over VHDL or Verilog simulation. For example, with a video motion estimation algorithm, the C input to Vivado HLS execute10 frames of video data in 10 seconds, while the corresponding RTL model takes roughly two days to process the same 10 video frames.



When coupled with Vivado IP Integrator, Vivado HLS provides designers and system architects with a faster and more robust way of delivering quality designs.



Vivado HLx Design Flow



15X Faster

HLS-Based Flow Example

16 people months
- 2 people
- 8 months

Faster for derivative designs
- C++ reuse
- Scales with parameters
- Device independent

Vivado HLS provides a faster path to IP creation by:

- Abstraction of algorithmic description, data type specification (integer, fixed-point or floating-point) and interfaces (FIFO, AXI4, AXI4-Lite, AXI4-Stream)
- Directives driven architecture-aware synthesis to quickly deliver a design that can rival or beat hand-coded RTL implementations in term of performance, power and area utilization.
- Accelerated verification using C/C++ test bench simulation, automatic VHDL or Verilog simulation and test bench generation
- Multi-language support (C, C++, OpenCL, SystemC) and the broadest language coverage in the industry
- Automatic use of Xilinx on-chip memory hierarchy, Digital Signal Processing compute elements and floating-point library

Domain Focused Software Libraries

Supported libraries include Math, DSP, Video, and linear algebra libraries for high performance low power implementations. In addition for complex cores such as FFTs and filters HLS integrates the optimized LogiCORE™ IP FFT and FIR Compiler for the highest quality of results. For domain-specific acceleration, Xilinx Alliance members also provide libraries for OpenCV, BLAS, Machine learning and more. For more information see http://www.xilinx.com/HLS

Reuse of Complete IP Sub-systems

Xilinx and its Alliance Partners have a rich library of Intellectual Property (IP), to help get products to market faster. The IP goes through a vigorous test and validation effort to insure success the first time. Beyond a simple library of cores we provide solutions to increase productivity.

Xilinx's new LogiCORE IP sub-systems are highly configurable, market-tailored building blocks that integrate multiple individual IP cores, including data -movers, software drivers, examples designs and test benches. Available with the Vivado Design Suite are new IP subsystems for Ethernet, PCIe, HDMI, video processing, image sensor processing and OTN development. As an example, the AXI-4 PCIe subsystem leverages multiple IP cores including PCIe, DMA, AXI-4 interconnect and provides the necessary software stack to be used in a processor system.

All IP sub-systems are based on industry standards: AMBA® AXI™4 interconnect protocol, IEEE P1735 encryption and XDC design constraints, enabling interoperability with user and Xilinx Alliance member packaged IP, in order to accelerate integration.

Integration Automation

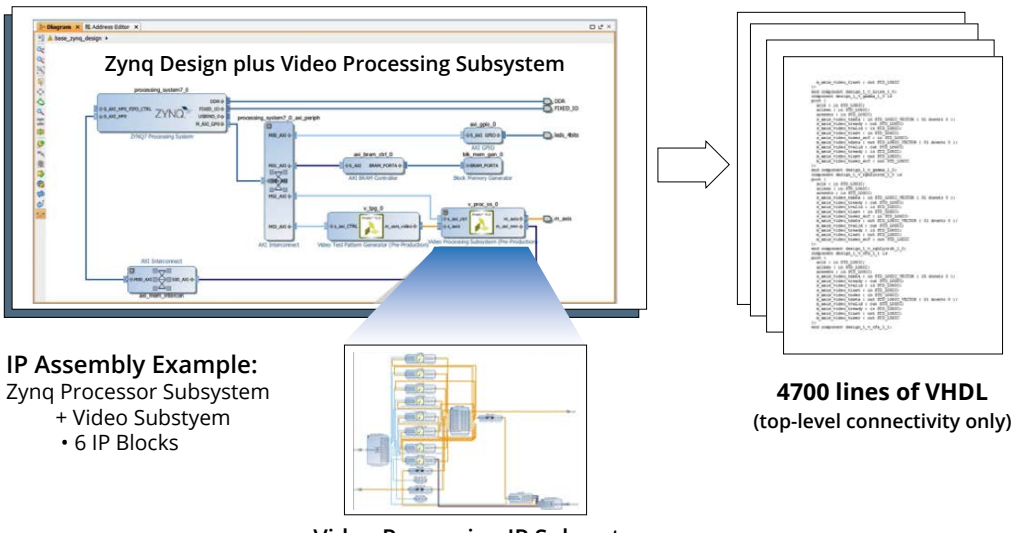
The Vivado Design Suite shatters the RTL design productivity plateau with Vivado IP Integrator, the industry's first plug-and-play system integration design environment.

Vivado IP Integrator enables rapid platform creation by generating customized connectivity to the board interfaces. It also enables system assembly of highly concurrent C/C++ generated functions, onto a platform.

Vivado IP Integrator provides a graphical and Tcl-based, correct-by-construction design development flow. It provides a device and platform aware, interactive environment that supports intelligent auto-connection of key interfaces, one-click subsystem generation, real-time DRCs, and interface change propagation, combined with a powerful debug capability.

Designers work at the "interface" and not "signal" level of abstraction when making connections between functions, greatly increasing productivity. Although IP Integrator leverages the industry standard AXI4, it also supports other interfaces and users can define their own custom interfaces for greater flexibility.

Integration Automation



With open, industry IP standards, Vivado Design Suite enables third-party vendors to deliver their IP portfolios to developers, who can now integrate them with Vivado IPI. Users can also package their own RTL, or C/C++/SystemC and MATLAB®/Simulink® algorithms into the IP catalog using Vivado HLS or System Generator for DSP with the Vivado IP packager.

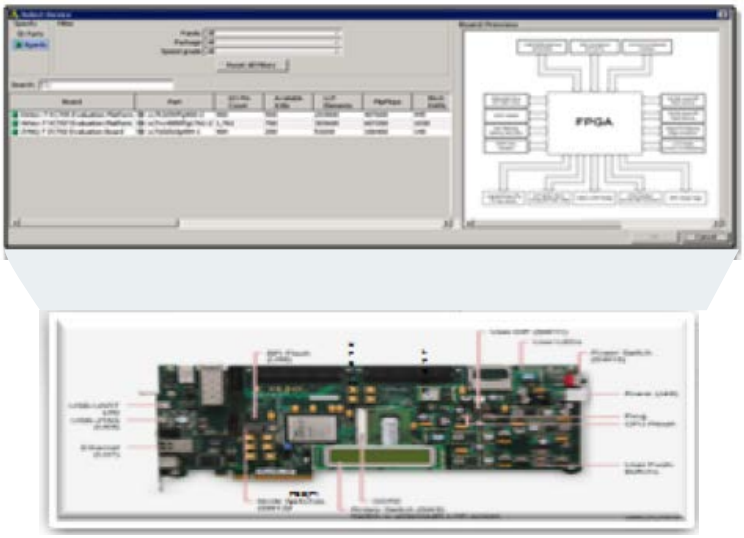
Accelerated Closure

The Vivado Design Suite accelerates the implementation process by delivering more turns per day while helping to reduce the number of design iterations needed. Its shared, scalable data model delivers unrivaled compiled times and memory footprint, and enables early analysis of critical design metrics such as power, timing and resource utilization. These metrics allow design and tool setting modifications to occur earlier in the design processes, where iterations are faster and impact on system performance higher.

Using the High-Level Design Methodology, iterations are pushed even higher, at the C/C++ level, for even faster and higher impact iterations, dwarfing the impact and the need of last minute place-and-route closure iterations.

Platform Creation and Reuse

The Vivado Design Suite is not only device aware—it is target platform aware— supporting Zynq® SoCs and MPSoCs, along with ASIC-class FPGAs and 3D ICs boards and kits. By being target platform aware, Vivado configures and applies board-specific design rule checks, which ensures rapid bring up of working systems.



Platform Aware

For example, by selecting the Zynq-7000 All Programmable SoC ZC702 Evaluation Kit, and instantiating a Zynq processing system within IPI, Vivado preconfigures the processing system with the correct peripherals, drivers, and memory map to support the board. Platform designers can now more rapidly identify, reuse, and integrate both software and hardware IP, targeting the dual-core ARM® processing system and high-performance FPGA logic.

The user easily specifies the interface between the processing system and their logic with a series of dialog boxes. Interfaces are automatically generated, optimized for performance or area, and then users can add their own algorithms with Vivado HLS or use the Vivado IP catalog to complete their design.

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Summary

Rapid development of complex smarter systems requires levels of automation that go beyond RTL-level design. Vivado Design Suite HLx Editions are uniquely positioned to do this.

The new Vivado HLx Editions offers a new approach for ultra-high productivity with next generation platform design automation, C/C++ programming of the differentiated logic, with graphical system assembly. This approach, described in the UltraFast High-Level Productivity Design Methodology Guide (UG1197), is proven to accelerate design creation and verification by 15x over RTL-based methodologies.

HLx also complements the Xilinx SDx Development Environments (SDSoC, SDAccel and SDNet) which are tailored for software and systems engineers. While the HLx methodology can automate platform design creation, the SDx family of development environments enable software-defined programming of such platform, using C, C++, OpenCL, or the emerging P4 language for packet processing.

HLx and SDx represent Xilinx's new era of software programmability solutions for developing smarter, connected and differentiated systems leveraging end-product-optimized custom hardware using All Programmable devices including Zynq SoCs, MPSoCs, ASIC-class FPGAs and 3D ICs.

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