Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit

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XPM 0402902-04

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/31/2012	1.0	Initial Xilinx release.
03/01/2013	1.1	Add Vivado® Design Suite to VC707 Evaluation Kit Contents. Removed references to USB flash drive throughout Chapter 1, Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit. Updated Step 1 and removed note in Extract the AMS Design Files, page 13.
09/25/2013	1.2	Updated disclaimer and copyright. Updated Introduction, VC707 Evaluation Kit Contents, Project Files, Extract the AMS Design Files, Set Up the Hardware, and Examine Analog Mixed Signal Features. Removed IBERT Demonstration, MultiBoot Design, MIG Design, Integrated Endpoint Block for PCI Express®, and LogiCORE™ IP Ethernet SGMII Designs sections. Added Appendix A, VC707 Board Components and Appendix B, Additional Resources.
03/07/2014	1.2.1	Made typographical edits.
05/03/2014	1.3	Updated Figure 1-1, Figure 1-7, and Figure 1-11 to show a Revision 1.0 board.
09/16/2014	1.4	Updated Verify Jumpers are in Default Positions, including removing the J7, J40, and J41 jumper connectors and adding Figure 1-6.
10/14/2015	1.4.1	Updated the XPM number to 0402902-04.

Table of Contents

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Chapter 1

Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit

Introduction

This document describes how to use the materials provided in the VC707 Evaluation Kit to set up the VC707 board and a host computer to run two reference designs, which test and demonstrate some of the key features of the XC7VX485T FPGA and the VC707 board:

- Built-in self test (BIST)
- Analog mixed signal (AMS) card demonstration

Note: These design summaries are for use as a quick start method for users who are familiar with Xilinx tools, technology, and reference designs. Additional instructions and background information are available from the VC707 Evaluation Kit website.

VC707 Evaluation Kit Contents

The VC707 Evaluation Kit includes:

- VC707 board with the Virtex®-7 XC7VX485T FPGA
- ISE® Design Suite: Logic Edition (full seat, node-locked, device-locked to the XC7VX485T FPGA)
- Vivado® Design Suite Installation DVD
- Printed entitlement voucher: provides entitlement of the Vivado Design Suite Logic Edition, node-locked, and device-locked to the XC7VX485T FPGA. Follow the printed instructions on the voucher to redeem your software entitlement.
- AMS101 evaluation card
- USB cable, standard-A plug to mini-B plug
- USB cable, standard-A plug to micro-B plug
- HDMI™ cable, type-A plug to type-A plug
- Power Supply: 100 VAC–240 VAC input, 12 VDC 5.0A output
- Power cords to support three main plug types
- Getting Started Guide

Host Computer Requirements

The example designs described in this document require an Intel processor based computer running Windows 7 or Windows XP operating system. The computer must have two USB ports and an Ethernet interface.

Note: The Windows 7 operating system is used in the setup instructions and examples.

Preliminary Setup

Complete the tasks in this section before running the reference designs.

Install ISE Software

Install the latest version of the Xilinx ISE® Design Suite on the host computer.

Install the USB UART Drivers

Download and install the Silicon Laboratories CP210x VCP drivers on the host computer. The drivers are available for download at no cost from Silicon Labs.

Configure the Host Computer COM Port

The BIST design uses a terminal program to communicate between the host computer and the VC707 board. To configure the host computer COM port for this purpose:

1. Connect the VC707 board to the host computer and power supply as shown in Figure 1-1.

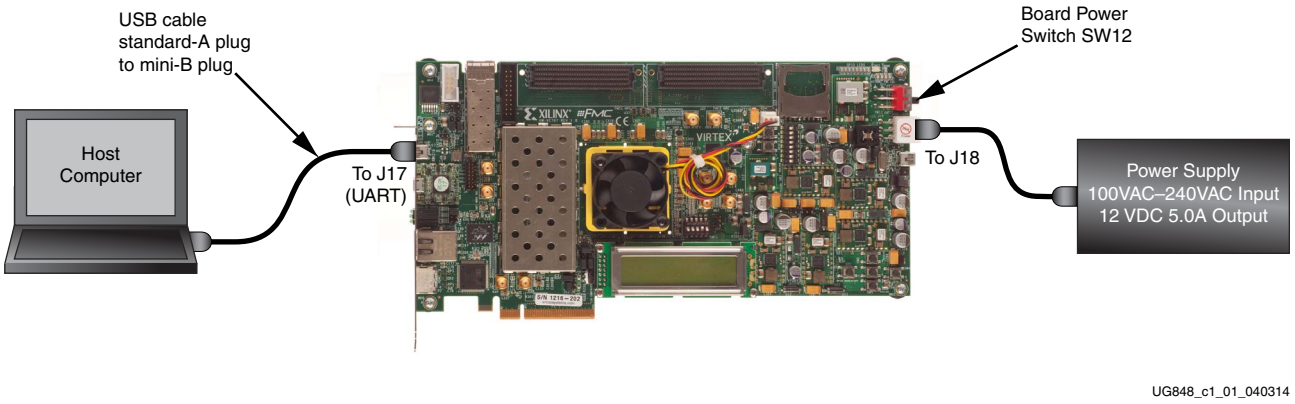

Figure 1-1: **Host Computer COM Port Configuration**

2. Turn Board power on (SW12).

3. Open the host computer Device Manager (Figure 1-2). In the Windows task bar, Click **Start**, click **Control Panel**, and then click **Device Manager**.

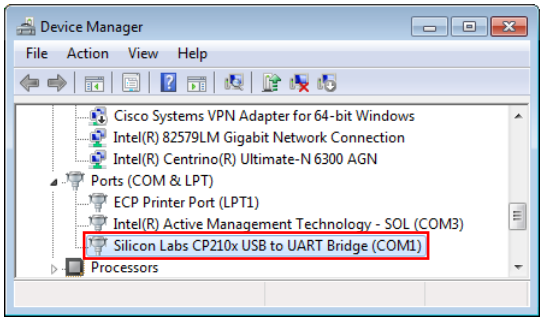

Figure 1-2: **Device Manager**

4. Open UART properties. Expand **Ports (COM & LPT)**, right-click **Silicon Labs CP210x USB to UART Bridge**, and then click **Properties**.
5. In the properties window, select the **Port Settings** tab, verify the settings match the values shown in Figure 1-3 and then click **Advanced**.

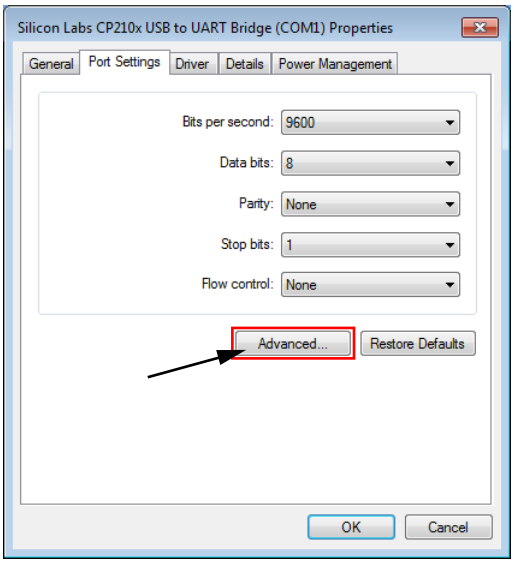

Figure 1-3: **Port Settings**

6. Select an unused COM Port Number and then click **OK**. Figure 1-4 shows **COM1** as the selected COM port number.

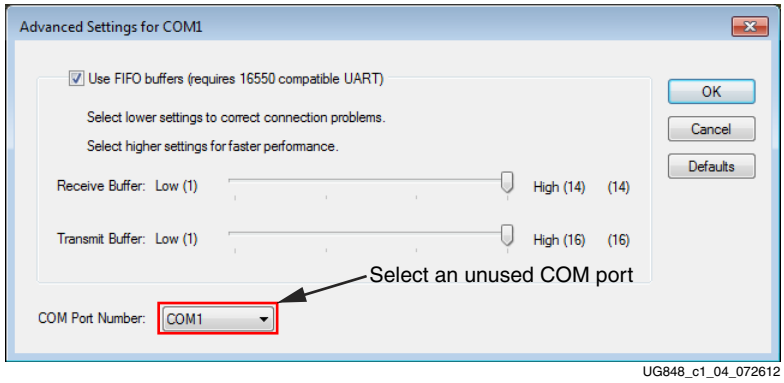

Figure 1-4: **Advanced Settings**

7. Click **OK** in the properties window (Figure 1-3, page 7), and then close the Device Manager and the Control Panel.

Install the Terminal Program

Download and install the Tera Term Pro terminal program on the host computer. Tera Term is available for download at no cost from the LogMeTT download page.

To communicate with the VC707 board, configure the New Connection and Serial Port settings as shown in Figure 1-5. These settings must match the host computer COM port settings shown in Figure 1-3, page 7 and Figure 1-4.

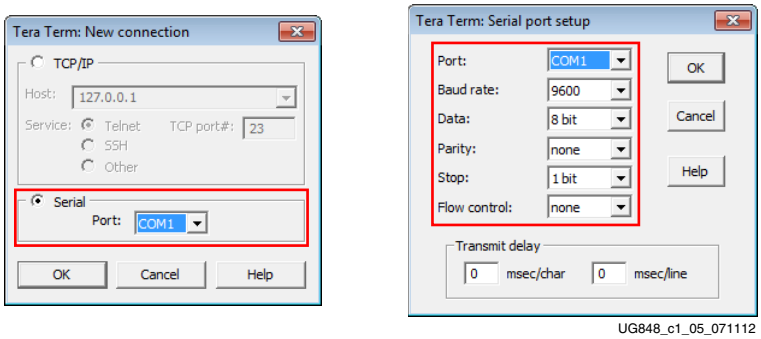

Figure 1-5: **TeraTerm Pro Settings**

Preliminary setup is complete and the reference designs can now be run.

Verify Jumpers are in Default Positions

Verify the jumpers on the VC707 board are positioned as shown in Table 1-1. See Figure 1-6 for the location of the jumpers.

Table 1-1: **Default Jumper Settings**

Callout	Jumper	Function	Default Jumper Position	Schematic 0381418 Page Number
1	J6	SFP Enable	None	31
2	J9	XADC GND ferrite filter bypass jumper	None	40
3	J10	XADC GND-to-XADC_AGND jumper	1–2	40
4	J11	TI Controller U42 Addr 52 Reset jumper	None	46
5	J12	TI Controller U43 Addr 53 Reset jumper	None	50
6	J13	USB Mini-B Connector J2 VBUS	None	44
7	J14	USB SMBC U8 CLKOUT selector	None	44
8	J38	SFP RX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1–2	31
9	J39	SFP TX Rate: 1-2 = Full BW Rate, 2-3 = Low BW Rate	1–2	31
10	J42	XADC external 1.2V or internal VREFP selector	1–2	40
11	J43	XADC VCC Select Header	2–3	40
12	J44	USB Mini-B Connector J2 GND jumper	None	44
13	J45	USB SMBC U8 VBUS	1–2	44
14	J49	PCIe Bus Width Select Header	1-2	30
15	J50	TI Controller U64 Addr 54 Reset jumper	None	53
16	J51	FMC_VADJ_ON_B jumper	1–2	46
17	J53	XADC VCC5V0-to-XADC_VCC5V0 jumper	1–2	40
18	J54	XADC REF3012 U35 V_{IN} Select	1–2	40

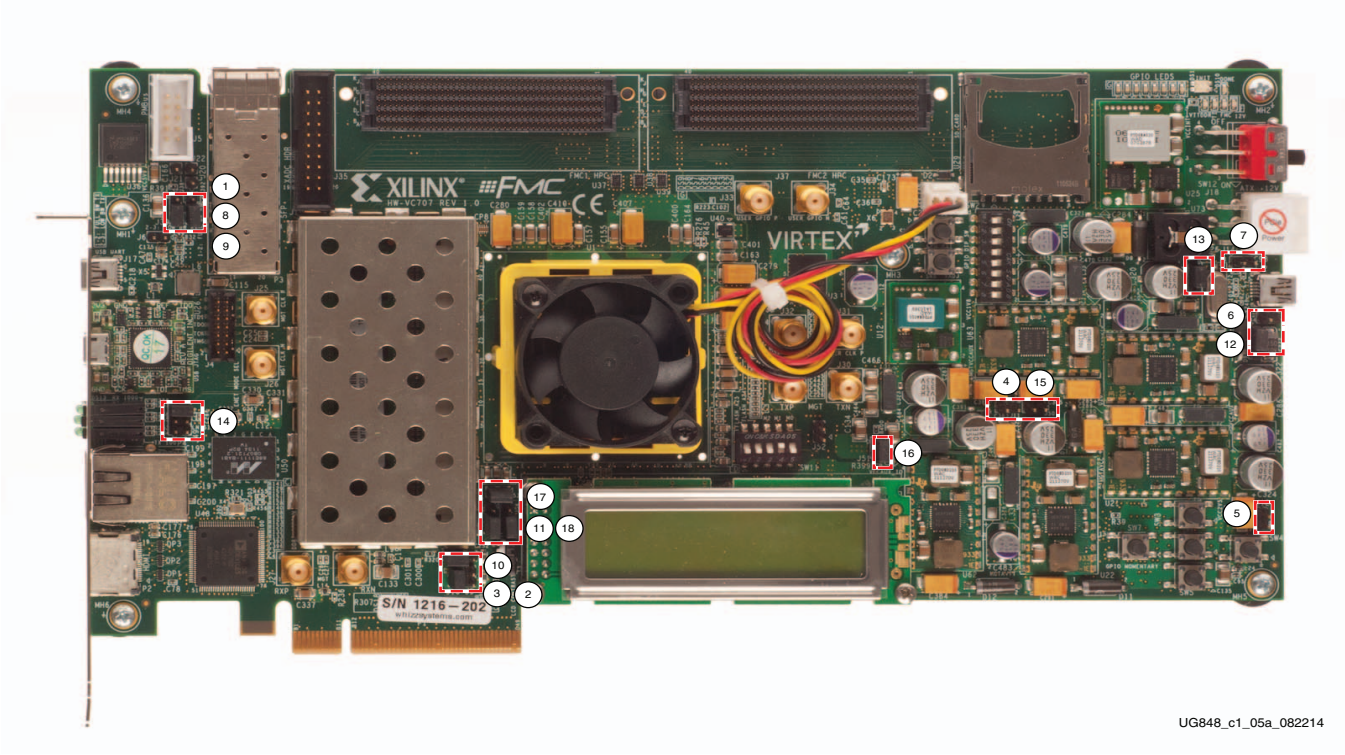

Figure 1-6: **VC707 Board Jumper Header Locations**

Built-In Self Test

The BIST tests several XC7VX485T FPGA and VC707 board features. The BIST interface is a menu of tests displayed by a terminal program running on the host computer.

Project Files

The BIST design is available for download from the VC707 Evaluation Kit website on the Docs & Designs tab.

The BIST is pre-loaded in the device and the project files are not required to run this demonstration.

Run BIST

1. Complete the tasks under Preliminary Setup, page 6.
2. Connect the VC707 board to the host computer and power supply as shown in Figure 1-7.

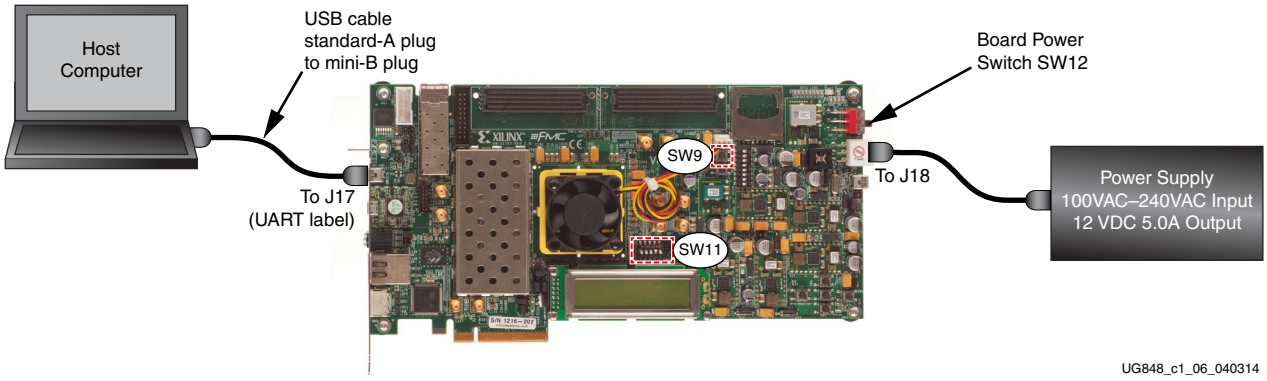

Figure 1-7: **BIST Board Connections**

3. Turn board power on (SW12).
4. Set DIP switch SW11 as shown in Figure 1-8.

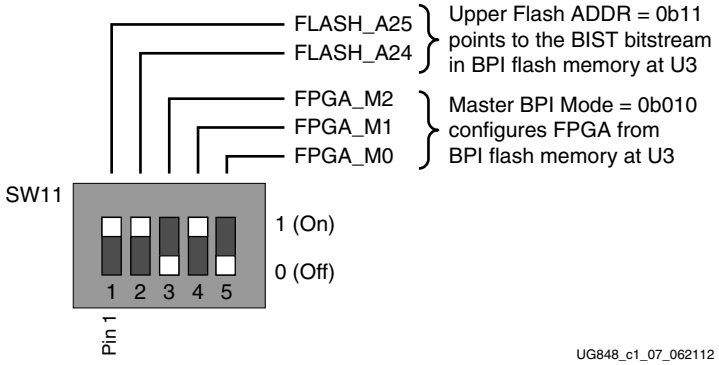

Figure 1-8: **SW11 BIST Settings**

5. Press and release the Program button SW9 (Figure 1-7). The BIST bitstream configures the FPGA and then runs BIST. The terminal program displays the BIST menu shown in Figure 1-9.

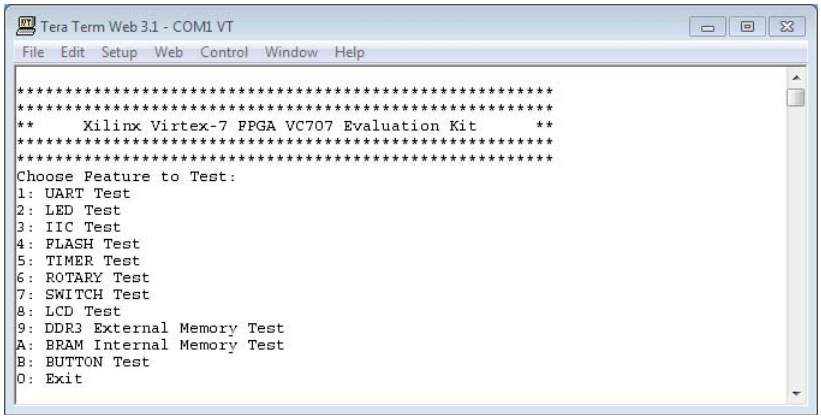

Figure 1-9: **BIST Menu**

6. To run a test, type the test number, and press the **Enter** key. Press any key to end the test and return to the menu.

AMS 101 Card Demonstration

The XC7VX485T FPGA features dual one Mega-sample per second (MS/s), 12-bit, analog-to-digital converters (XADC) built into the FPGA. The AMS card demonstration uses the AMS 101 card (Figure 1-11, page 14) to generate an analog signal and the AMS evaluator tool (Figure 1-13, page 15) to view and control the signal.

Install the AMS Evaluator Tool

Download the AMS Evaluator installer files:

1. Go to AMS101 Evaluation Card.
2. Click **AMS101 Evaluation Card Targeted Reference Designs**.
3. Download the 7 series FPGA and Zynq®-7000 AP SoC AMS Evaluator Installer for AMS Targeted Reference Design zip file.
4. Extract the AMS101 AMS Evaluator Installer Vxx to your hard drive.
5. Click the `setup.exe` file to install the National Instruments LabVIEW Engine needed to host the AMS Evaluator tool.

The GUI was developed with National Instruments LabVIEW 2011 software. To enable use of the GUI without a LabVIEW license, Xilinx bundled the LabVIEW run-time engine with the GUI installer. During the installation process, the run-time engine is installed on the PC.

Extract the AMS Design Files

1. Go to the VC707 Evaluation Kit website and navigate to the Docs & Designs tab.
2. Click **Virtex-7 FPGA VC707 Evaluation Kit**.
3. Navigate to the software version that you are using, click **+** to expand the document type list, and click **Targeted Reference Designs**.
4. Download the "AMS Targeted Reference Design for Virtex-7 FPGA VC707 Evaluation Kit" zip file.
5. After downloading the design files, open the `xadc_eval_design_vc707_vxx` folder and unzip the files to a working directory on the host computer.
6. Open the ChipScope™ Pro Analyzer in the ISE design tools.
7. Click **Open_cable**.
8. Select **Device**, choose **Configure**, and click **Select New File**.
9. Open the AMS design in the `xadc_eval_design_vc707_vxx` folder by opening the `ready_to_test` folder and selecting the `xadc_eval_design.bit` file.

Set Up the Hardware

1. Complete the tasks under Preliminary Setup, page 6.
2. On the AMS101 card (Figure 1-11), place jumpers across pins 1–2 on J3 and J5.

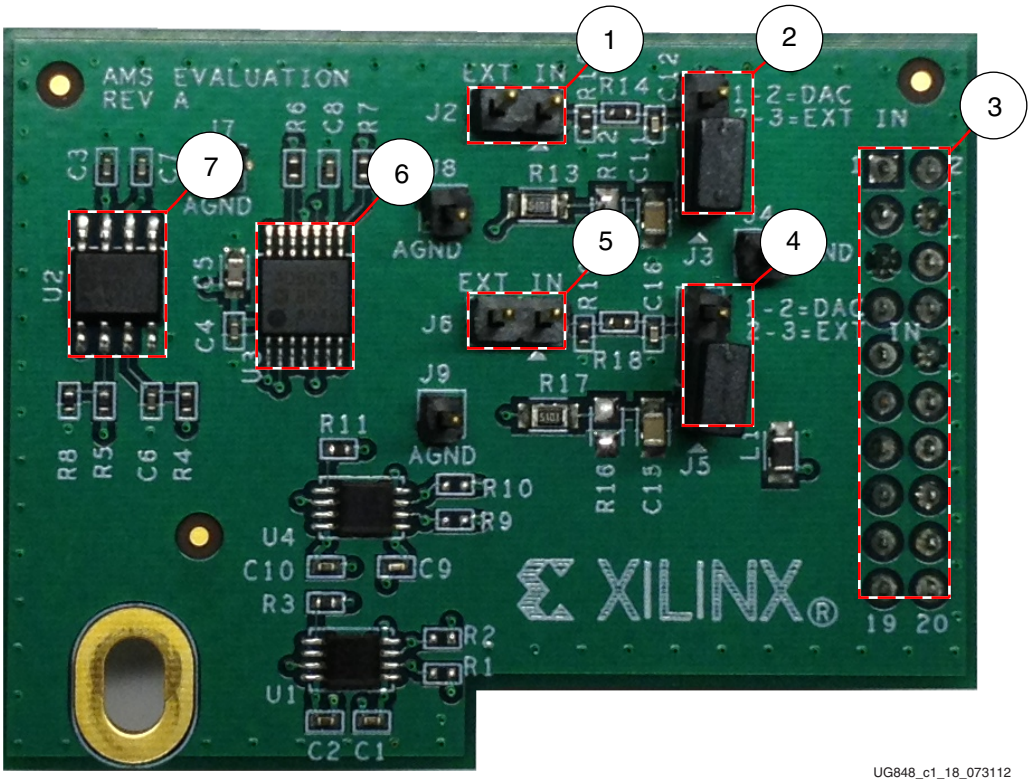

Figure 1-10: **AMS101 Evaluation Card**

Table 1-2: **AMS101 Evaluation Card Jumper and Component Notes**

Callout	Reference Designator	Notes
1	J2	External signal source input to V_P positive analog input.
2	J3	Jumper on pins 1–2 selects DAC signal source. Jumper on pins 2–3 selects external input source on J2.
3		20-pin connector to XADC header J35 on the VC707 board.
4	J5	Jumper on pins 1–2 selects DAC signal source. Jumper on pins 2–3 selects external input source on J6.
5	J6	External signal source to V_N negative analog input.
6	U3	16-bit DAC. Sets analog test voltage.
7	U2	Reference buffer for DAC.

3. Turn off the VC707 board power (SW12) before installing the AMS 101 card on the VC707 board XADC header J35.
4. Plug the AMS 101 Card into the XADC header J35 on the VC707 board as shown in Figure 1-11.
5. Connect the VC707 board to the host computer and power supply as shown in Figure 1-11.

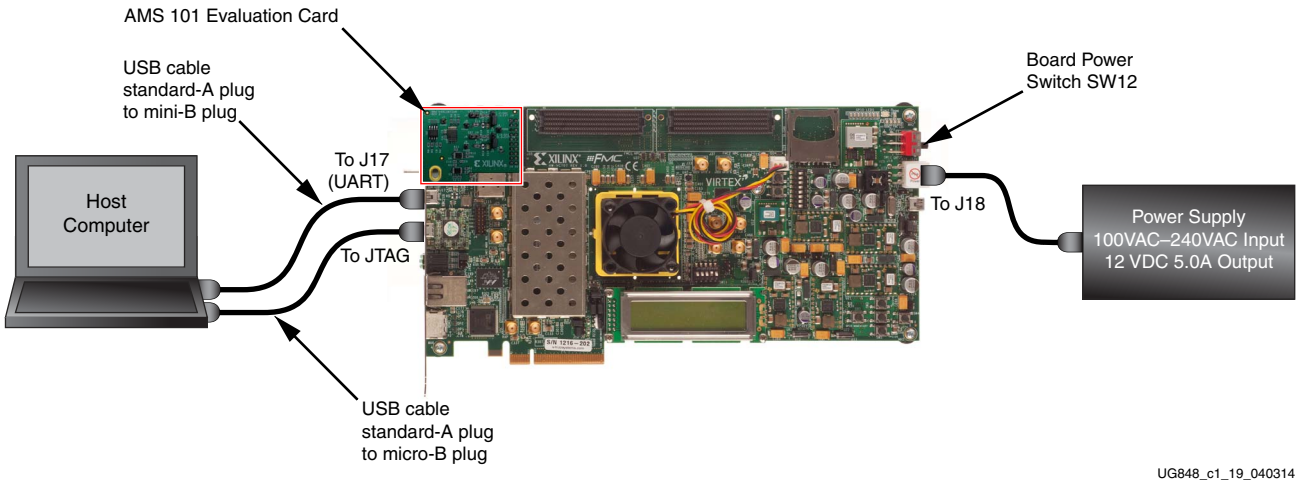

Figure 1-11: **BIST Board Connections**

6. Turn board power on (SW12).

Examine Analog Mixed Signal Features

The AMS evaluator tool (Figure 1-13) is useful for examining analog signals in the time and frequency domains, displaying linearity, viewing the XADC register settings, and monitoring the internal FPGA temperature sensor and supply voltages. The AMS evaluator tool also provides user-controllable decimation on the XADC output data to enhance the signal-to-noise ratio (SNR) performance.

After the AMS Evaluator installer files are installed, a red Xilinx logo ("X") is displayed on the host PC desktop. Click the "X" to open the AMS Evaluator tool (Figure 1-12).

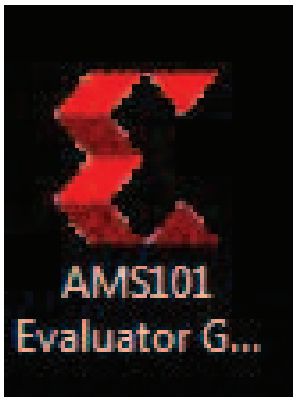

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Figure 1-12: **AMS Icon**

To run the AMS evaluator tool executable file:

1. Open the `AMS_Eval_Demo_Files_<ISE_Version>` directory and double-click `AMS101 Evaluator GUI V1.0.exe`. See Figure 1-13.

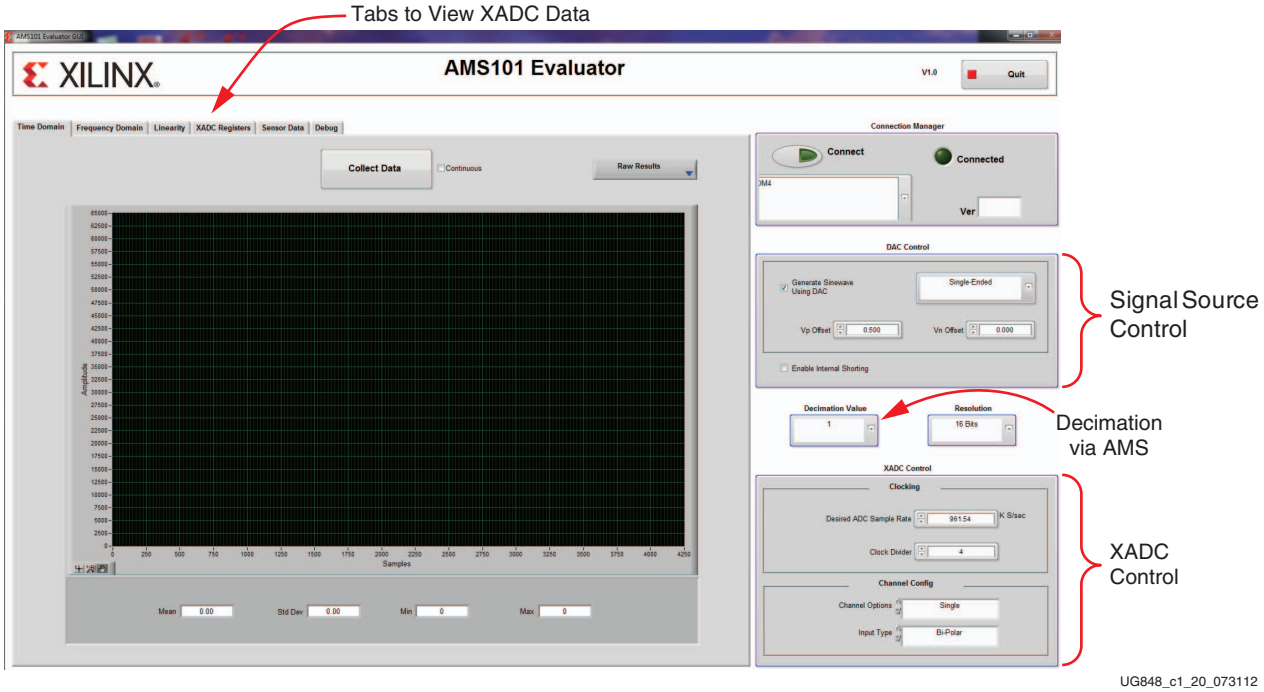

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Figure 1-13: **AMS101 Evaluator Tool**

For an extensive explanation of the AMS101 evaluation card see the *AMS101 Evaluation Card User Guide* (UG886) [Ref 1].

Next Steps

1. Download the *VC707 Evaluation Board for the Virtex-7 FPGA User Guide* (UG885) [Ref 2].
2. Review and run the reference designs available at the VC707 Evaluation Kit website from the Docs & Designs tab.

Additional Information

VC707 board reference design files, user guides, schematics, and bill of materials, can be downloaded from the VC707 Evaluation Kit website.

Other documents associated with Xilinx devices, design tools, intellectual property, boards, and kits are available at the Xilinx documentation website.

Instructions for restoring the BPI flash memory with the factory-loaded reference designs are provided in *VC707 Restoring Flash Contents* (XTP145) [Ref 3].

For an extensive explanation of the AMS101 evaluation card, see the *AMS101 Evaluation Card User Guide* (UG886) [Ref 1].

Appendix A

VC707 Board Components

The VC707 board block diagram is shown in Figure A-1. The VC707 board schematics are available for download from the VC707 Evaluation Kit product page on the Docs & Designs tab at the VC707 Evaluation Kit website.

Caution! The VC707 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

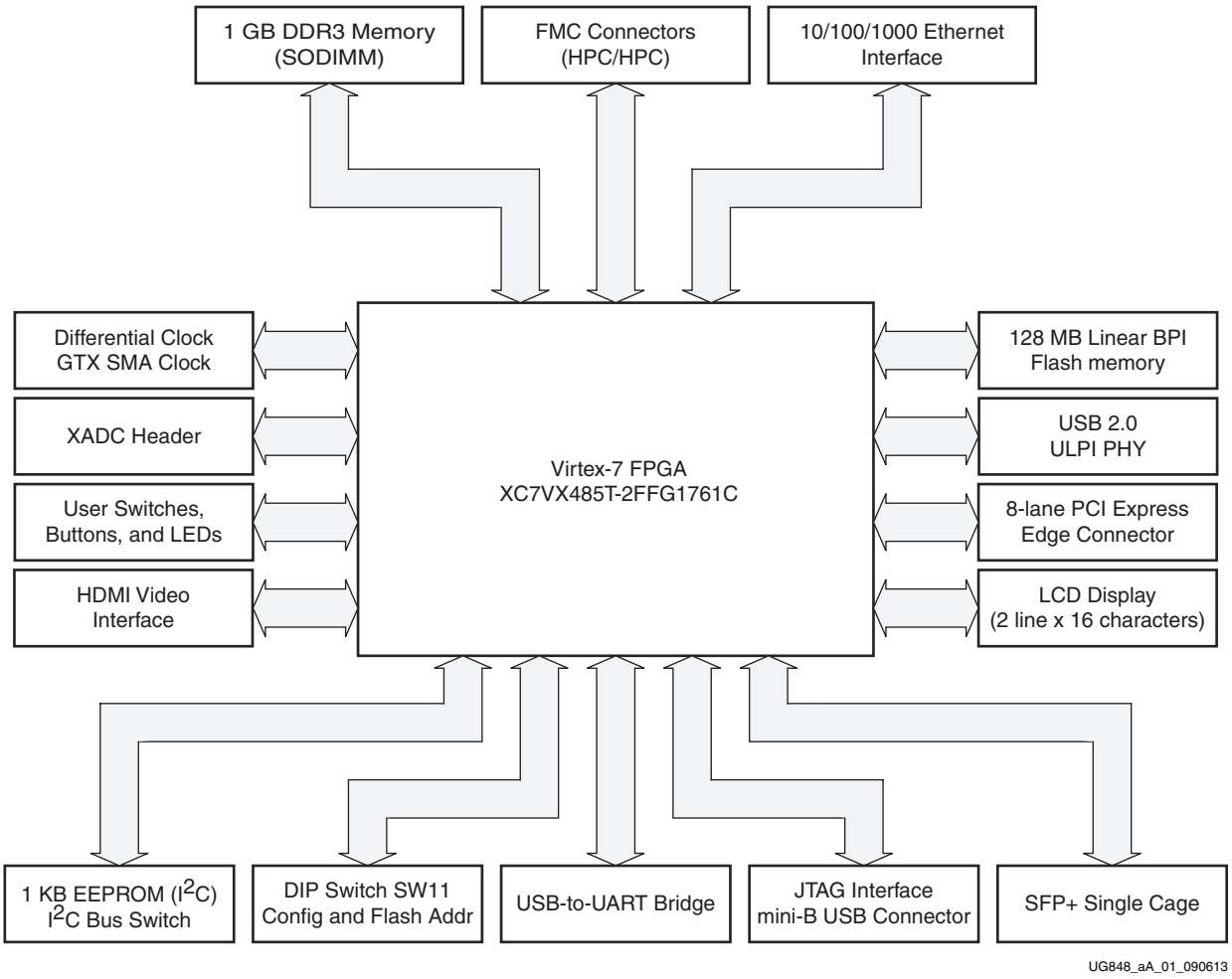

Figure A-1: **VC707 Board Block Diagram**

Feature Descriptions

Figure A-2 shows the VC707 board.

Note: The image in Figure A-2 is for reference only and might not reflect the current revision of the board.

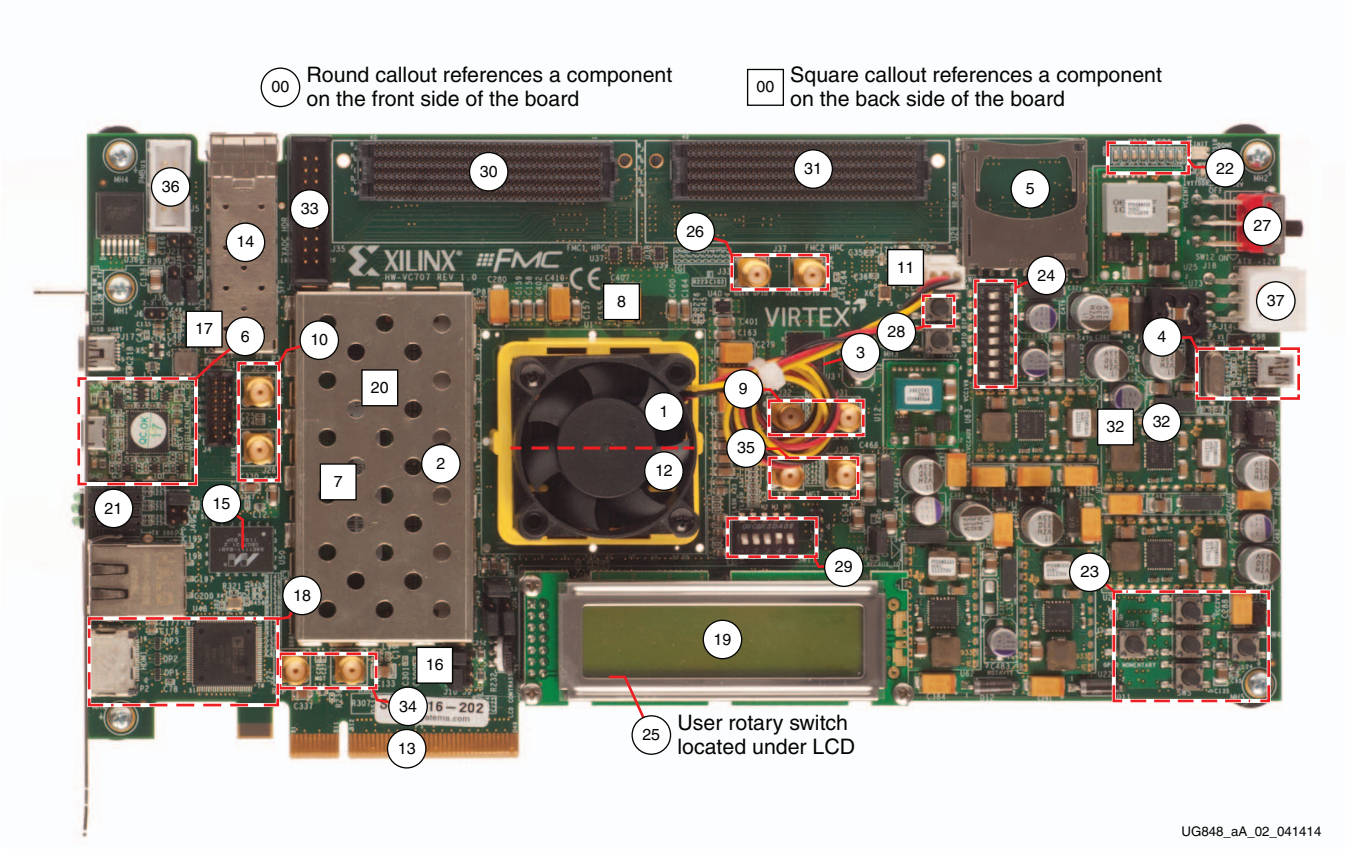

Figure A-2: **VC707 Board Component Locations**

Table A-1: **VC707 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
1	U1	Virtex-7 FPGA with cooling fan	XC7VX485T-2FFG1761C	
2	J1	DDR3 SODIMM memory (1 GB)	Micron MT8JTF12864HZ-1G6G1	21
3	U3	BPI parallel NOR flash memory (1 Gb)	Micron PC28F00AG18FE	35
4	U8, J2	USB ULPI transceiver, USB mini-B connector	SMSC USB3320-EZK	44
5	U29	SD card interface connector	Molex 67840-8001	37
6	U26	USB JTAG interface, USB micro-B connector	Digilent USB JTAG module	20
7	U51	System clock, 200 MHz, LVDS (back side of board)	SiTime SIT9102-243N25E200.0000	32
8	U34	I^2C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)	Silicon Labs SI570BAB0000544DG	32
9	J31, J32	User SMA clock	Rosenberger 32K10K-400L5	32
10	J25, J26	GTX transceiver SMA reference clock	Rosenberger 32K10K-400L5	32

Table A-1: **VC707 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
11	U24	Jitter attenuated clock (back side of board)	Silicon Labs SI5324C-C-GM	33
12		GTX transceiver Quad 111 – Quad 119	Embedded within FPGA U1	12 – 15
13	P1	PCI Express connector	8-lane card edge connector	30
14	P3	SFP/SFP+ module connector	Molex 74441-0010	31
15	U50	10/100/1000 Mb/s Ethernet PHY	Marvell M88E1111-BAB1C000	34
16	U2	SGMII GTX transceiver clock generator	ICS ICS84402IAGI-01LF	32
17	U44	USB-to-UART bridge	Silicon Labs CP2103GM	36
18	P2, U48	HDMI video connector, HDMI controller	Molex 500254-1927, AD ADV7511KSTZ-P	43, 42
19	J23	LCD character display and connector	2 x 7 0.1 inch male header	39
20	U52	I^2C Bus Switch (back side of board)	TI PCA9548ARGER	41
21	DS11–DS13	Ethernet status LEDs	EPHY status LED, dual green	34
22	DS2–DS9	User LEDs	GPIO LEDs, green 0603	38
23	SW3–SW7	User pushbuttons, active-High	E-Switch TL3301EP100QG	38
24	SW2	User DIP Switch	8-pole C and K SDA08H1SBD	38
25	SW10	User rotary switch (under LCD assembly)	Panasonic EVQ-WK4001	38
26	J33, J34	User SMA GPIO	Rosenberger 32K10K-400L5	32
27	SW12	Power on/off switch	C&K 1201M2S3AQE2	45
28	SW9	FPGA PROG pushbutton	E-Switch TL3301EP100QG	38
29	SW11	Config mode/upper linear flash address dip switch	5-pole C&K SDA05H1IBD	36
30	J35	FMC HPC1 connector (J35)	Samtec ASP_134486_01	22–25
31	J37	FMC HPC2 connector (J37)	Samtec ASP_134486_01	26–29
32		Power management system (front and back side of board)	TI UCD9248PFC in conjunction with various regulators	45–55
33	J19	Xilinx XADC header	2 x 10 0.1inch male header	40
34	J27, J28	GTX receiver SMA (RX)	Rosenberger 32K10K-400L5	32
35	J29/J30	GTX transmitter SMA (TX)	Rosenberger 32K10K-400L5	32
36	J5	2 x 5 shrouded PMBus connector	Assmann HW10G-0202	46
37	J18	12V power input 2 x 3 connector	Molex 39-30-1060	46

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Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC707 board and its documentation is available on these websites:

Virtex-7 VC707 Evaluation Kit

Virtex-7 VC707 Evaluation Kit documentation

Virtex-7 VC707 Evaluation Kit Master Answer Record (AR 45382)

These documents and sites provide supplemental material useful with this guide:

1. *AMS101 Evaluation Card User Guide* (UG886)
2. *VC707 Evaluation Board for the Virtex-7 FPGA User Guide* (UG885)
3. *VC707 Restoring Flash Contents* (XTP145)
4. Silicon Labs
5. LogMeTT
6. National Instruments LabVIEW 32-bit Run-Time Engine

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Appendix C

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
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