FPGA Broadcast Mezzanine Card

User Guide

UG753 (v1.1) January 14, 2013

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/08/10	1.0	Initial Xilinx release.
12/04/12	1.1	Updated data sheet references in Table 1. Added footnotes to Table 2. Moved resource information from the former Preface to Appendix A, Additional Resources, which now contains additional links to resources. Moved the Warranty to Appendix B, Warranty.

Table of Contents

XILINX®

FPGA Broadcast Mezzanine Card

Introduction

The FPGA broadcast mezzanine card (commonly called *FMC card*) plugs into the Virtex®-6 FPGA ML605 and Spartan®-6 FPGA SP605 evaluation boards (also referred to as carrier boards) to provide interfaces for professional broadcast audio and video equipment.

The basic features of the FMC card are:

- Compatibility with ML605 and SP605 carrier boards.
- Four input BNC connectors to support the triple-rate serial digital interface (SDI) which includes 3G-SDI, HD-SDI, and SD-SDI. (Only one GTP receiver is connected to the FMC card when connecting to the SP605 carrier board.)
- Four output BNC connectors to support triple-rate SDI. (Only one GTP transmitter is connected to the FMC card when connecting to the SP605 carrier board.)
- An external analog video sync BNC input connector and sync separator to provide horizontal and vertical sync signals to the carrier board. This allows the interfaces to be genlocked to an external video sync signal.
- Two AES3 RX BNC inputs and two AES3 TX BNC outputs to support up to four input and four output digital audio channels.
- AES10 input and output BNC connectors to support MADI.
- An expansion FMC connector allows expansion FMC mezzanine cards to be plugged onto the FMC card. This connector is for use primarily with an expansion card to add four more SDI input and output connectors. It is not compatible with all FMC mezzanine cards. At this time, an SDI expansion card for this connector is not available.
- Two sites for clock modules to provide flexible clocking resources. These sites are compatible with older clock modules designed for the ML571 serial digital video board, as well as new clock modules designed specifically for the FMC card. The clock modules can provide reference clocks to the serial transceivers on the carrier board. The clock modules can also provide other clock frequencies, such as audio clocks, to regional and global clock inputs of the carrier board FPGA. Each clock module can provide multiple clocks to the carrier board or to other clock synthesis resources on the FMC card.
- A Spartan®-3A FPGA controls all operations on the FMC card and provides a simple serial peripheral interface (SPI) to the carrier board.

Installation

The FMC card plugs into the HPC FMC connector on the ML605 carrier board or into the only FMC connector on the SP605 board. It draws all of its power from the carrier board through the FMC connector.

When connected to the ML605 carrier board, the FMC card interferes with some connectors along the top edge of the carrier board. It is difficult to plug the power connector from the power brick into the ML605 power connector with the FMC card installed. Xilinx provides a short adapter cable that allows the power brick to plug into the vertical ATX-style power connector located just below the regular power connector on the ML605 carrier board.

The carrier board can either include or exclude the JTAG chain of the FMC card into its JTAG chain. A jumper, located near the FMC connector, must be moved to include the FMC card in the carrier board JTAG chain. There are two devices on the FMC card JTAG chain, a Spartan-3A FPGA and a Xilinx® Platform Flash PROM used to program the Spartan-3A device.

The Spartan-3A FPGA can be configured from either the Platform Flash PROM, or through JTAG using the iMPACT (included in the ISE® development software tools) or ChipScope™ tools. For all standard SDI demonstrations, the Spartan-3A FPGA is configured from the Platform Flash PROM. If the revision of the code in the Platform Flash PROM is out-of-date and needs to be updated, the iMPACT tool can be used to burn a new MCS file into the Platform Flash PROM. This is accomplished by right-clicking on the xcf02s device icon shown in the iMPACT Boundary Scan view (Figure 1), selecting the **Assign New Configuration File...** option, and then right-clicking on the xcf02s device icon and selecting the **Program** option.

There is a JTAG jumper on the FMC card that allows the inclusion or exclusion of JTAG devices on an expansion FMC card plugged into the expansion FMC connector on the FMC card. If no expansion FMC card is plugged into the FMC card, or the expansion card does not have a JTAG chain, this jumper must be in the EXP_OUT position (jumper connecting the left two pins of the connector) for the FMC card JTAG chain to work. This jumper, labeled JTAG CONFIG, is located just below the expansion FMC connector.

Figure 1 shows the devices on the JTAG chain of the ML605 board and FMC card as viewed by the iMPACT tool.

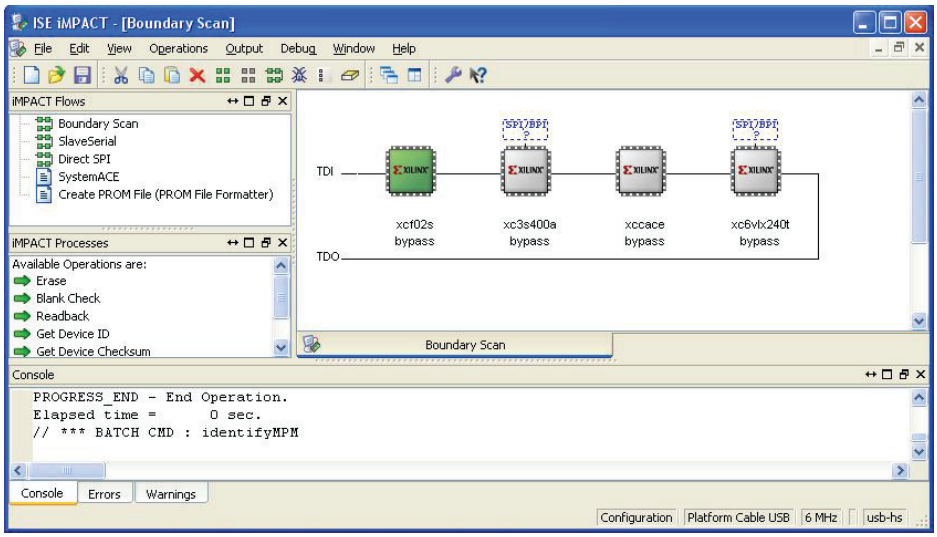

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Figure 1: **ML605 Board and FMC Card JTAG Chain**

Clock Block Diagram

The main clock paths of the FMC card are shown in Figure 2. The Spartan-3A FPGA can provide either the 27 MHz local XO or the horizontal sync signal from the LMH1981 sync separator to the Si5324 device, or, the Si5324 device can take a reference clock from the carrier board. If provided from the 27 MHz local XO, any of the standard SDI reference clock frequencies (148.5 MHz, 148.5/1.001 MHz, 74.25 MHz, and 74.25/1.001 MHz) can be synthesized. A 24.576 MHz clock frequency, often used for audio interfaces, can also be synthesized. If the horizontal sync signal is used, the Si5324 device can synthesize 27 MHz.

One output of the Si5324 device is connected to a global or regional clock pin on the FMC connector. The other output of the Si5324 device is connected to clock crossbar 1, where it can be routed to a serial transceiver reference clock pin, or to global or regional clock inputs of the FPGA on the carrier board.

The clocks from the clock modules are applied to the clock crossbars, directly to the FMC connector, or back to the Spartan-3A FPGA. The reference clock inputs to the clock modules can come from the FMC connector, the Spartan-3A FPGA, or from the clock crossbars.

The sync separator's outputs are applied to the Spartan-3A FPGA. The Spartan-3A FPGA can forward them to the FMC connector and to the Si5324 device. The Spartan-3A FPGA also processes the sync signals and determines the frame rate of the video sync signal.

Crossbar 3 handles high-speed signals from either the LVDS signals received via the FMC connector or from two of the serial transceiver outputs, also received from the FMC connector. It can route these signals to either of the other two crossbar switches or to two SDI TX outputs on the FMC card. To drive SDI TX1 and TX2, the signals from the DP0 and DP1 serial transceivers on the carrier board must pass through crossbar 3. Alternatively, these SDI TX outputs can be driven by the LVDS signal for slower speed protocols, such as SD-SDI and DVB-ASI. It is possible to use serial transmitters to synthesize clocks. Crossbar 3 supports this by allowing the output of either serial transmitter to be routed to clock crossbar 1 and clock crossbar 2.

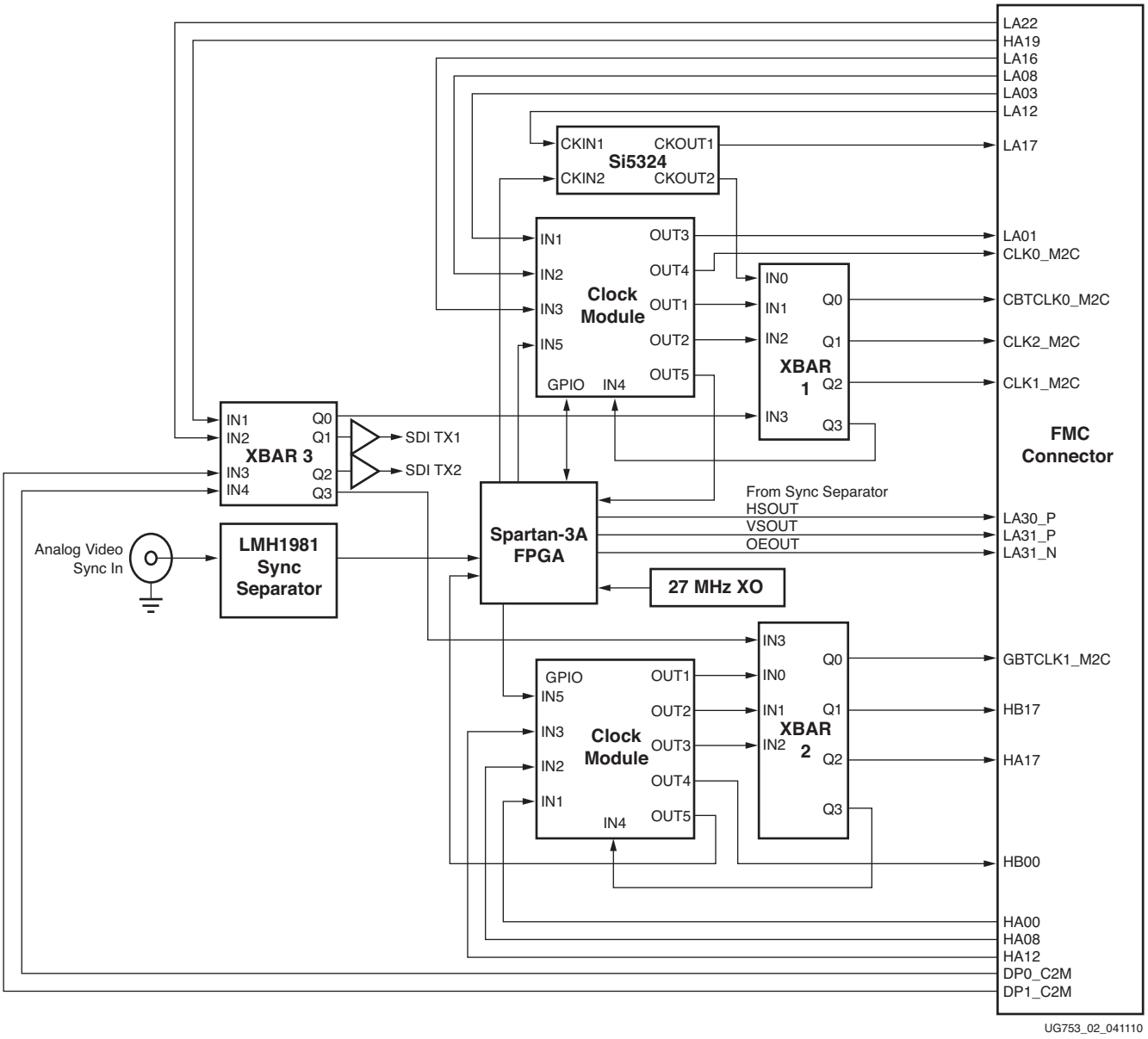

Figure 2: **Clock Paths Block Diagram**

FMC Card Control

Almost all aspects of the FMC card are controlled by the Spartan-3A FPGA. The Spartan-3A FPGA is, in turn, controlled via SPI interfaces connected to the carrier board FPGA through the FMC connector. There are three separate SPI interfaces connected between the carrier board and the Spartan-3A FPGA. One is the main SPI interface for general control of the board. The other two SPI interfaces control the two clock modules. For all three of these SPI interfaces, the carrier board is the master.

The Spartan-3A FPGA interfaces with various devices and the clock modules on the FMC card through I^2C or SPI serial interfaces, or by direct control signals. Figure 3 shows the various I^2C and SPI interfaces on the FMC card.

The `main_avb_control` module provides a simplified control and status interface to the FMC card. This module is instantiated in the carrier board FPGA design. It contains an SPI master that handles all communications between the carrier board FPGA and the FMC card. The module's ports are identified in Table 1.

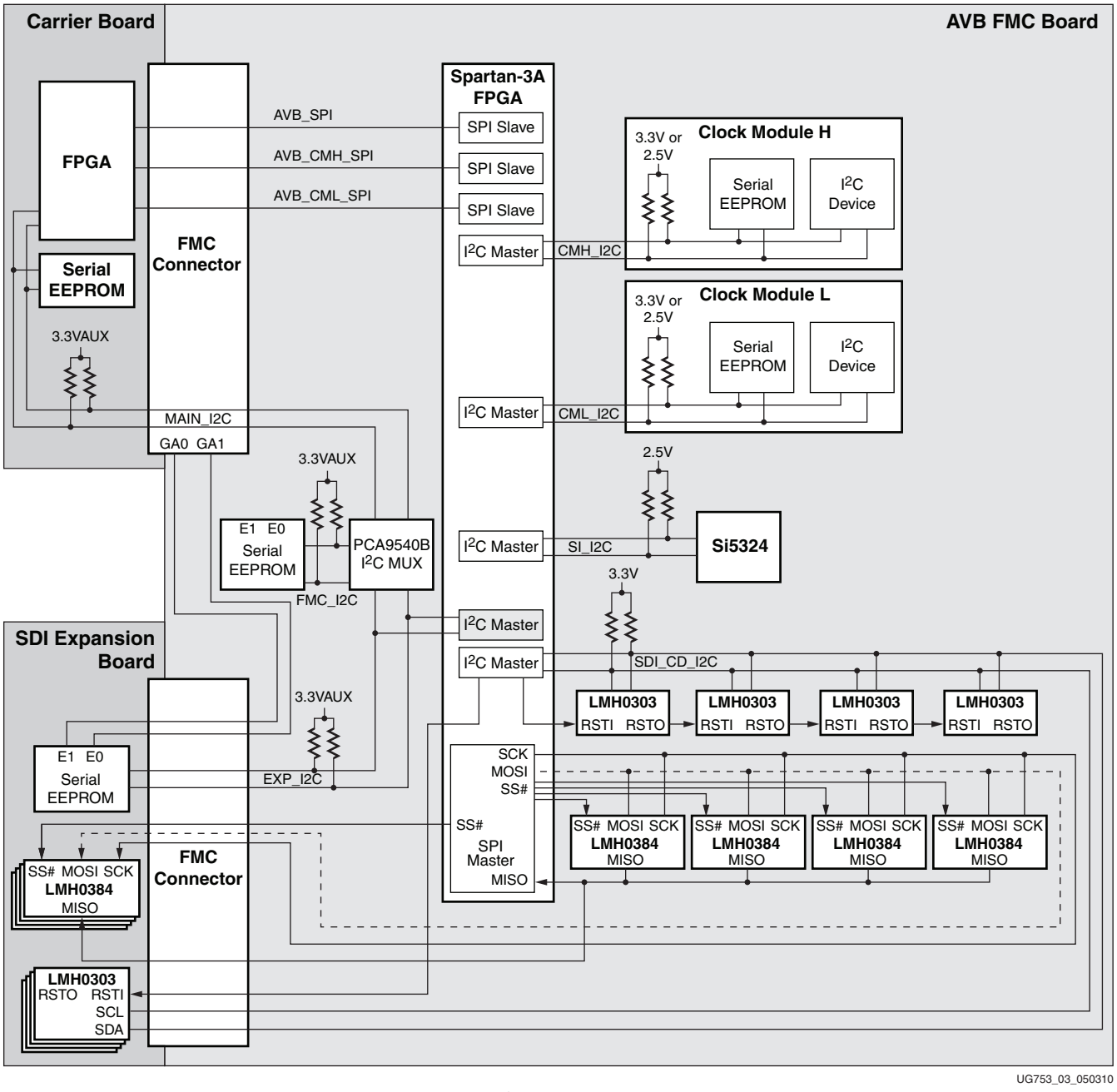

Figure 3: **I²C and SPI Interfaces**

Note relevant to Figure 3:

- The MOSI line to the LMH0384 devices is routed as individual outputs from the Spartan-3A FPGA to each of the four LMH0384 devices on the FMC card and the four devices on the SDI expansion card. This is because the LMH0384 MOSI pin serves as the carrier on other cable equalizer devices. In SPI mode, all eight MOSI lines are

driven identically and act virtually as a single signal. This is represented in Figure 3 as a single dashed line to indicate the special nature of the signal.

Table 1: **Port List for main_avb_control Module**

Name	Width	Direction	Description
clk	1	In	27 MHz clock. Connects to the 27 MHz clock provided by the FMC card on FMC LVDS pair HB06 or LVTTL signal LA18_N_CC (both signals always carry the 27 MHz clock).
rst	1	In	Resets the entire module. Typically, this can be tied Low.
sck	1	Out	Main SPI serial clock. Wired to FMC connector pin LA00_P_CC.
mosi	1	Out	Main SPI master serial data output. Wired to FMC connector pin LA00_N_CC.
miso	1	In	Main SPI master serial data input. Wired to FMC connector pin LA27_P.
ss	1	Out	Main SPI slave select signal. Wired to FMC connector pin LA14_N.
fpga_rev	8	Out	Indicates the revision of the Spartan-3A FPGA configuration on the FMC card.
exp_brd_prsnt	1	Out	Signal is High if there is an expansion FMC card plugged into the FMC card expansion FMC connector.
board_options	8	Out	Indicates build options of the FMC card.
xbar_1_out0_sel	2	In	Selects the signal to drive crossbar 1, output 0: • `00` = Si5324 • `01` = Clock module L, clock output 1 • `10` = Clock module L, clock output 2 • `11` = Crossbar 3, output 0
xbar_1_out1_sel	2	In	Selects the signal to drive crossbar 1, output 1. Same choices as for xbar_1_out0_sel.
xbar_1_out2_sel	2	In	Selects the signal to drive crossbar 1, output 2. Same choices as for xbar_1_out0_sel.
xbar_1_out3_sel	2	In	Selects the signal to drive crossbar 1, output 3. Same choices as for xbar_1_out0_sel.
xbar_2_out0_sel	2	In	Selects the signal to drive crossbar 2, output 0: • `00` = Crossbar 3, output 3 • `01` = Clock module H, clock output 1 • `10` = Clock module H, clock output 2 • `11` = Clock module H, clock output 3
xbar_2_out1_sel	2	In	Selects the signal to drive crossbar 2, output 1. Same choices as for xbar_2_out0_sel.
xbar_2_out2_sel	2	In	Selects the signal to drive crossbar 2, output 2. Same choices as for xbar_2_out0_sel.
xbar_2_out3_sel	2	In	Selects the signal to drive crossbar 2, output 3. Same choices as for xbar_2_out0_sel.

Table 1: **Port List for main_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
xbar_3_out0_sel	2	In	Selects the signal to drive crossbar 3, output 0: • `00` = FMC LVDS pair HA19 • `01` = FMC LVDS pair LA22 • `10` = FMC serial transceiver DP0_C2M • `11` = FMC serial transceiver DP1_C2M
xbar_3_out1_sel	2	In	Selects the signal to drive crossbar 3, output 1. Same choices as for xbar_3_out0_sel.
xbar_3_out2_sel	2	In	Selects the signal to drive crossbar 3, output 2. Same choices as for xbar_3_out0_sel.
xbar_3_out3_sel	2	In	Selects the signal to drive crossbar 3, output 3. Same choices as for xbar_3_out0_sel.
Si5324_reset	1	In	A High on this port resets the main Si5324 chip on the FMC card.
Si5324_clkin_sel	2	In	Selects the clock input and operating mode of the main Si5324 on the FMC card. See Si5324 Device, page 14 for details.
Si5324_out_fsel	4	In	Selects from a predefined set of output frequencies for the Si5324. See Si5324 Device for details.
Si5324_in_fsel	5	In	Selects from a predefined set of input frequencies for the Si5324. See Si5324 Device for details.
Si5324_bw_sel	4	In	Selects the bandwidth of the Si5324 device. Only legal Si5324 device bandwidth settings can be used. The legal settings vary based on the Si5324_out_fsel and Si5324_in_fsel settings. Consult the `Si5324 Bandwidth Settings.htm` file included with the reference design files to determine the correct value.
Si5324_DHOLD	1	In	Driving this port High places the Si5324 device in digital holdover mode. For normal operation, this input must be Low.
Si5324_FOS2	1	Out	When High, this indicates a frequency offset error on CKIN2 of the Si5324 device.
Si5324_FOS1	1	Out	When High, this indicates a frequency offset error on CKIN1 of the Si5324 device.
Si5234_LOL	1	Out	When High, this indicates that the Si5324 device PLL is not locked to the input reference clock.
Si5324_reg_adr	8	In	Register address to peek or poke a register in the Si5234.
Si5324_reg_wr_dat	8	In	Data to be poked into a register in the Si5324 device.
Si5324_reg_rd_dat	8	Out	Data read from a register in the Si5324 device during a peek operation.
Si5324_reg_wr	1	In	This input is asserted High for one clk cycle to initiate a poke into a register in the Si5324 device. The Si5324_reg_adr and Si5324_reg_wr_dat ports must be set up prior to asserting this input. This input must not be asserted if Si5324_reg_rdy is Low.

Table 1: **Port List for main_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
Si5324_reg_rd	1	In	This input is asserted High for one clk cycle to initiate a peek of a register in the Si5324 device. The register address must be set up on Si5324_reg_adr prior to asserting this signal. This input must not be asserted if Si5324_reg_rdy is Low. On the rising edge of clk when this input is High, Si5324_reg_rdy goes Low and stays Low until the data has been read from the Si5324 register and output on Si5324_reg_rd_dat.
Si5324_reg_rdy	1	Out	This output is asserted High when the module is ready to accept a new Si5324 register peek or poke request. If this input is Low, the module is executing the last peek or poke request.
Si5324_error	1	Out	This output is asserted High if the last peek or poke request was NACKed by the Si5324 device on the I^2C bus.
sync_video_fmt	11	Out	This port indicates the number of horizontal sync pulses per field of the external video sync signal as reported by the LMH1981mult-format video sync separator. This number fluctuates when the video sync signal is an interlaced format with different numbers of lines in the two fields. Refer to the *LMH1981 Multi-Format Video Sync Separator* data sheet at the Texas Instrument site for details [Ref 1].
sync_updating	1	Out	The sync_video_fmt port is only valid when this output is Low.
sync_frame_rate	3	Out	Indicates the frame rate of the external video sync signal. This is always the frame rate, even for interlaced video. • `000` = 23.98 Hz • `001` = 24 Hz • `010` = 25 Hz • `011` = 29.97 Hz • `100` = 30 Hz • `101` = 50 Hz • `110` = 59.94 Hz • `111` = 60 Hz
sync_m	1	Out	This output is Low for frame rates of 24, 25, 30, 50, and 60 Hz. It is High for frame rates of 23.98, 29.97, and 59.94 Hz.
sync_error	1	Out	This output is High if the rate detector cannot determine the frame rate of the external sync signal.
sdi_rx1_led	2	In	Controls the SDI RX1 LEDs. See LED Control, page 16 for details.
sdi_rx2_led	2	In	Controls the SDI RX2 LEDs.
sdi_rx3_led	2	In	Controls the SDI RX3 LEDs.
sdi_rx4_led	2	In	Controls the SDI RX4 LEDs.
sdi_rx5_led	2	In	Controls the SDI RX5 LEDs. The SDI RX5 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_rx6_led	2	In	Controls the SDI RX6 LEDs. The SDI RX6 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_rx7_led	2	In	Controls the SDI RX7 LEDs. The SDI RX7 LEDs are only available if the SDI expansion card is connected to the FMC card.

Table 1: **Port List for main_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
sdi_rx8_led	2	In	Controls the SDI RX8 LEDs. The SDI RX8 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_tx1_red_led	2	In	Controls the SDI TX1 red LED.
sdi_tx1_grn_led	2	In	Controls the SDI TX1 green LED.
sdi_tx2_red_led	2	In	Controls the SDI TX2 red LED.
sdi_tx2_grn_led	2	In	Controls the SDI TX2 green LED.
sdi_tx3_red_led	2	In	Controls the SDI TX3 red LED.
sdi_tx3_grn_led	2	In	Controls the SDI TX3 green LED.
sdi_tx4_red_led	2	In	Controls the SDI TX4 red LED.
sdi_tx4_grn_led	2	In	Controls the SDI TX4 green LED.
sdi_tx5_red_led	2	In	Controls the SDI TX5 red LED. The SDI TX5 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_tx5_grn_led	2	In	Controls the SDI TX5 green LED.
sdi_tx6_red_led	2	In	Controls the SDI TX6 red LED. The SDI TX6 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_tx6_grn_led	2	In	Controls the SDI TX6 green LED.
sdi_tx7_red_led	2	In	Controls the SDI TX7 red LED. The SDI TX7 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_tx7_grn_led	2	In	Controls the SDI TX7 green LED.
sdi_tx8_red_led	2	In	Controls the SDI TX8 red LED. The SDI TX8 LEDs are only available if the SDI expansion card is connected to the FMC card.
sdi_tx8_grn_led	2	In	Controls the SDI TX8 green LED.
aes_rx1_red_led	2	In	Controls the AES3 RX1 red LED.
aes_rx1_grn_led	2	In	Controls the AES3 RX1 green LED.
aes_rx2_red_led	2	In	Controls the AES3 RX2 red LED.
aes_rx2_grn_led	2	In	Controls the AES3 RX2 green LED.
aes_tx1_red_led	2	In	Controls the AES3 TX1 red LED.
aes_tx1_grn_led	2	In	Controls the AES3 TX1 green LED.
aes_tx2_red_led	2	In	Controls the AES3 TX2 red LED.
aes_tx2_grn_led	2	In	Controls the AES3 TX2 green LED.
madi_rx_red_led	2	In	Controls the AES10 RX red LED.
madi_rx_grn_led	2	In	Controls the AES10 RX green LED.
madi_tx_red_led	2	In	Controls the AES10 TX red LED.
madi_tx_grn_led	2	In	Controls the AES10 TX green LED.
sync_red_led	2	In	Controls the external sync red LED.

Table 1: **Port List for main_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
sync_grn_led	2	In	Controls the external sync green LED.
sdi_eq_cd_n	8	Out	Indicates the carrier detect (CD) status of the eight SDI cable equalizers. Each bit is asserted Low if the corresponding equalizer is detecting a valid carrier signal. Bit 0 corresponds to SDI RX1. Bit 7 corresponds to SDI RX8. SDI RX4 through RX8 are only available if the SDI expansion card is connected to the FMC card.
sdi_eq_ext_3G_reach	8	In	Enables the extended 3G-SDI reach control algorithm for each SDI cable equalizer. The algorithm is enabled for an equalizer if the corresponding bit is High. Bit 0 corresponds to SDI RX1, and bit 7 corresponds to SDI RX8. Refer to the *LMH0384 3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer* data sheet at the Texas Instruments site for details of this algorithm [Ref 2].
sdi_eq_select	3	In	Selects which SDI cable equalizer's cable length indicator (CLI) value is output on the sdi_eq_cli port.
sdi_eq_cli	8	Out	The CLI value of the SDI cable equalizer selected by the sdi_eq_select port is output on this port. It is continuously updated. Refer to the *LMH0384 3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer* data sheet for details about the CLI value [Ref 2].
sdi_drv_hd_sd	8	In	Selects the slew rate of each SDI cable driver. The cable driver's bit is driven Low for HD-SDI and 3G-SDI, and High for SD-SDI. Bit 0 corresponds to SDI TX1, and bit 7 corresponds to SDI TX8.
sdi_drv_enable	8	In	These bits enable the SDI cable drivers. The cable driver's enable bit is driven High to enable the cable driver, and Low for low power mode. Bit 0 corresponds to SDI TX1, and bit 7 corresponds to SDI TX8.
sdi_drv_fault_n	8	Out	These bits reflect the status of the FAULT output of each SDI cable driver. If a bit is Low, the corresponding cable driver is reporting a fault. That fault can be caused by either no signal on its input or an improperly terminated output load (usually no cable plugged into the connector). To automatically power down SDI cable drivers when they are have no load, the eight bits of this port are connected to the eight bits of the sdi_drv_enable port.

Si5324 Device

The Si5324 device on the FMC card primarily provides a reference clock to the serial transceivers on the carrier board. It can also be used as one of the two frequency synthesis chips needed to implement a genlock solution.

This device provides versatile clock synthesis capabilities. It also can be programmed with very low loop filter bandwidth to reduce low frequency jitter.

The Si5324 device has two clock inputs. One input is driven by the Spartan-3A FPGA, and the other is driven by an LVDS pair from the FMC connector. A two-bit port called Si5324_clkin_sel selects the reference clock source for the Si5324 device, as shown in Table 2.

Table 2: **Si5324 Device Clock Input Source Selection**

Si5324_clkin_sel [1]	Clock Source
00	27 MHz XO
01	External video sync – automatic mode
10 [2]	FMC LA29 LVDS pair
11	External video sync – manual mode

Notes:
1. When running provided demonstrations for this card, changing the Sk5324_clkin_sel selection from the default is not recommended.
2. Code 10 is not a valid code for use with the Si5324_clkin_sel input port on this mezzanine card.

The Spartan-3A FPGA either provides the 27 MHz clock or the external horizontal sync signal to CKIN2 on the Si5324 device. The FMC LA29 LVDS pair is always wired to CKIN1. The Spartan-3A FPGA selects either CKIN1 or CKIN2 based on the Si5324_clkin_sel value.

If the external video sync signal is selected as the reference to the Si5324 device, either automatic or manual mode can be chosen. In automatic mode, the Spartan-3A FPGA determines the frequency of the external sync signal, and automatically programs the input clock frequency of the Si5324 device. In manual mode, the carrier board FPGA specifies the input clock frequency via the Si5324_in_fsel port, as shown in Table 3. The Si5324_out_fsel port specifies the output frequency as shown in Table 3. The Si5324_out_fsel port is four bits wide, and selections 1000 and 1001 are reserved to generate 297 MHz and 297/1.001 MHz, respectively, but these two frequencies are not yet fully supported.

The Spartan-3A FPGA is pre-programmed to support the set of input and output frequency combinations shown in Table 3. Only those combinations with a checkmark are supported as pre-programmed combinations on the FMC card. Other frequency synthesis mappings can be programmed into the Si5324 device using the Si5324 register peek/poke ports.

Table 3: **Pre-Programmed Si5324 Input/Output Frequency Combinations**

Si5324_out_fsel Si5324_in_fsel	0000 27 MHz	0001 74.25 MHz	0010 74.1758 MHz	0011 148.5 MHz	0100 148.3516 MHz	0101 24.576 MHz	0110 148.4258 MHz
0x00 = 480i (NTSC)	✓						
0x01 = 480p	✓						
0x02 = 576i (PAL)	✓						
0x03 = 576p	✓						
0x04 = 720p 24 Hz	✓						
0x05 = 720p 23.98 Hz	✓						
0x06 = 720p 25 Hz	✓						
0x07 = 720p 30 Hz	✓						
0x08 = 720p 29.97 Hz	✓						
0x09 = 720p 50 Hz	✓						
0x0A = 720p 60 Hz	✓						

Table 3: **Pre-Programmed Si5324 Input/Output Frequency Combinations *(Cont'd)***

Si5324_out_fsel Si5324_in_fsel	0000 27 MHz	0001 74.25 MHz	0010 74.1758 MHz	0011 148.5 MHz	0100 148.3516 MHz	0101 24.576 MHz	0110 148.4258 MHz
0x0B = 720p 59.94 Hz	✓						
0x0C = 1080i 50 Hz	✓						
0x0D = 1080i 60 Hz	✓						
0x0E = 1080i 59.94 Hz	✓						
0x0F = 1080p 24 Hz	✓						
0x10 = 1080p 23.98 Hz	✓						
0x11 = 1080p 25 Hz	✓						
0x12 = 1080p 30 Hz	✓						
0x13 = 1080p 29.97 Hz	✓						
0x14 = 1080p 50 Hz	✓						
0x15 = 1080p 60 Hz	✓						
0x16 = 1080p 59.94 Hz	✓						
0x17 = 27 MHz	✓	✓	✓	✓	✓	✓	✓
0x18 = 74.25 MHz	✓	✓	✓	✓	✓	✓	✓
0x19 = 74.1758 MHz	✓	✓	✓	✓	✓		
0x1A = 148.5 MHz	✓	✓	✓	✓	✓	✓	✓
0x1B = 148.3516 MHz	✓	✓	✓	✓	✓		

As identified in Table 3, the Si5324 device only generates 27 MHz output clocks when fed a video sync signal. To implement a genlocked SDI transmitter, for example, the reference clock frequency to the serial transceiver must be 74.25 MHz, 74.1758 MHz, 148.5 MHz, or 148.3516 MHz. Two Si5234 devices can be connected in series with the first one converting the video sync signal to 27 MHz and the second one converting the 27 MHz to the required serial transceiver reference clock frequency. This requires the addition of additional Si5324 devices by adding a Si5324 clock module to one of the clock module sites on the FMC card.

The Si5324 device cannot always generate a 24.576 MHz audio clock from all input clock frequencies. Cascading two Si5324 devices can solve this problem by first converting the input clock to 27 MHz in the first device and then converting it to 24.576 MHz in the second device.

LED Control

Each BNC connector on the FMC card has a red/green LED next to it to indicate the status associated with that connector. The `main_avb_control` module allows the carrier board FPGA to control all of these LEDs. Control ports are also provided to control the LEDs next to the four SDI TX connectors and four SDI RX connectors on the SDI expansion card that can be connected to the expansion FMC connector on the FMC card.

The eight possible SDI RX LEDs (four on the FMC card and four on the SDI expansion card) are controlled by eight two-bit ports. For example, the port named sdi_rx1_led

controls the red and green LEDs next to the SDI RX1 connector. The LEDs are controlled as shown in Table 4. For any active SDI RX connector, mode 11 should be used. This allows the LED to be controlled automatically by the cable equalizer carrier detect signal.

Table 4: **SDI RX LED Control**

sdi_rx*n*_led	LED
00	Off
01	Green On
10	Red On
11	Green if cable EQ CD is asserted, red otherwise.

For all other LEDs, there are separate two-bit ports to independently control the red and green sides of the LED as shown in Table 5.

Table 5: **LED Control for All But SDI RX LEDs**

sdi_rx*n*_led	LED
00	Off
01	On
10	Slow flash
11	Rapid flash

Clock Module Control

There are sites for two clock modules on the FMC card. Clock module H is primarily associated with signals only available if the FMC card is connected to an HPC FMC connector. Clock module L is associated with signals available on either the LPC or the HPC FMC connector.

The carrier board FPGA controls each clock module via a dedicated SPI interface, one SPI interface for each clock module. Different clock modules have different control requirements. Some of them have I^2C interfaces. The Spartan-3A FPGA contains an I^2C master for each clock module which is, in turn, controlled by the SPI interface from the carrier board. Most clock modules have a number of discrete input and output signals. Some of these discrete signals can be connected either directly or through the Spartan-3A FPGA to FMC signals. Others must be controlled or monitored by the carrier board indirectly through the SPI interface.

A module called cm_avb_control can be instantiated in the FPGA on the ML605 or SP605 boards to control one clock module. If both clock modules are installed on the FMC card, then two instances of the cm_avb_control module need to be instantiated in the FPGA, one for each clock module. This module can be used to control any type of clock module, but is specifically designed to control the Cook Technologies CTSLCM1 clock module that has three Si5324 devices on it. The module's ports are identified in Table 6.

Table 6: **Port List for cm_avb_control Module**

Name	Width	Direction	Description
clk	1	In	27 MHz clock. Connects to the 27 MHz clock provided by the FMC card on FMC LVDS pair HB06 or LVTTL signal LA18_N_CC (both signals always carry the 27 MHz clock).
rst	1	In	Resets the entire module. Typically, this can be tied Low.
sck	1	Out	Clock module SPI serial clock. Connects to FMC connector pin LA29_P for clock module L, to HB11_N for clock module H.
mosi	1	Out	Clock module SPI master serial data output. Connects to FMC connector LA07_P for clock module L, to HB07_P for clock module H.
miso	1	In	Clock module SPI master serial data input. Connects to FMC connector LA29_N for clock module L, to HA05_P for clock module H.
ss	1	Out	Clock module SPI slave select signal. Connects to FMC connector LA07_N for clock module L, to HA05_N for clock module H.
module_type	16	Out	Indicates the clock module type. A value of `0x0001` indicates the CTSLCM1 module. Older clock modules do not have identification PROMs and cannot be automatically identified.
module_rev	16	Out	Indicates the revision of the clock module. Older clock modules do not have identification PROMs and cannot be automatically identified.
module_type_valid	1	Out	This output goes High when the FMC card has identified the module type and revision, and outputs the values on the module_type and module_rev ports.
module_type_error	1	Out	This output goes High if the FMC card receives an I^2C bus NACK while attempting to read the module type and revision from the clock module.
clkin5_src_sel	1	In	This input controls a multiplexer in the Spartan-3A FPGA on the FMC card. This multiplexer selects the source of the signal that drives the clock IN5 input of the clock module. If this input is Low, the local 27 MHz XO on the FMC card is routed to clock IN5. If this input is High, an LVDS pair on the FMC connector is routed to clock IN5. For clock module L, this LVDS pair is LA28_P/N. For clock module H, this LVDS pair is HB05_P/N.
gpio_dir_0	8	In	Specifies the direction of clock module the GPIO[7:0] signals. See Clock Module GPIO, page 21 for details. (`0` = output to clock module, `1` = input from clock module.)
gpio_dir_1	8	In	Specifies the direction of clock module the GPIO[15:8] signals.See Clock Module GPIO for details. (`0` = output to clock module, `1` = input from clock module.)
gpio_dir_2	8	In	Specifies the direction of clock module the GPIO[23:16] signals. See Clock Module GPIO for details. (`0` = output to clock module, `1` = input from clock module.)
gp_out_value_0	8	In	Specifies the value to be output to the clock module on the GPIO[7:0] signals that are configured as outputs.
gp_out_value_1	8	In	Specifies the value to be output to the clock module on the GPIO[15:8] signals that are configured as outputs.

Table 6: **Port List for cm_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
gp_out_value_2	8	In	Specifies the value to be output to the clock module on the GPIO[23:16] signals that are configured as outputs.
gp_in_value_0	8	Out	Indicates the current value of the clock module GPIO[7:0] signals that are programmed as inputs.
gp_in_value_1	8	Out	Indicates the current value of the clock module GPIO[15:8] signals that are programmed as inputs.
gp_in_value_2	8	Out	Indicates the current value of the clock module GPIO[23:16] signals that are programmed as inputs.
gp_in	4	Out	Indicates the current value of the clock module GPIN[3:0] signals. These are outputs of the clock module to the Spartan-3A FPGA on the FMC card.
i2c_slave_adr	8	In	I^2C bus slave address. See Clock Module I^2C Peek and Poke, page 23 for details.
i2c_reg_adr	8	In	I^2C bus register address. See Clock Module I^2C Peek and Poke for details.
i2c_reg_dat_wr	8	In	Data written during the next I^2C bus poke operation. See Clock Module I^2C Peek and Poke for details.
i2c_reg_wr	1	In	A High on this port causes an I^2C bus poke operation. See Clock Module I^2C Peek and Poke for details.
i2c_reg_rd	1	In	A High on this port causes an I^2C bus peek operation. See Clock Module I^2C Peek and Poke for details.
i2c_reg_dat_rd	8	Out	Data read from clock module during last peek operation. See Clock Module I^2C Peek and Poke for details.
i2c_reg_rdy	1	Out	When this output is High, the previously requested peek or poke operation has been completed and a new peek or poke operation may be requested. See Clock Module I^2C Peek and Poke for details.
i2c_reg_error	1	Out	When this output is High, the previously requested peek or poke operation received an I^2C bus NACK. See Clock Module I^2C Peek and Poke for details.
These ports are only valid when controlling a CTSLCM1 clock module. There are three Si5324 devices on this module identified as A, B, and C.			
Si5324_A_clkin_sel	1	In	Controls the clock in the select multiplexer of Si5324 A: • `0` = select CKIN1 • `1` = select CKIN2
Si5324_A_out_fsel	4	In	Selects the output frequency of Si5324 A. See Table 3, page 15.
Si5324_A_in_fsel	5	In	Specifies the input frequency of the reference clock provided to Si5324 A. See Table 3.
Si5324_A_bw_sel	4	In	Selects the bandwidth of the Si5324 A. Only legal Si5324 bandwidth settings can be used. The legal settings vary based on the Si5324_out_fsel and Si5324_in_fsel settings. Consult the `Si5324 Bandwidth Settings.htm` file included with the reference design files to determine the correct value.
Si5324_A_DHOLD	1	In	Driving this port High places the Si5324 A in digital holdover mode. For normal operation, this input must be Low.

Table 6: **Port List for cm_avb_control Module *(Cont'd)***

Name	Width	Direction	Description
Si5324_A_FOS2	1	Out	When High, this indicates a frequency offset error on CKIN2 of Si5324 A.
Si5324_A_FOS1	1	Out	When High, this indicates a frequency offset error on CKIN1 of Si5324 A.
Si5324_A_LOL	1	Out	When High, this indicates that the Si5324 A PLL is not locked to the input reference clock.
Si5324_B_clkin_sel	1	In	Controls the clock in the select multiplexer of Si5324 B: • `0` = select CKIN1 • `1` = select CKIN2
Si5324_B_out_fsel	4	In	Selects the output frequency of Si5324 B. See Table 3, page 15.
Si5324_B_in_fsel	5	In	Specifies the input frequency of the reference clock provided to Si5324 B. See Table 3.
Si5324_B_bw_sel	4	In	Selects the bandwidth of the Si5324 B. Only legal Si5324 device bandwidth settings can be used. The legal settings vary based on the Si5324_out_fsel and Si5324_in_fsel settings. Consult the `Si5324 Bandwidth Settings.htm` file included with the reference design files to determine the correct value.
Si5324_B_DHOLD	1	In	Driving this port High places the Si5324 B in digital holdover mode. For normal operation, this input must be Low.
Si5324_B_FOS2	1	Out	When High, this indicates a frequency offset error on CKIN2 of Si5324 B.
Si5324_B_FOS1	1	Out	When High, this indicates a frequency offset error on CKIN1 of Si5324 B.
Si5324_B_LOL	1	Out	When High, this indicates that the Si5324 B PLL is not locked to the input reference clock.
Si5324_C_clkin_sel	1	In	Controls the clock in the select multiplexer of Si5324 C: • `0` = select CKIN1 • `1` = select CKIN2
Si5324_C_out_fsel	4	In	Selects the output frequency of Si5324 C. See Table 3.
Si5324_C_in_fsel	5	In	Specifies the input frequency of the reference clock provided to Si5324 C. See Table 3.
Si5324_C_bw_sel	4	In	Selects the bandwidth of the Si5324 C. Only legal Si5324 bandwidth settings can be used. The legal settings vary based on the Si5324_out_fsel and Si5324_in_fsel settings. Consult the `Si5324 Bandwidth Settings.htm` file included with the reference design files to determine the correct value.
Si5324_C_DHOLD	1	In	Driving this port High places the Si5324 C in digital holdover mode. For normal operation, this input must be Low.
Si5324_C_FOS2	1	Out	When High, this indicates a frequency offset error on CKIN2 of Si5324 C.
Si5324_C_FOS1	1	Out	When High, this indicates a frequency offset error on CKIN1 of Si5324 C.
Si5324_C_LOL	1	Out	When High, this indicates that the Si5324 C PLL is not locked to the input reference clock.

Each clock module can have up to five reference clock inputs and up to five clock outputs, as shown in Figure 2, page 8.

Clock Module GPIO

Each clock module can have a number of general-purpose input and output signals. Some of these are controlled indirectly through the `cm_avb_control` module's GPIO control and status ports. Others are wired directly to FMC connector pins.

Table 7 shows how the 24 GPIO signals and 4 GPIN signals map to signals on the clock module. The direction of each of the 24 GPIO signals is controlled by the gpio_dir_0, gpio_dir_1, and gpio_dir_2 ports on the `cm_avb_control` module. Signals programmed as outputs (gpio_dir bit = `0`), are output from the Spartan-3A FPGA on the FMC card to input pins on the clock module. The values of these outputs are controlled by the gpio_out_value_0, gpio_out_value_1, and gpio_out_value_2 ports on the `cm_avb_control` module. Signals programmed as inputs (gpio_dir bit = `1`) are output from the clock module and input to the Spartan-3A FPGA on the FMC card. The status of each of these signals is periodically updated on the gpio_in_value_0, gpio_in_value_1, and gpio_in_value_2 ports of the `cm_avb_control` module. There are four additional signals that are always outputs from the control module and wired to inputs of the Spartan-3A FPGA on the FMC card. The status of each of these four signals is periodically updated on the gp_in port of the `cm_avb_control` module.

Table 7: **Clock Module GPIO and GPIN Signals**

GPIO/GPIN Signal	Clock Module Pin	Use on CTSLCM1
GPIO 0	J1-27 (CM_D_1)	
GPIO 1	J1-31 (CM_D_2)	
GPIO 2	J1-33 (CM_D_3)	
GPIO 3	J1-37 (CM_D_4)	
GPIO 4	J1-39 (CM_D_5)	
GPIO 5	J1-14 (CM_D_6)	
GPIO 6	J1-16 (CM_D_7)	
GPIO 7	J1-20 (CM_D_8)	
GPIO 8	J1-28 (CM_D_11)	
GPIO 9	J1-32 (CM_D_12)	
GPIO 10	J1-34 (CM_D_13)	
GPIO 11	J1-38 (CM_D_14)	
GPIO 12	J1-40 (CM_D_15)	
GPIO 13(1)	J2-25 (CM_D_16)	Si5324 C CKOUT2
GPIO 14	J2-27 (CM_D_17)	
GPIO 15	J2-31 (CM_D_18)	
GPIO 16	J2-33 (CM_D_19)	
GPIO 17	J2-37 (CM_D_20)	Si5324 A RST#
GPIO 18	J2-39 (CM_D_21)	Si5324 A INT
GPIO 19	J2-14 (CM_D_22)	
GPIO 20	J2-16 (CM_D_23)	Si5324 B RST#

Table 7: **Clock Module GPIO and GPIN Signals *(Cont'd)***

GPIO/GPIN Signal	Clock Module Pin	Use on CTSLCM1
GPIO 21	J2-20 (CM_D_24)	Si5324 B INT
GPIO 22	J2-28 (CM_D_27)	Si5324 C RST#
GPIO 23	J2-40 (CM_D_31)	Si5324 C INT
GPIN 0	J2-22 (CM_D_25)	
GPIN 1	J2-26 (CM_D_26)	
GPIN 2	J2-34 (CM_D_29)	
GPIN 3	J2-38 (CM_D_30)	

Notes:

1. GPIO 13 is dual use. It can be either a general-purpose I/O signal, or it can be the fifth clock output of the clock module. On the CTSLCM1 module, it is the fifth clock output. If used on older clock modules, it is a general-purpose I/O signal. When the CTSLCM1 module is used, this GPIO signal must never be programmed as an output. The clock signal on this pin on the CTSLCM1 is available on the LA24_P/N FMC pins for clock module L and on the HA00_P/N_CC FMC pins for clock module H.
2. In addition, clock module pin J1-26 is reserved on most modules for the I^2C bus SCL signal and J1-22 for the I^2C bus SDA signal. These signals are controlled by the I^2C controller located in the Spartan-3A FPGA on the FMC card. These two clock module pins cannot be controlled directly by the carrier board.

Clock Module Clock Signals

Table 8 shows how the five reference clock inputs and five clock outputs of the each clock module are connected.

Table 8: **Clock Module Clock Signals**

Clock Module Signal	Clock Module L Connection	Clock Module H Connection	Use on CTSLCM1
Clock In 1	FMC LA03_P/N	FMC HA04_P/N	Si5324 C CKIN2
Clock In 2	FMC LA08_P/N	FMC HA08_P/N	Si5324 A CKIN2
Clock In 3	FMC LA16_P/N	FMC HA12_P/N	Si5324 B CKIN2
Clock In 4	Clock Crossbar 1, Output 3	Clock Crossbar 2, Output 3	Si5324 C CKIN1
Clock In 5	Clock Mux in Spartan-3A FPGA	Clock Mux in Spartan-3A FPGA	Si5324 A CKIN1
Clock Out 1	Clock Crossbar 1, Input 1	Clock Crossbar 2, Input 1	Si5324 B CKOUT1
Clock Out 2	Clock Crossbar 2, Input 2	Clock Crossbar 2, Input 2	Si5324 C CKOUT1
Clock Out 3	FMC LA01_P/N_CC	Clock Crossbar 2, Input 3	Si5324 A CKOUT1
Clock Out 4	FMC CLK0_M2C_P/N	FMC HB00_P/N_CC	Si5324 B CKOUT2
Clock Out 5(1)	FMC LA24_P/N	FMC HA00_P/N_CC	Si5324 C CKOUT2

Notes:

1. GPIO 13 is dual use. It can be either a general-purpose I/O signal, or it can be the fifth clock output of the clock module. On the CTSLCM1 module, it is the fifth clock output. If used on older clock modules, it is a general-purpose I/O signal. When the CTSLCM1 module is used, this GPIO signal must never be programmed as an output. The clock signal on this pin on the CTSLCM1 is available on the LA24_P/N FMC pins for clock module L and on the HA00_P/N_CC FMC pins for clock module H.
2. In addition, clock module pin J1-26 is reserved on most modules for the I^2C bus SCL signal and J1-22 for the I^2C bus SDA signal. These signals are controlled by the I^2C controller located in the Spartan-3A FPGA on the FMC card. These two clock module pins cannot be controlled directly by the carrier board.

Clock Module I2C Peek and Poke

The cm_avb_control module gives the carrier board FPGA access to any register in any device connected to the I2C bus of the clock module to which it is connected. A set of ports on the cm_avb_control module allows the carrier board FPGA to read from or write to any I2C bus location.

To write to a location, the i2c_reg_rdy signal must be High, indicating that there are no pending I2C bus peek and poke operations in progress. Then, the I2C device slave address must be specified on the i2c_slave_adr port. The address of the register in the device must be specified on the i2c_reg_adr port. The data written to the register must be specified on the i2c_reg_dat_wr port. After these three ports are set up correctly, the i2c_reg_wr port signal must be asserted High for one clock cycle to initiate the poke operation. The i2c_reg_rdy output goes Low at the first rising edge of the clock after i2c_reg_wr is asserted, and stays Low until the poke operation is completed. When i2c_reg_rdy goes High, i2c_reg_error is normally Low, but it goes High if the operation receives a negative acknowledge (NACK) on the I2C bus, usually indicating an error condition.

To read a location, the i2c_reg_rdy signal must be High. Then, the I2C device slave address must be specified on the i2c_slave_adr port. The address of the register in the device must be specified on the i2c_reg_adr port. The i2c_reg_rd port must be asserted High for one clock cycle to initiate the peek operation. The i2c_reg_rdy output goes Low at the next rising edge of the clock after i2c_reg_rd is asserted and stays Low until the peek operation is completed. When i2c_reg_rdy goes High, the data read from the device is present on the i2c_reg_dat_rd port. The i2c_reg_error output goes High if the operation received a NACK, usually indicating an error condition.

For debugging purposes, the I2C peek and poke ports of the cm_avb_control module can be interfaced to a ChipScope™ analyzer VIO module, allowing manual peek and poke capability for any device connected to the I2C bus.

CTSLCM1 Clock Module

This clock module from Cook Technologies was designed specifically for the FMC card. Older clock modules are compatible with the FMC card, but are smaller. The CTSLCM1 is larger so that it can be securely fastened to the FMC card with four screws.

This clock module has three Silicon Labs Si5324 devices on it. Figure 4 shows a block diagram of this clock module.

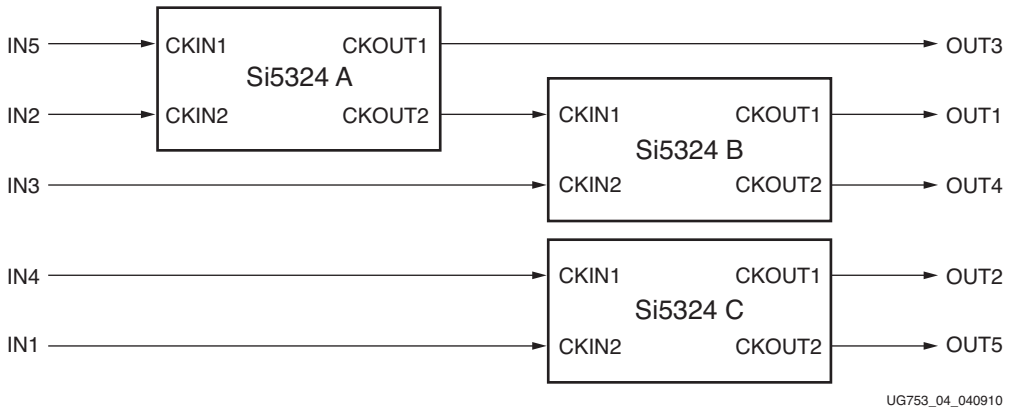

Figure 4: **CTSLCM1 Clock Module**

There are five reference clock inputs and five output clocks on this clock module. The CKOUT2 output of device Si5324 A is permanently connected to the CKIN1 input of device Si5324 B. This allows these two Si5324 devices to be cascaded when CKIN1 is selected as the reference clock source for the Si5324 B device.

The three Si5324 devices are controlled by an I^2C master in the Spartan-3A FPGA on the FMC card, via the I^2C bus. The I^2C master is implemented in a PicoBlaze™ processor that is pre-programmed to configure the Si5324 devices with a variety of synthesis schemes useful for SDI applications. This is the same set of synthesis schemes available for the Si5324 device located directly on the Si5324 device, and described in Table 3, page 15.

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Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For continual updates, add the Answer Record to your myAlerts:

www.xilinx.com/support/myalerts.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

These Xilinx documents and product pages provide supplemental material useful with this guide:

Virtex-6 FPGA Broadcast Connectivity Kit
www.xilinx.com/products/boards-and-kits/DK-V6-BCCN-G.htm

Virtex-6 FPGA ML605 Evaluation Kit
www.xilinx.com/products/boards-and-kits/EK-V6-ML605-G.htm

Spartan-6 FPGA SP605 Evaluation Kit
www.xilinx.com/products/boards-and-kits/EK-S6-SP605-G.htm

The Virtex-6 FPGA Broadcast Connectivity Kit Master Answer Record
www.xilinx.com/support/answers/43656.htm

The Spartan-6 FPGA SP605 Evaluation Kit Master Answer Record
www.xilinx.com/support/answers/33839.htm

The Virtex-6 FPGA ML605 Evaluation Kit Master Answer Record
xkb/Pages/34836.aspx

XAPP1075, *Implementing Triple-Rate SDI with Virtex-6 FPGA GTX Transceivers*

References

The following websites provide supplemental material useful with this guide:

1. Texas Instruments, *LMH1981 Multi-Format Video Sync Separator*
   http://www.ti.com/lit/ds/snls214g/snls214g.pdf
2. Texas Instruments, *LMH0384 3 Gbps HD/SD SDI Extended Reach and Configurable Adaptive Cable Equalizer*
   http://www.ti.com/lit/ds/snls308e/snls308e.pdf

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Appendix B

Warranty

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(iii) Development Systems procured through unauthorized third parties; and
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