Multi-Channel 25G Reed-Solomon Forward Error Correction

PB057 (v1.0) December 5, 2018 **LogiCORE IP Product Brief**

Introduction

The Multi-Channel 25G Reed-Solomon Forward Error Correction implements the Reed-Solomon Forward Error Correction (RS-FEC) sublayer for one to four 25G Ethernet channels, making use of the hard 100G RS-FEC IP block in the Xilinx® UltraScale+™ devices.

Xilinx also provides a soft 25G IEEE 802.3by Reed-Solomon Forward Error Correction IP core. The Multi-Channel 25G RS-FEC is intended for applications where two or more channels are required, a CMAC hard block is available, and there is a need to reduce the amount of logic resources. It is possible to use a combination of the IP cores, for example by using the Multi-Channel 25G RS-FEC core to implement the receive paths and the 25G IEEE 802.3by Reed-Solomon Forward Error Correction soft core for the transmit paths.

Features

- Support for between 1 and 4 parallel 25GE channels using hard RS-FEC function in UltraScale+™ CMAC block
- Conform to IEEE Std 802.3by and *25/50G Gigabit Ethernet Consortium Schedule 3 (v1.6)* (http://25gethernet.org/) specifications
- Pin-level interface compatible with Xilinx® 25G Ethernet subsystem IP
- Support for RS(528,514) encode and decode
- Support for alignment, transcoding, and alignment marker mapping
- Support for standard ±200PPM differences between receive channels' recovered clocks
- Support for symbol error statistics per channel
- Supports latency measurement per channel, including delay added by buffering and CDC
- Support for Virtex® UltraScale+™ and some Kintex® UltraScale+™ parts (with CMAC)

Additional Documentation

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: https://www.xilinx.com/member/25g_rs_fec.html.

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Virtex® UltraScale+™ Kintex® UltraScale+™ Zynq UltraScale+ MPSoC Zynq® UltraScale+™ RFSoC
Supported User Interfaces	Configuration and status bus
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog (Simulation-Only)
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado® Design Suite
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The Multi-Channel 25G RS-FEC core implements up to four instances of the RS-FEC layer which forms part of the IEEE 802.3 25G Ethernet PHY. The RS-FEC layer is shaded in the following figure.

Figure 1: **IEEE Std 802.3 Ethernet Model**

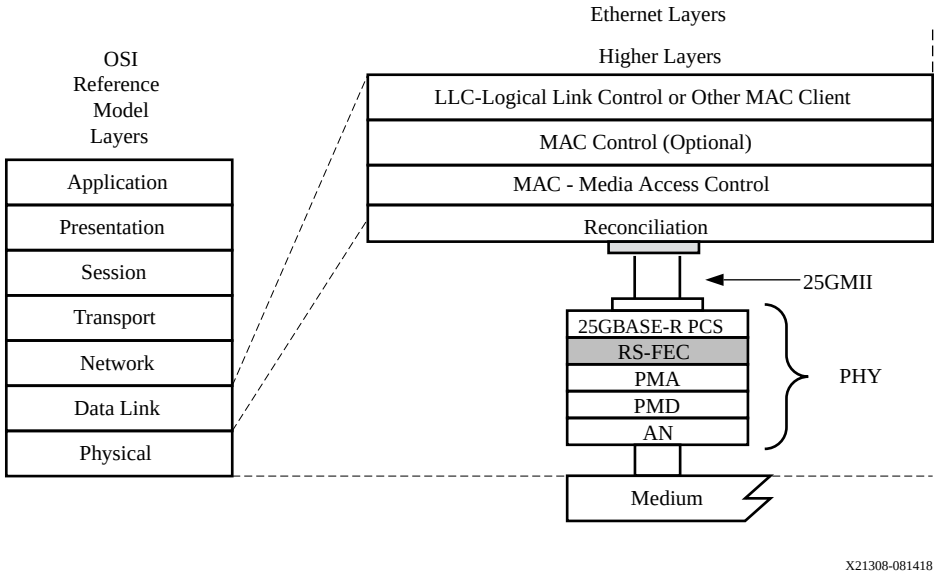

Table 1: **Ethernet Definitions**

Acronym	Definition
25GMII	25 Gigabit Media Independent Interface
AN	Auto-negotiation
LLC	Logical Link Control
MAC	Media Access Control
MDI	Medium Dependent Interface
PCS	Physical Coding Sublayer
PHY	Physical Layer Device
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
RS-FEC	Reed-Solomon Forward Error Correction

The RS-FEC layer of IEEE Std 802.3by defines several stages of synchronization, alignment and transcoding in addition to the RS encoder and decoder.

The operation of each RS-FEC receive and/or transmit channel implemented by the core is independent of the operation of the other channels. Each channel has its own clock and reset input ports, and synchronization or resynchronization on one channel has no effect on any other active link. Error correction statistics and alignment status are reported separately for each channel.

Applications

The Multi-Channel 25G RS-FEC core is used in 25G Ethernet PHY applications such as 25GBASE-SR for switch-to-switch interconnect based on multi-mode fiber and 25GBASE-KR for electrical backplanes.

The core can be connected to up to four 25G Ethernet MAC/PCS IP cores. It is designed to provide logic savings compared to an implementation based on an array of single-channel 25G RS-FEC IP cores, by leveraging the embedded 100G RS-FEC function that exists within the UltraScale+™ CMAC block.

The core operates with a constant latency when alignment lock has been achieved. It also provides cycle-accurate measurements of the delay added by the FEC operation to each transmit and receive channel. This makes it suitable for use in timing-sensitive applications and those where compliance with IEEE-1588 is required.

Unsupported Features

The following features of the IEEE 802.3 standard are not supported in the core:

- The core does not support Energy Efficient Ethernet (EEE), which is an optional feature of IEEE 802.3 defined in Clause 78 of the standard.
- The core does not perform rate compensation for codeword markers within the transmit or receive paths (see sections 108.5.2.2 and 108.5.3.6 of IEEE Std 802.3by). This function is instead performed by the Xilinx 10G/25G High Speed Ethernet Subsystem. The position of codeword markers within the transmitted and received data streams is indicated between the two cores by means of dedicated codeword marker flag signals associated with each data bus.
- The core does not support error indication bypass mode or error correction bypass mode (108.6.1, 108.6.2). Error indication and error correction are always enabled. The RS-FEC itself is also always enabled (108.6.3). To bypass the FEC function entirely, external multiplexing must be implemented to connect the PCS layer directly to the transceivers.

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the Multi-Channel 25G RS-FEC product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx® LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Revision History

Section	Revision Summary
12/05/2018 Version 1.0	
Initial Xilinx release.	N/A

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