LTE RACH Detector v3.1

PB021 February 4, 2021 **LogiCORE IP Product Brief**

Introduction

The Xilinx® LogiCORE™ IP LTE RACH Detector core decodes PRACH data encoded according to the *E-UTRA; Physical channels and modulation (3GPP TS 36.211 v13.0.0)* specification.

Additional Documentation

A full product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_rach_detector_eval.html

Features

- Channel detection for *3GPP TS 36.211 v13.0.0*
- Supports Formats 0-4
- Supports bandwidths: 1.4, 3, 5, 10, 15, and 20 MHz
- Supports up to 64 roots
- Supports up to 4 antennas
- Supports multiplexing in frequency, for up to 6 frequency channels
- C model available for the core
- Fully optimized for speed and area
- Fully synchronous design using either a single clock or separate core and AXI clocks

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Versal™ ACAP UltraScale+™ UltraScale™ Zynq®-7000 SoC 7 Series
Supported User Interfaces	AXI4-Stream Interface AXI4-Register Interface
Resources	Performance and Resource Utilization web page (registration required)
Provided with Core	
Design Files	VHDL and Netlist
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Encrypted VHDL C Model
Supported S/W Driver	Not Applicable
Tested Design Tools(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 54487
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LTE RACH detector core provides a RACH detection solution for the E-UTRA; Physical channels and modulation (3GPP TS 36.211 v13.0.0) specification. The LTE RACH detector searches through the received antenna samples and correlates against one or more (up to 64) RACH preamble sequences. The preamble sequences are based on Zadoff-Chu sequences, as defined in section 5.7 of 3GPP TS 36.211 v13.0.0.

At the eNode-B, the correlation results from the RACH detector are used to detect UE access attempts and compute/update UE transmission timing advance to ensure that the signals received from all UEs are time synchronized within the cyclic prefix (CP).

To accommodate different cell sizes and Doppler conditions, five different RACH formats can be used. Format 0 occupies a single subframe; Formats 1 and 2 occupy two subframes; Format 3 occupies three subframes. Format 4 is available for TDD mode only. The LTE RACH detector can be used to receive RACH transmissions in all five formats.

Within LTE, multiple system bandwidths are supported. The LTE RACH detector can process samples for 1.4, 3, 5, 10, 15, and 20 MHz systems.

The RACH detector core performs a cyclic correlation for each Zadoff-Chu sequence it is configured to detect. This identifies all of the peaks resulting from each cyclic shifted copy of the root.

The transmitted RACH sequence can be multiplexed across up to six frequency channels. Allocation in frequency is achieved by modulating the RACH preamble during baseband signal generation. The RACH detector core demultiplexes these channels, and performs a correlation against the Zadoff-Chu sequences for each channel.

The architecture has been designed to provide efficient use of the FPGA. All processing-intensive and timing-critical operations are performed by the FPGA. The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

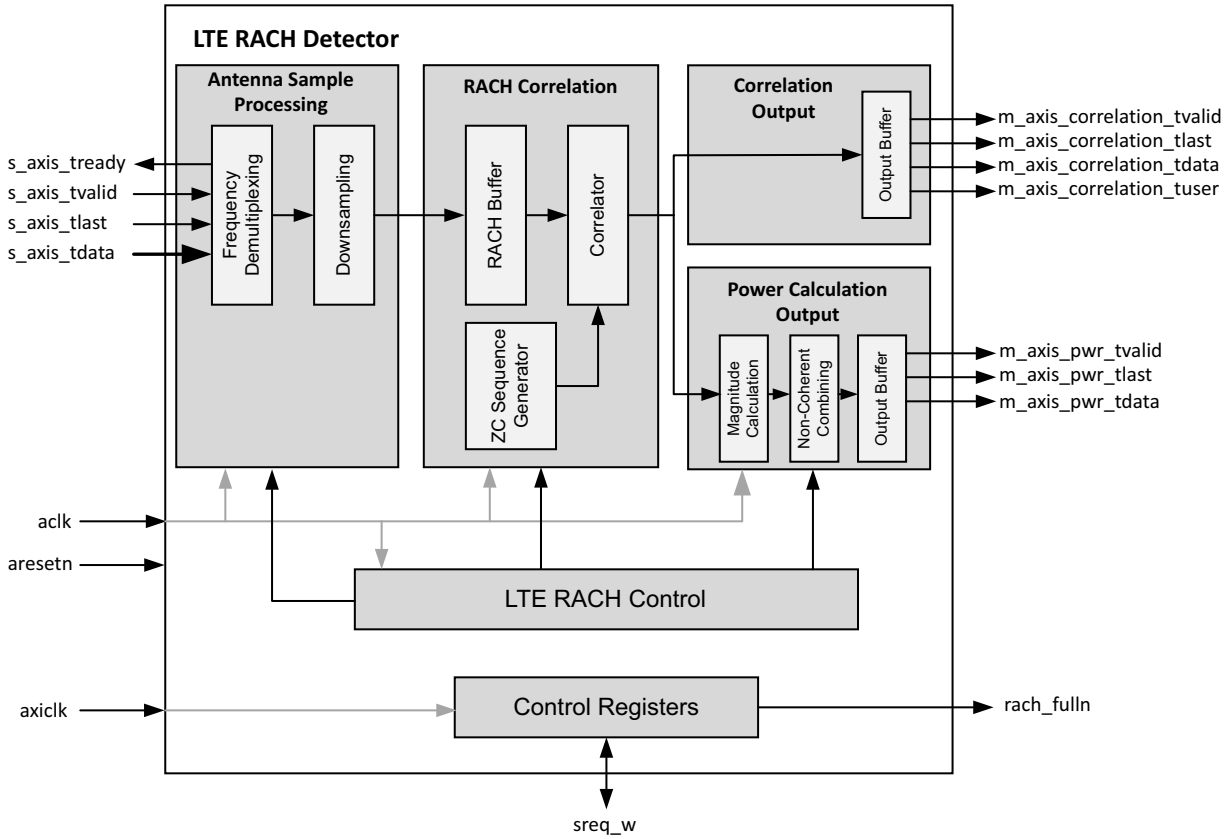

Figure 1: **Internal Structure of the LTE RACH Detector Core**

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities

in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the LTE RACH Detector product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
02/04/2021	3.1	• Added Versal support
10/04/2017	3.1	• Added optional aclken pin • Added optional axiclk domain • Added optional axiclken pin
04/05/2017	3.0	• Added per antenna correlation result port • Updated correlation resolution to be 16Ts • Added support for 15, 3 and 1.4 MHz • Updated interfaces to AXI4-Stream
10/05/2016	2.0	Aligned to Product Guide update.
11/18/2015	2.0	Added support for UltraScale+ families.
06/04/2014	2.0	Initial Xilinx release. This document replaces XMP041.

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