LogiCORE IP LTE MIMO Encoder v4.0

PB017 (v4.0) November 18, 2015 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP 3GPP LTE MIMO Encoder core implements multiple-input, multiple-output (MIMO) encoding for LTE eNodeB applications as defined in the 3GPP TS 36.211 v.9.1 specification [Ref 1]. It represents one IP component in the Xilinx broader LTE baseband platform.

Additional Documentation

A product guide is available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/lte_mimo_enc_eval/index.htm

Features

- AXI4-Stream compliant interfaces
- Implements layer mapping and precoding as defined in the 3GPP TS 36.211 v.9.1 specification [Ref 1]
- Supports both Transmit Diversity and Spatial Multiplexing encoding schemes
- Cyclic Delay Diversity option
- Supports 2 and 4 antennas
- Maximum theoretical throughput supported for systems with up to 20 MHz bandwidth
- Parameterizable input/output data precision

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 All Programmble SoC 7 Series
Supported User Interfaces	AXI4-Stream
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	VHDL Behavioral Verilog and VHDL Structural Model and C Model
Supported S/W Driver	Not Applicable
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Not Applicable
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Applications

The 3GPP LTE MIMO Encoder can be used in base station applications implementing eNodeB following the 3GPP TS 36.211 v.9.1 specification [Ref 1]. The LTE MIMO Encoder can perform the MIMO encoding functions for downlink transmission.

Theory of Operation

The LTE MIMO Encoder is to be part of the eNodeB, the downlink baseband processing that encompasses layer mapping and precoding as defined in [Ref 1]. Figure 1 shows a high-level view of the functionality included in this product.

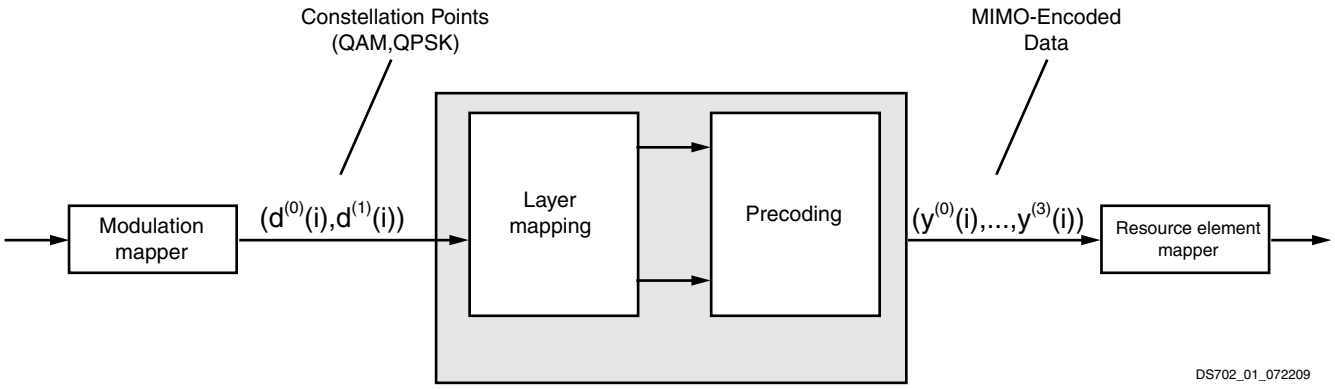

Figure 1: **LTE MIMO Encoder v4.0 Functionality**

C Model

The LTE 3GPP MIMO Encoder core has a bit accurate C model designed for system modeling. The model is bit accurate but not cycle-accurate, so it produces exactly the same output data as the core on a code-word by code-word basis. However, it does not model the core latency or interface signals.

The bit accurate behavioral C model of the LTE MIMO Encoder v4.0 and associated product guide are available to customers. The C model is provided as a dynamically linked library for Windows 32-bit and 64-bit Linux platforms. A `README.txt` file describes the contents of the installed directory structure and any further platform-specific installation instructions.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

For Answer Records related to the LTE 3GPP MIMO Encoder core, see AR: 54469.

Licensing and Ordering Information

A free evaluation version of the core is provided with the Xilinx Vivado Design Suite, which lets you assess the core functionality and demonstrates the various interfaces of the core in simulation. To access the evaluation version visit the 3GPP LTE MIMO Encoder IP Evaluation page.

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the 3GPP LTE MIMO Encoder product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

References

1. Third Generation Partnership Projects (3GPP); Evolved Universal Radio Access (E-UTRA); Physical Channels and Modulation (Release 9), 3GPP TS 36.211 V9.1.0 (2010-03).

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
11/18/2015	4.0	UltraScale+ device support added.
06/04/2014	4.0	Initial Xilinx release. This document replaces XMP026.

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