Virtex-5 XC5VFX30T, XC5VFX70T, XC5VFX100T, XC5VFX130T, and XC5VFX200T CES9988 FPGA Errata

EN060 (v1.1) March 31, 2009 **Errata Notification**

Introduction

Xilinx has made every effort to ensure the highest possible quality. These Virtex®-5 FPGA engineering samples (ES) adhere to the specifications described in the following errata.

Devices

These errata apply to the Virtex-5 devices shown in Table 1.

Table 1: **Virtex-5 Devices Affected by These Errata**

Devices	XC5VFX30T CES9988	JTAG ID (Revision Code): 6
	XC5VFX70T CES9988	JTAG ID (Revision Code): 6
	XC5VFX100T CES9988	JTAG ID (Revision Code): 2
	XC5VFX130T CES9988	JTAG ID (Revision Code): 2
	XC5VFX200T CES9988	JTAG ID (Revision Code): 0
Packages	All	
Speed Grades	-2	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTX Transceivers

The GTX transceivers with a speed grade of -2 covered by this errata (Table 1) operate up to 5.0 Gb/s as specified in DS202, *Virtex-5 FPGA Data Sheet: DC and Switching Characteristics*. These GTX transceivers will support operation above 5.0 Gb/s when used in the modes described in Table 2.

Table 2: **GTX Transceiver Supported Use Models above 5.0 Gb/s in -2 Speed Grade**

Use Model					Maximum Bit Rate Supported	
	Internal Data Width		FPGA Interface Data Width			
Encoding Scheme	INTDATAWIDTH Port	Bits	TXDATAWIDTH (0/1) Ports RXDATAWIDTH (0/1) Ports	Bytes	Maximum Bit Rate (Gb/s) Maximum USRCLK (MHz)	
8B/10B	1	20	2, 1	4, 2	6.5	325
None	1	20	2, 1	4, 2	6.5	325
64B/66B	0	16	2	4	6.25	390.625
64B/67B	0	16	2	4	6.25	390.625
None	0	16	2	4	6.25	390.625

Clock Correction

The Clock Correction feature of the Virtex-5 FPGA GTX transceiver can cause data corruption on the receiver when a clock correction sequence is skipped or added. See UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for more detailed information about the Clock Correction feature.

This issue can occur when all of the following conditions are true:

- Asynchronous operation: When the local reference clock of the Virtex-5 FPGA GTX transceiver is driven from a different oscillator than the far-end transceiver. This introduces a parts per million (PPM) offset in frequency between the operation of the transceivers, requiring clock correction to skip or add clock correction sequences on a periodic basis. This also implies that the RXUSRCLK and RXUSRCLK2 ports of the Virtex-5 FPGA GTX transceiver are derived from the local oscillator and not the RXRECCLK port.
- Clock Correction is enabled.
  - CLK_CORRECT_USE_0/1 attribute is set to **TRUE**.
- The length of the clock correction sequence is 1 or 3 Bytes.
  - CLK_COR_ADJ_LEN_0/1 attribute is set to **1** or **3**.

When the conditions described above are met, one of the multiple work-around options described below shall be used to mitigate this issue. XAUI, PCIe®, SRIO, and Infiniband are the most common protocols affected but only when used in asynchronous operation.

Work-around

If the application permits, implement one of the following work-around options:

•Use synchronous clocking

•Convert to 2 byte or 4 byte clock correction sequence

•If the application does not permit one of these options, see Answer Record 32164.

All versions of UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* subsequent to the current version, v2.1, will properly reflect the Clock Correction behavior described herein.

PowerPC 440 Processor

Branch History Table

The Branch History Table (BHT) must be disabled for deterministic execution latency.

Auxiliary Processor Unit

There are two errata for the Auxiliary Processor Unit (APU):

- After a Translation Look-aside Buffer (TLB) miss caused by an instruction fetch, in a very specific combination of events, the Auxiliary Processor Unit (APU) can lock up or corrupt the data.
- When the floating-point execution is disabled in the PowerPC® 440 processor but enabled in the APU controller, and an FPU instruction is executed, the processor can generate a spurious program exception instead of an FPU-unavailable exception.

Additional Information

For more details, including work-arounds for the processor errata, refer to answer record 30529.

Operational Guidelines

Design Software Requirements

CORE Generator™ software must be used to correctly configure the GTX transceivers.

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.61 (or later), Xilinx ISE™ Design Suite 10.1, Service Pack 2 (or later).
- The stepping should not be set, but if set, it must be set to zero in the user constraint file (UCF):

  CONFIG STEPPING = “0”;

Traceability

The XC5VFX30T CES9988 is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

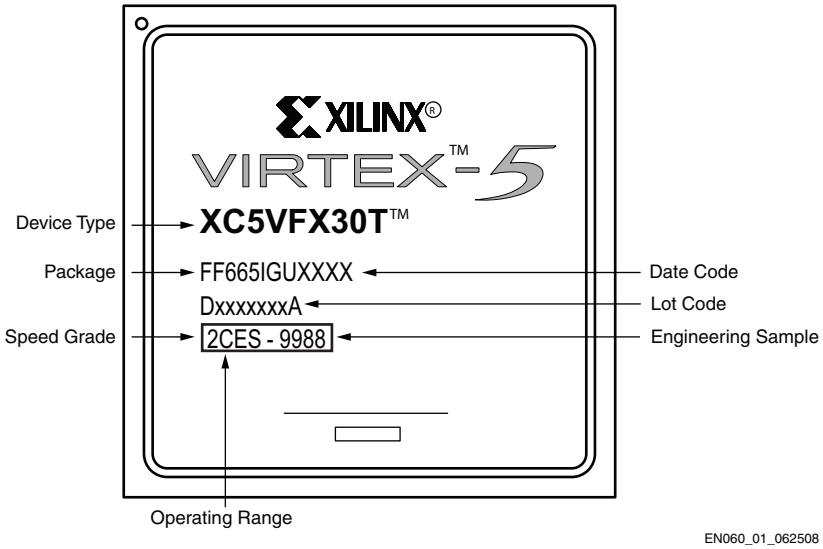

Figure 1: **Example XC5VFX30T CES9988 Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For additional questions regarding these errata, please contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
08/04/08	1.0	Initial Xilinx release.
03/31/09	1.1	Added Clock Correction section.

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XC5VFX100T-1FF1136I4872