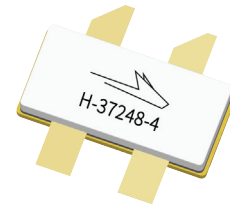


PTRA093302FC

Thermally-Enhanced High Power RF LDMOS FET 330 W, 50 V, 746 – 768 MHz

Description

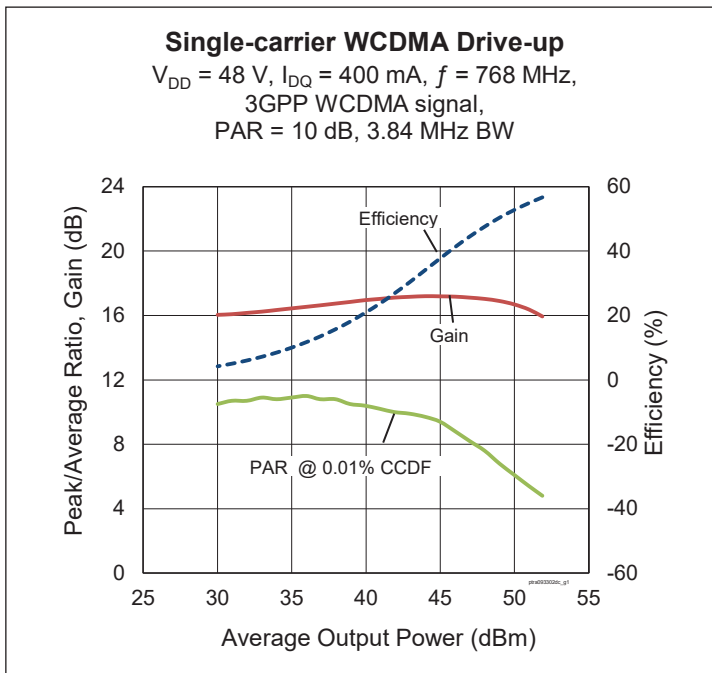
The PTRA093302FC is a 330-watt LDMOS FET with an asymmetric design intended for use in multi-standard cellular power amplifier applications in the 746 MHz to 768 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flange. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTRA093302FC
Package H-37248-4

Features

- Input matched
- Asymmetric Doherty design
 - Main: $P_{1dB} = 150$ W Typ
 - Peak: $P_{1dB} = 175$ W Typ
- Typical Pulsed CW performance, 746–768 MHz, 48 V, combined outputs
 - Output power at $P_{1dB} = 200$ W
 - Efficiency = 54%
 - Gain = 16.5 dB
- Capable of handling 10:1 VSWR @48 V, 79 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS-compliant



RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty production test fixture)

$V_{DD} = 48$ V, $I_{DQ} = 400$ mA, $P_{OUT} = 79$ W avg, $V_{GS(peak)} = (V_{GS} @ I_{DQ} = 400$ mA) – 3.0 V, $f = 768$ MHz. 3GPP WCDMA signal: peak/average = 10 dB @ 0.01% CCDF, channel bandwidth = 3.84 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16.0	17.25	—	dB
Drain Efficiency	η_D	47.0	51.6	—	%
Adjacent Channel Power Ratio	ACPR	—	–32.5	–30.0	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1	μA
	$V_{DS} = 105\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1	μA
On-State Resistance	(main) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.4	—	Ω
	(peak) $V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.3	—	Ω
Operating Gate Voltage	(main) $V_{DS} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$	V_{GS}	3.1	3.56	4.0	V
	(peak) $V_{DS} = 50\text{ V}$, $I_{DQ} = 0\text{ mA}$	V_{GS}	0.2	0.58	1.0	V

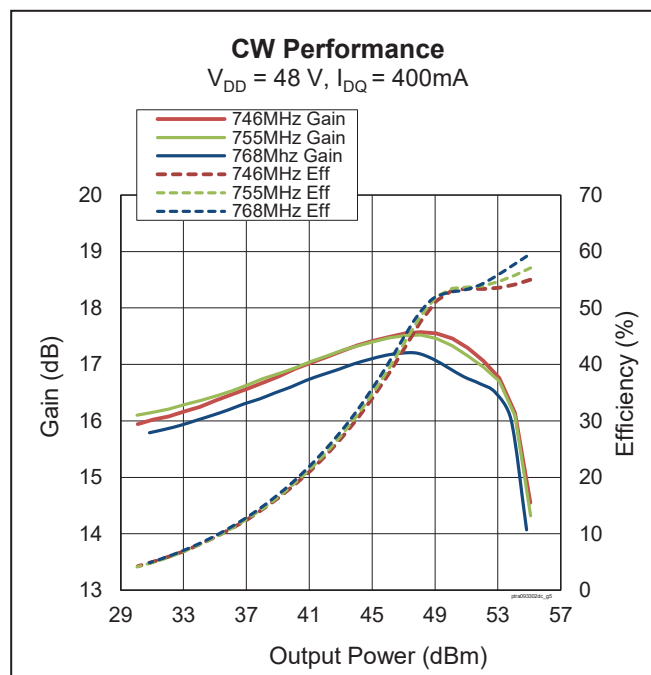
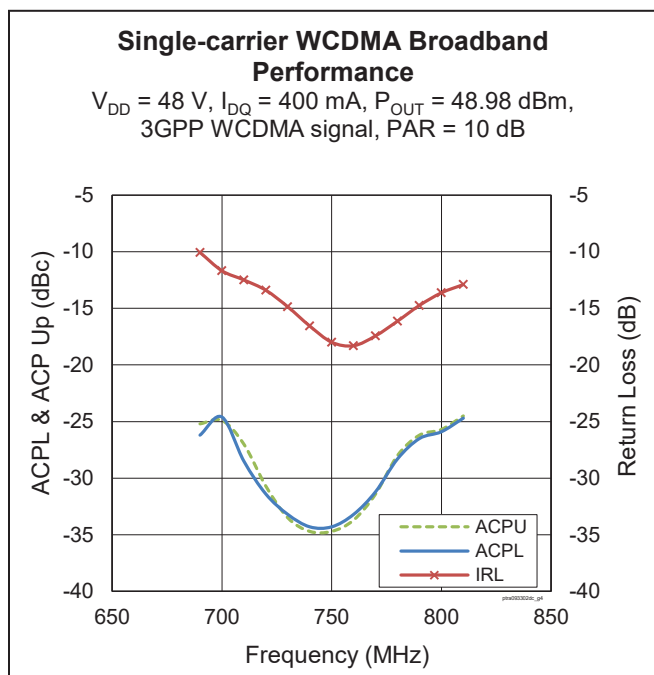
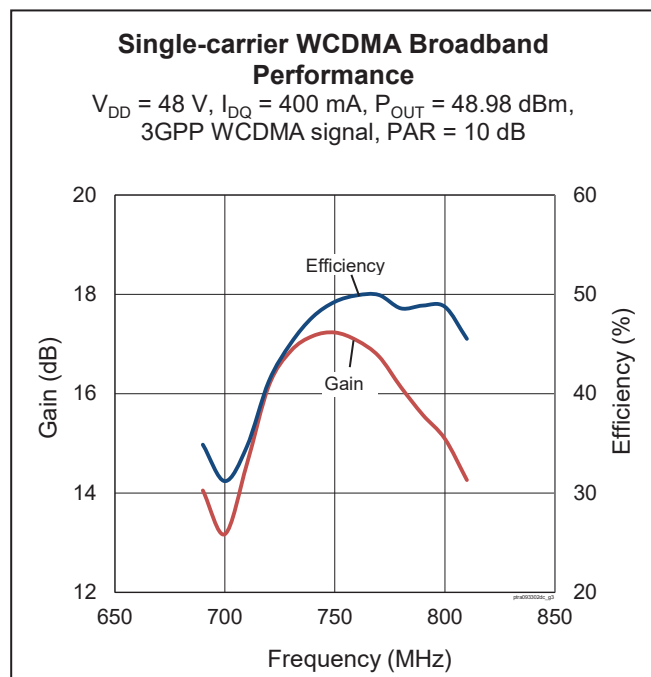
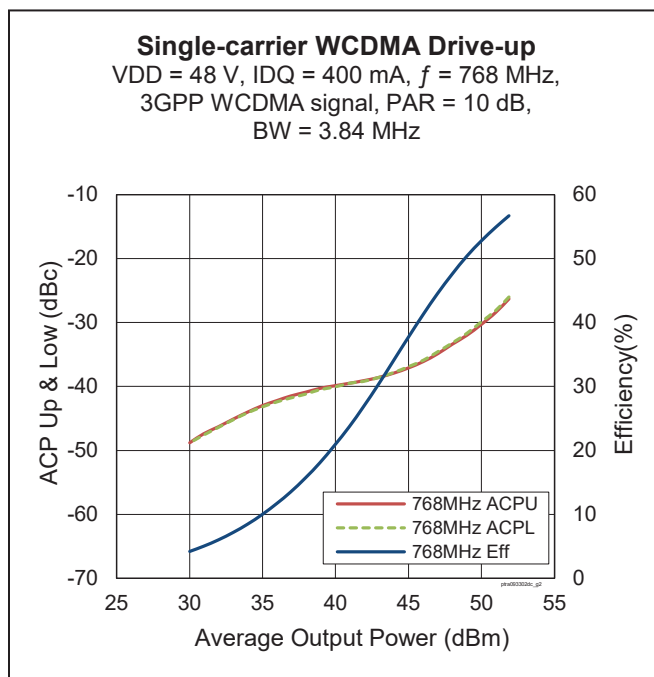
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	−6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−65 to +150	$^{\circ}\text{C}$
Thermal Resistance (main, $T_{CASE} = 70^{\circ}\text{C}$, 79 W CW)	$R_{\theta JC}$	0.56	$^{\circ}\text{C/W}$

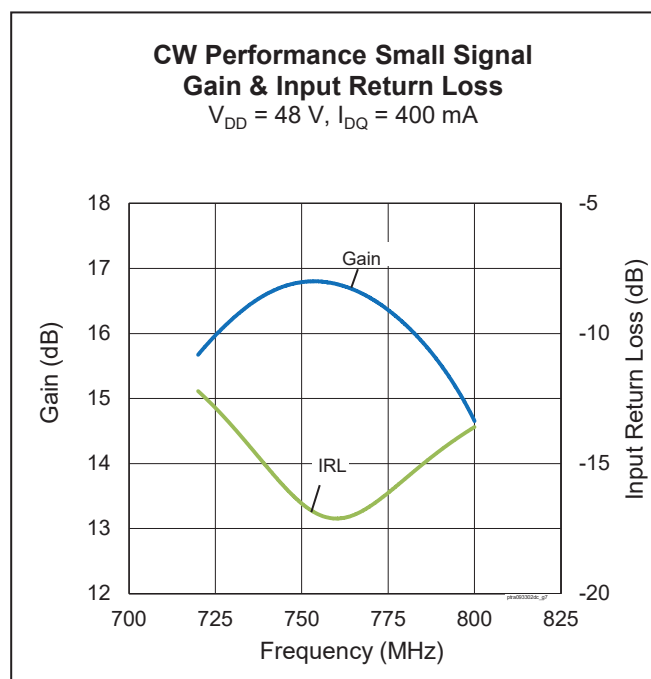
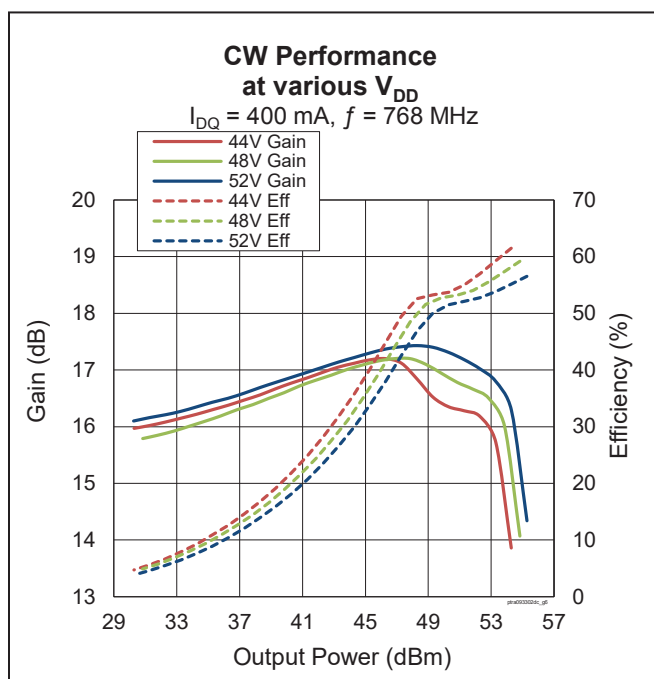
Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTRA093302FC V1 R0	PTRA093302FC-V1-R0	H-37248-4, earless flange	Tape & Reel, 50 pcs
PTRA093302FC V1 R2	PTRA093302FC-V1-R2	H-37248-4, earless flange	Tape & Reel, 250 pcs

Typical RF Performance (data taken in production test fixture)



Typical RF Performance (cont.)



Load Pull Performance

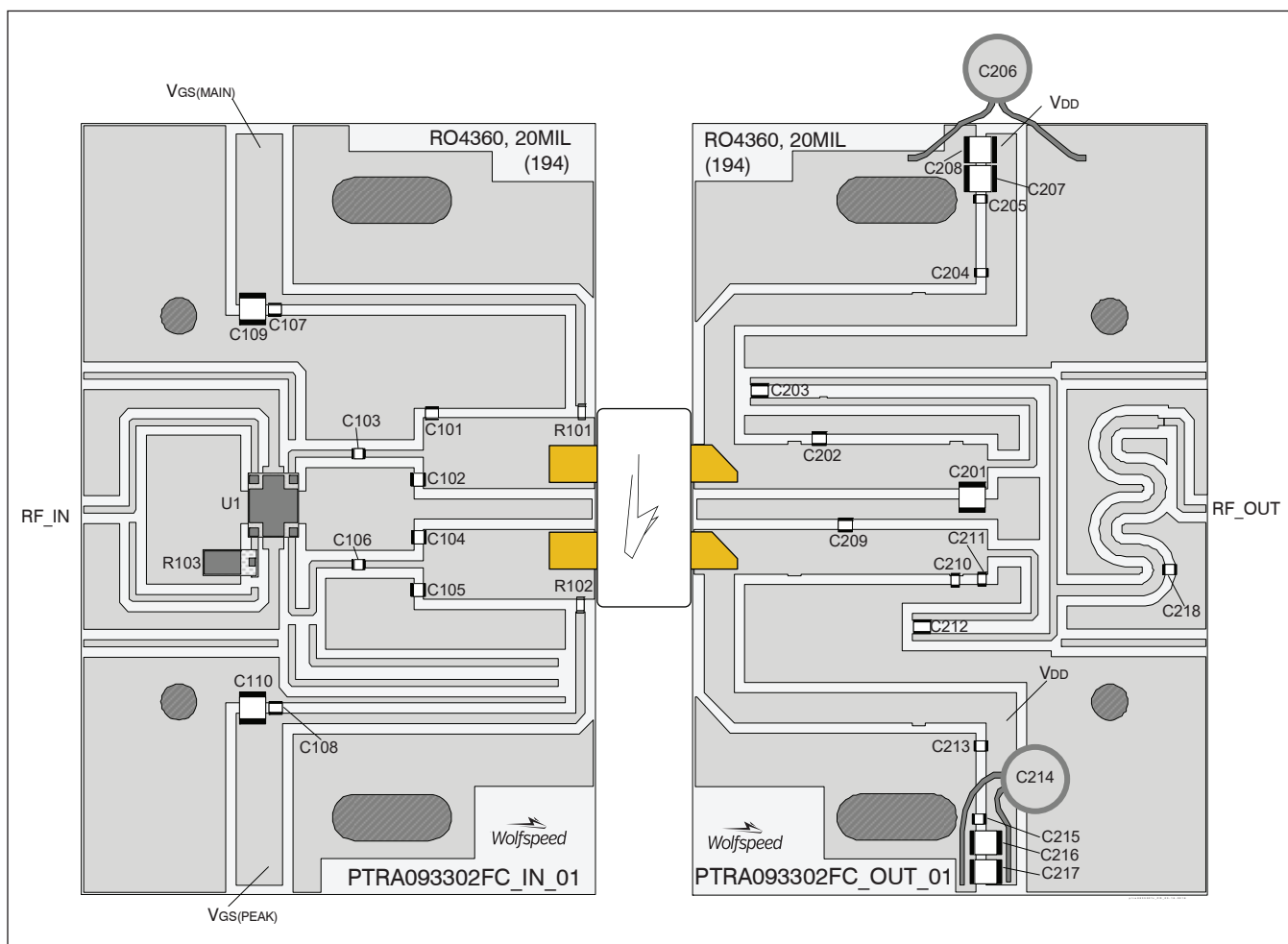
Main Side Load Pull Performance – Pulsed CW signal: 10 μs , 10% duty cycle, 48 V, $I_{DQ} = 300 \text{ mA}$, class AB

Freq [MHz]	Z_s [Ω]	P_{1dB}									
		Max Output Power					Max PAE				
		Z_L [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_L [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
746	1.72-j4.55	2.68-j0.21	20.45	52.45	176	55.0	2.14+j2.47	22.95	50.52	113	70.0
751	1.85-j4.5	2.22-j0.22	19.88	52.37	173	49.6	2.03+j3.1	23.54	49.57	91	70.6
756	1.91-j4.63	3.66-j0.89	20.24	52.30	170	53.5	2.34+j2.63	22.98	50.42	110	69.9
768	2.1-j4.9	3.49-j0.85	20.13	52.33	171	53.7	2.51+j2.47	22.64	50.64	116	69.6

Peak Side Load Pull Performance – Pulsed CW signal: 10 μs , 10% duty cycle, 48 V, $V_{GS(PEAK)} = 2.1 \text{ V}$, class C

Freq [MHz]	Z_s [Ω]	P_{1dB}									
		Max Output Power					Max PAE				
		Z_L [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Z_L [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
746	1.45-j4.42	1.91-j0.19	16.5	53.07	203	54.8	1.85+j2.73	17.60	50.22	105	71.8
751	1.51-j4.50	1.65+j0.04	16.6	53.08	203	55.3	2.18+j2.84	17.62	50.40	110	73.6
756	1.59-j4.59	2.25-j0.56	16.3	52.90	195	53.2	2.00+j2.41	17.51	50.66	116	71.1
768	1.72-j4.94	2.40-j0.76	16.2	52.99	199	53.4	1.75+j3.02	17.27	49.62	92	71.6

Reference Circuit, 746 – 768 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit Assembly

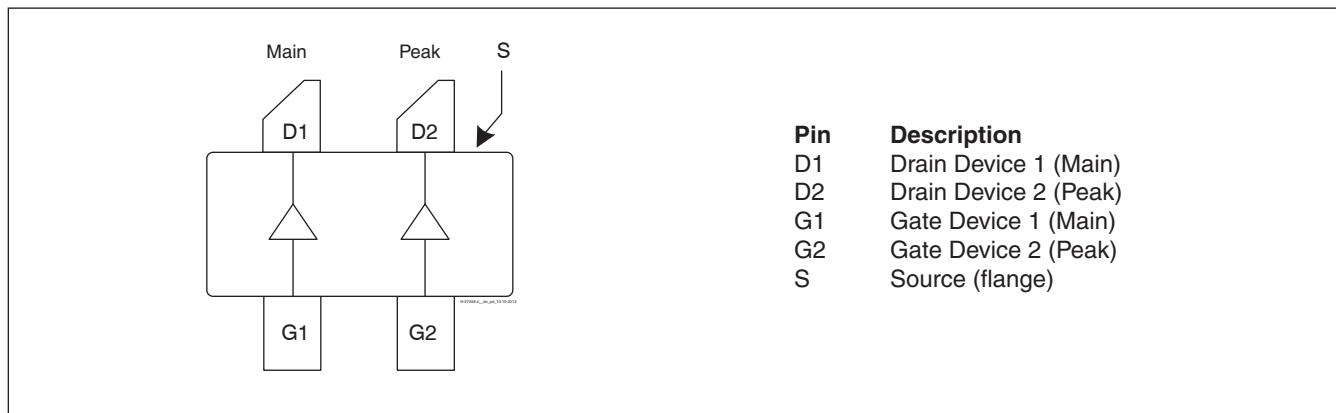
DUT	PTRA093302FC V1
Test Fixture Part No.	LTA/PTRA093302FC V1
PCB	Rogers 4360, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 6.15$, $f = 746 - 768$ MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at www.wolfspeed.com/RF	

Reference Circuit (cont.)

Components Information for circuit assembly

Component	Description	Manufacturer	P/N
Input			
C101, C102, C104	Capacitor, 6.8 pF	ATC	ATC100A6R8CW150XB
C103, C106, C107, C108	Capacitor, 68 pF	ATC	ATC100A680JW150XB
C105	Capacitor, 3.9 pF	ATC	ATC800A3R9CW250T
C109, C110	Capacitor, 10 μ F	Taiyo Yuden	UMK325C7106MM-T
R101, R102	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-3GEYJ100V
R103	Resistor, 50 Ω	Richardson	C16A50Z4
U1	Hybrid Coupler	Anaren	X3C07P1-05S
Output			
C201	Capacitor, 9.1 pF	ATC	ATC100B9R1CW500XB
C202, C209, C210	Capacitor, 6.8 pF	ATC	ATC100A6R8CW150XB
C203, C204, C212, C213	Capacitor, 68 pF	ATC	ATC100A680JW150XB
C205, C215	Capacitor, 56 pF	ATC	ATC100A560JW150XB
C206, C214	Capacitor, 470 μ F	Cornell Dubilier Electronics (CDE)	SEK471M050ST
C207, C208, C216, C217	Capacitor, 10 μ F	Taiyo Yuden	UMK325C7106MM-T
C211	Capacitor, 1.1 pF	ATC	ATC800A1R1CW250T
C218	Capacitor, 0.5 pF	ATC	ATC100A0R5CW150XB

Pinout Diagram (top view)



Lead connections for PTRA093302FC

Package Outline Specifications

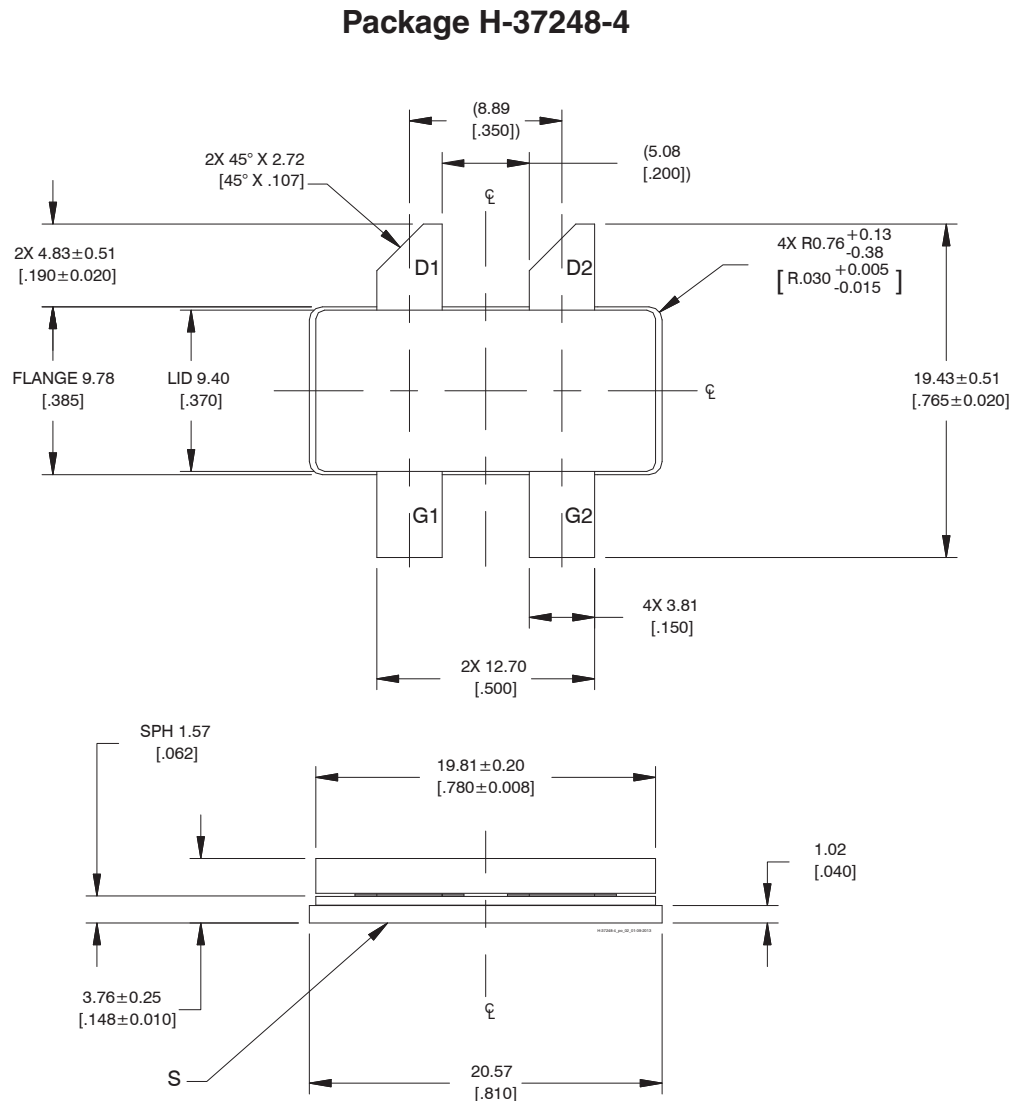


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [0.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: $0.10 + 0.076/-0.025$ mm [$0.004+0.003/-0.001$ inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2014-06-19	Advance	All	Data Sheet reflects advance specification for product development
02	2015-10-29	Preliminary	All	Data Sheet reflects preliminary specification
03	2016-03-16	Production	5-6	Add reference circuit information, firm specifications. Product released to production.
03.1	2017-01-31	Production	2	Update operating voltage and junction temperature
04	2018-06-22	Production	All	Converted to Wolfspeed Data Sheet

For more information, please contact:

4600 Silicon Drive
Durham, North Carolina, USA 27703
www.wolfspeed.com/RF

Sales Contact
RFSales@wolfspeed.com

RF Product Marketing Contact
RFMarketing@wolfspeed.com
919.407.7816

Notes

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