CMPA5259050D1

5.0 – 5.9 GHz*, 60 W GaN HPA

Description

Wolfspeed's CMPA5259050D1 is a 60W MMIC HPA utilizing Wolfspeed's high performance, 0.15um GaN on SiC production process. The CMPA5259050D1 operates from 5.0-5.9 GHz and supports both defense and commercial-related radar applications. The CMPA5259050D1 achieves 60 W of saturated output power with 23 dB of large signal gain and typically 50% power-added efficiency under pulsed operation. CW operation is also an option.

The CMPA5259050D1 provides improved RF performance over previous generations allowing customers to improve SWaP-C benchmarks in their next-generation systems.

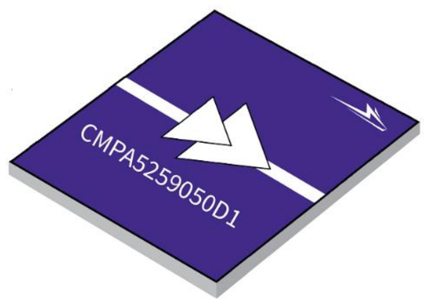


Figure 1. CMPA5259050D1

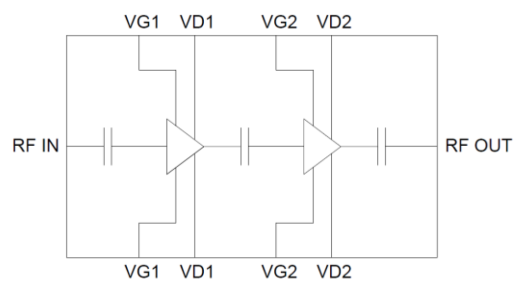


Figure 2. Functional Block Diagram

Features

- Psat: 60 W
- PAE: 50 %
- LSG: 23 dB
- S21: 30 dB
- S11: -10 dB
- S22: -10 dB
- Pulsed / CW operation

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional information.

*Production screening from 5.2-5.9 GHz

Applications

- Military and Commercial Radar

RoHS COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain to Source Voltage	V_{DSS}	V	84	25 °C
Drain Voltage	V_D	V	28	
Gate Voltage	V_G	V	-10, +2	
Drain Current	I_D	A	4.5	
Gate Current	I_G	mA	19	
Input Power	P_{in}	dBm	28	
Dissipated Power	P_{diss}	W	80	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	320	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	5:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	28	
Gate Voltage	Vg	V	-1.8	
Drain Current	Idq	mA	500	
Input Power	Pin	dBm	25	
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		5.2		5.9	
Output Power	dBm	5.2		48.5		
		5.55		48.5		
		5.9		48.0		
Power-added Efficiency	%	5.2		53		
		5.55		53		
		5.9		50		
LSG	dB	5.2		23.5		
		5.55		23.5		
		5.9		23.0		
Small-Signal Gain (S21)	dB	5.2		30		Pin = -20 dBm
		5.55		30		
		5.9		30		
Input Return Loss	dB			-10		Pin = -20 dBm
Output Return Loss	dB			-10		Pin = -20 dBm

Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 3: Pout v. Frequency v. Temperature

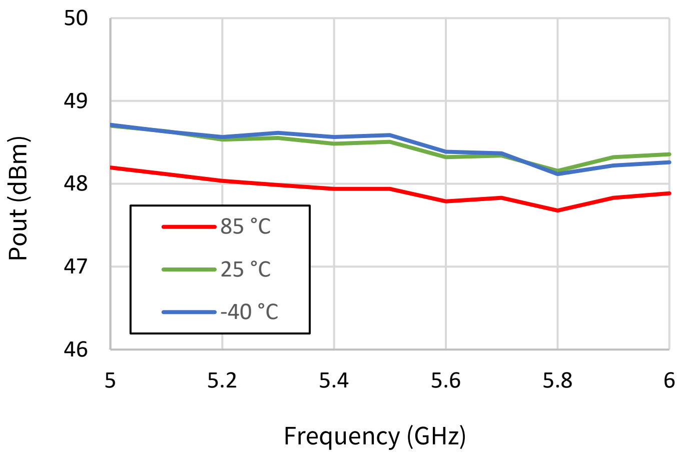


Figure 4: PAE v. Frequency v. Temperature

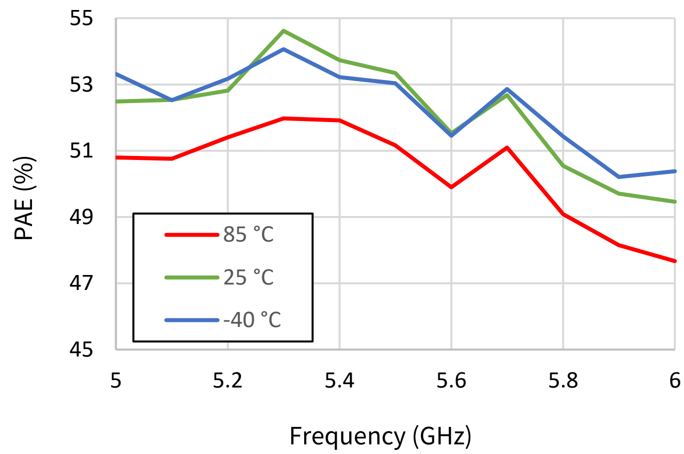


Figure 5: Id v. Frequency v. Temperature

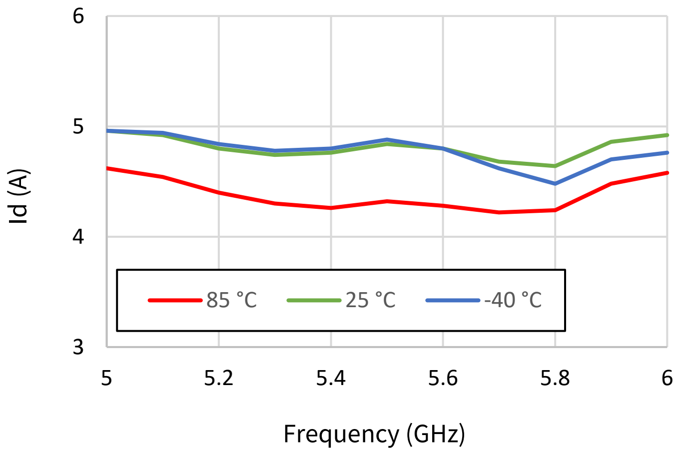


Figure 6: Ig v. Frequency v. Temperature

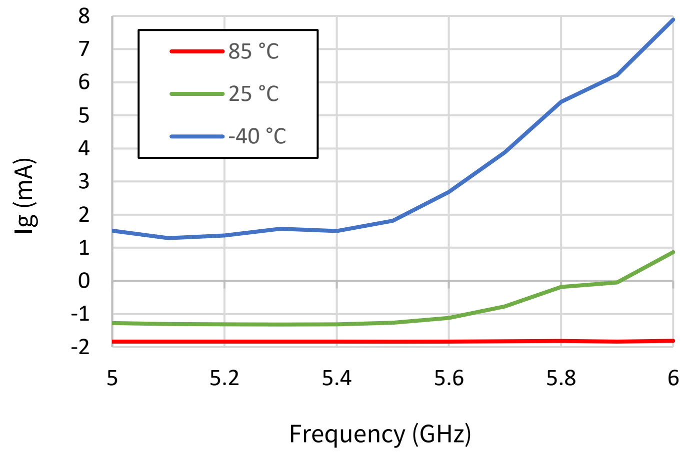
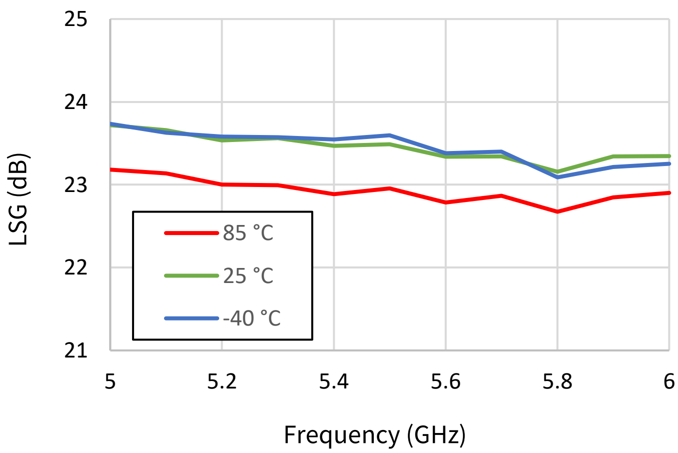


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 8: Pout v. Frequency v. Vd

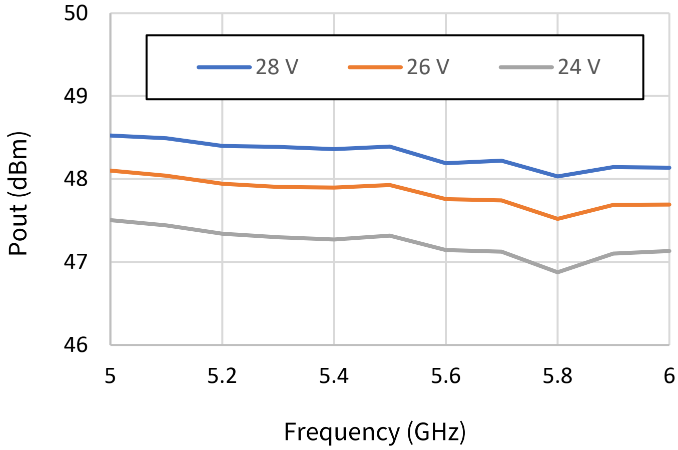


Figure 9: PAE v. Frequency v. Vd

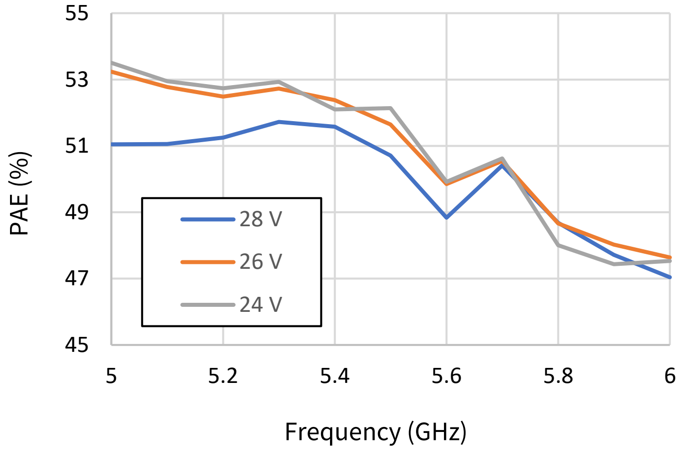


Figure 10: Id v. Frequency v. Vd

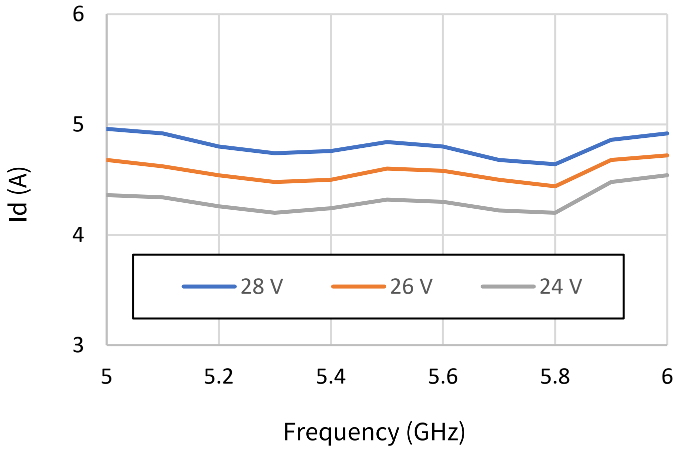


Figure 11: Ig v. Frequency v. Vd

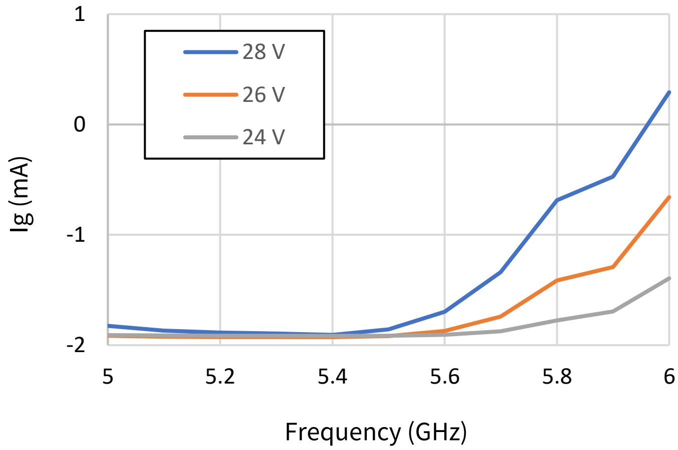
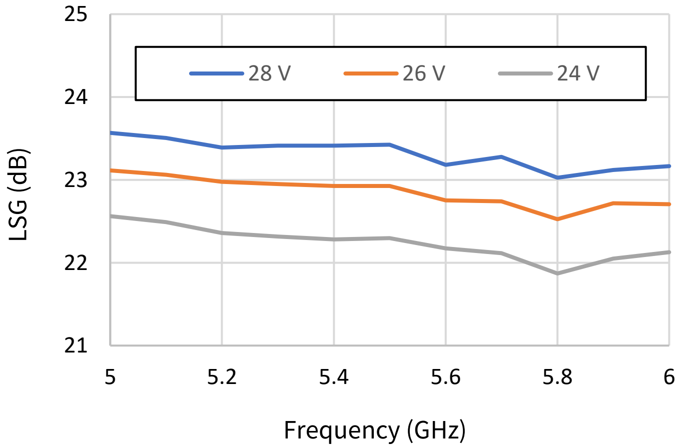


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 13: Pout v. Frequency v. Idq

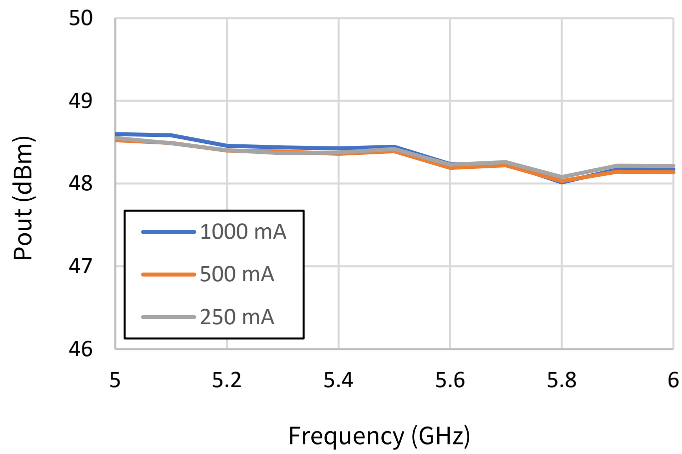


Figure 14: PAE v. Frequency v. Idq

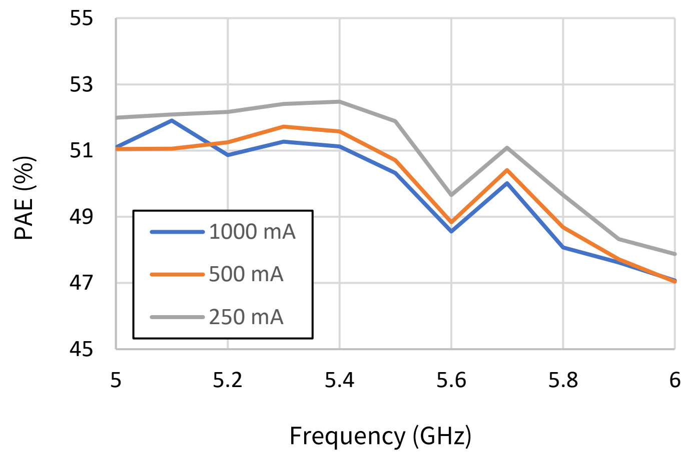


Figure 15: Id v. Frequency v. Idq

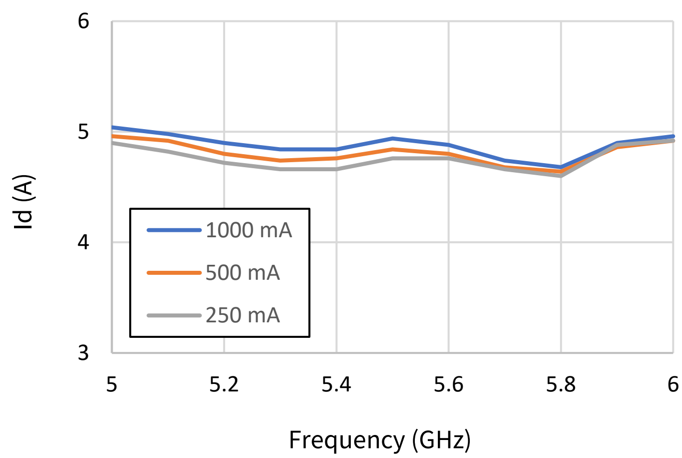


Figure 16: Ig v. Frequency v. Idq

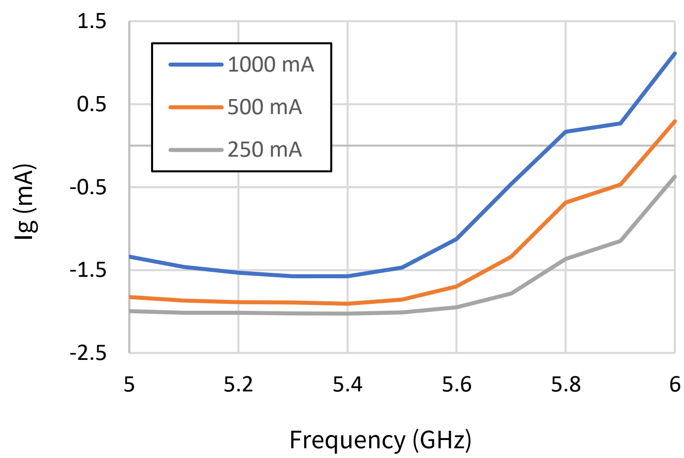
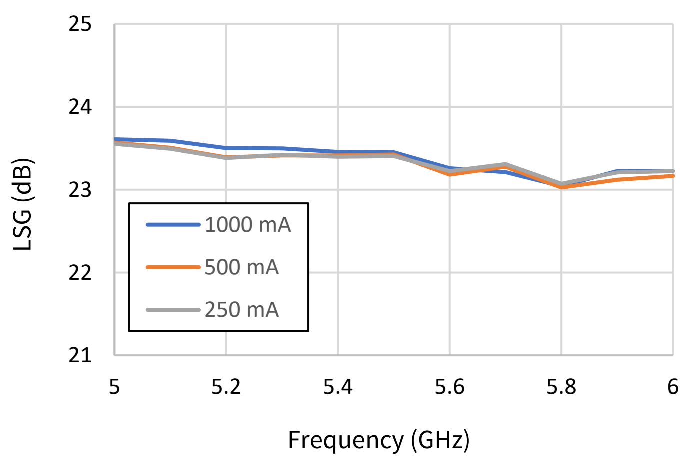


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 18: Pout v. Pin v. Frequency

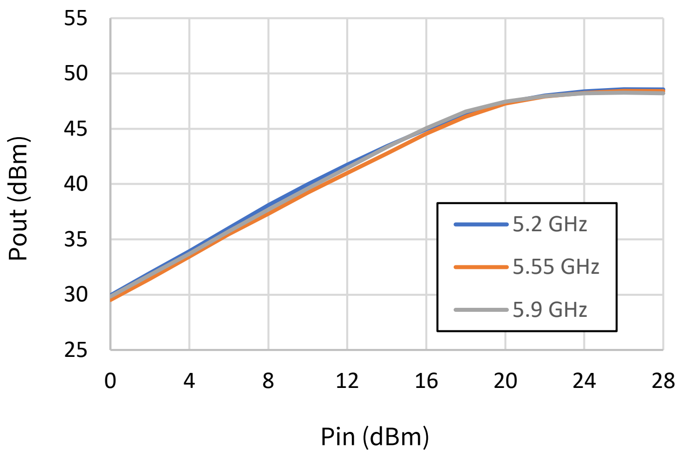


Figure 19: PAE v. Pin v. Frequency

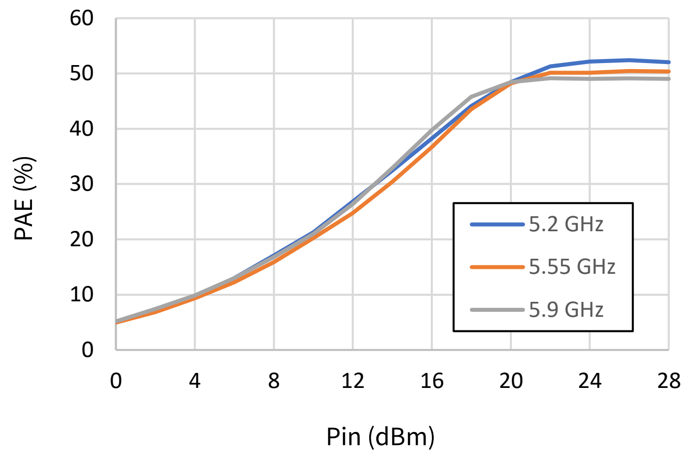


Figure 20: Id v. Pin v. Frequency

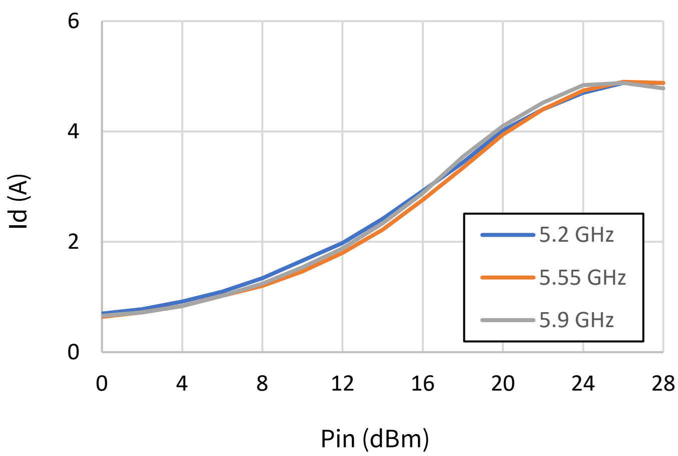


Figure 21: Ig v. Pin v. Frequency

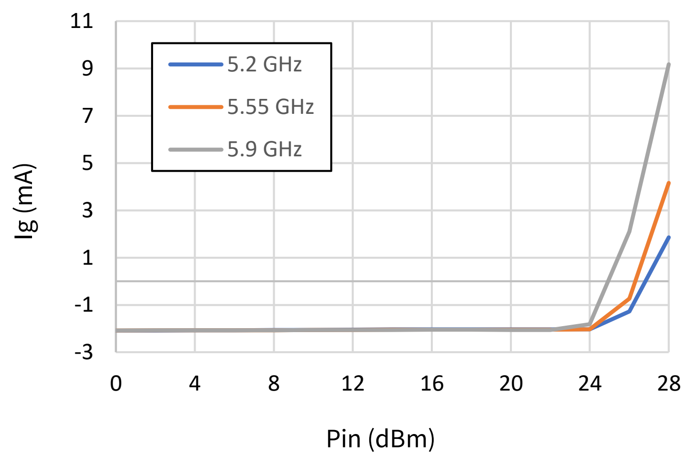
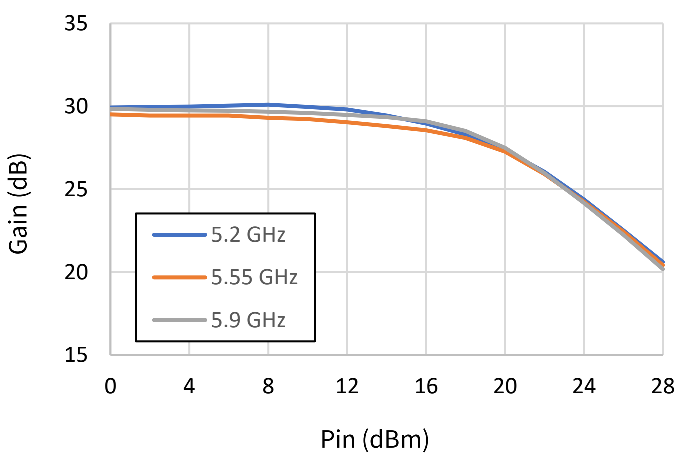


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 23: Pout v. Pin v. Temperature

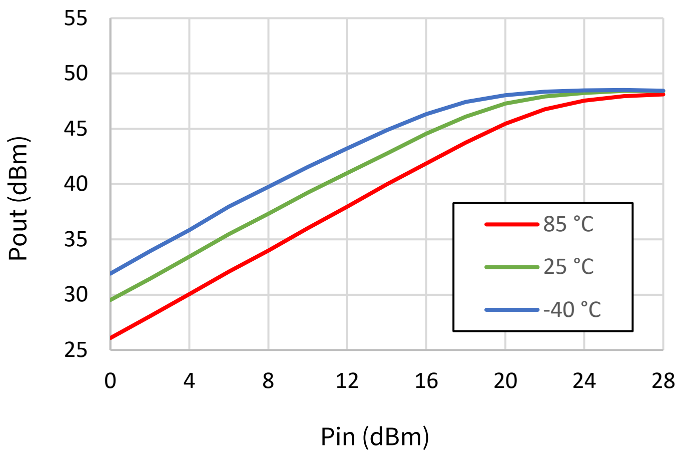


Figure 24: PAE v. Pin v. Temperature

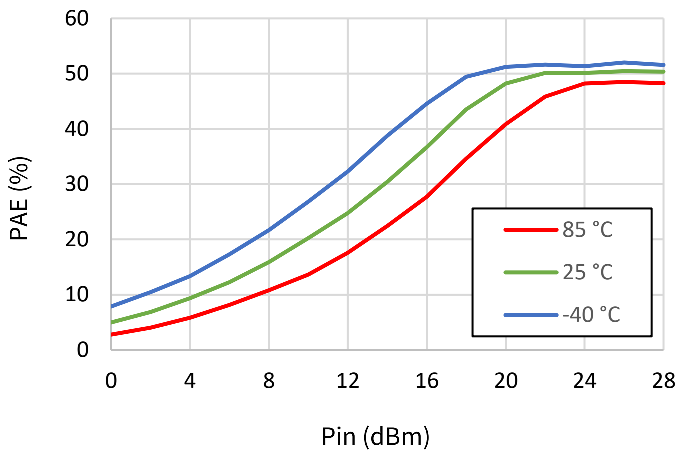


Figure 25: Id v. Pin v. Temperature

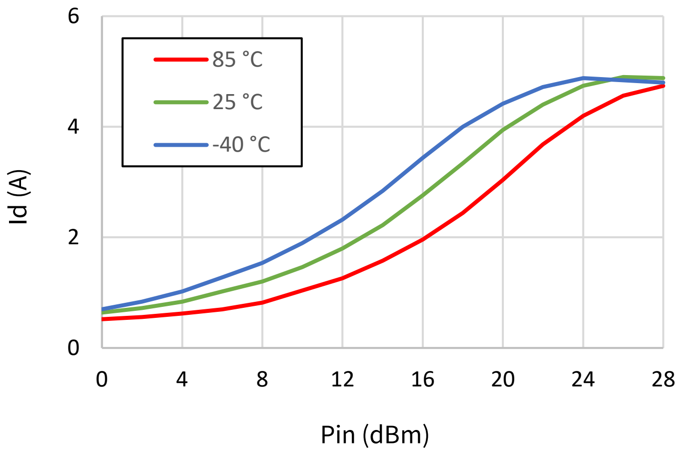


Figure 26: Ig v. Pin v. Temperature

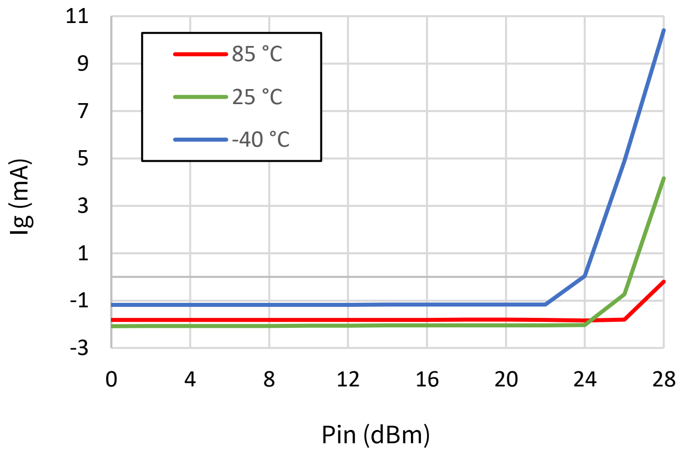
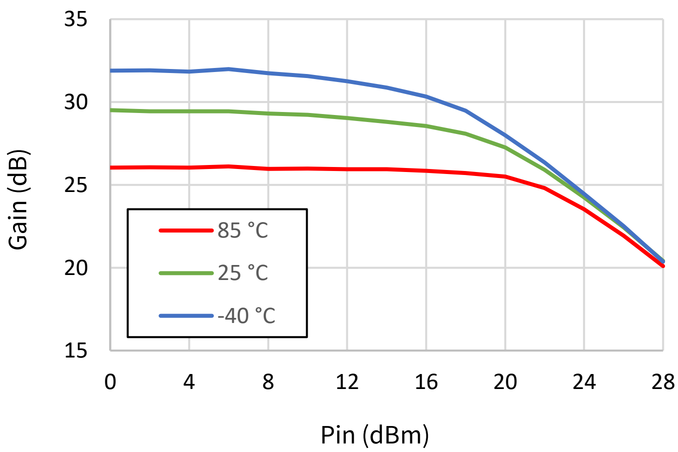


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 28: Pout v. Pin v. Vd

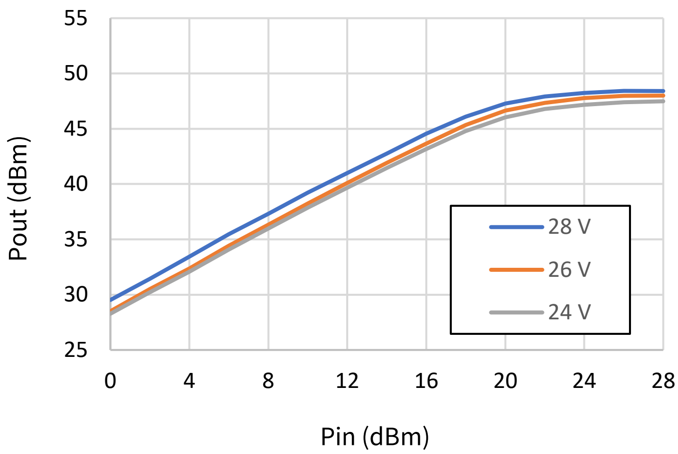


Figure 29: PAE v. Pin v. Vd

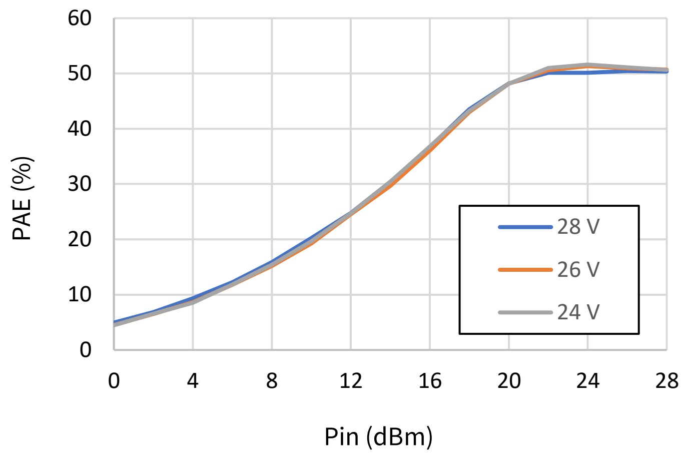


Figure 30: Id v. Pin v. Vd

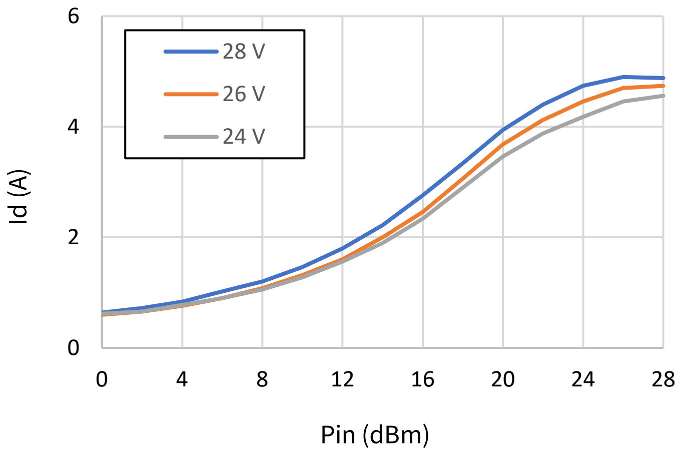


Figure 31: Ig v. Pin v. Vd

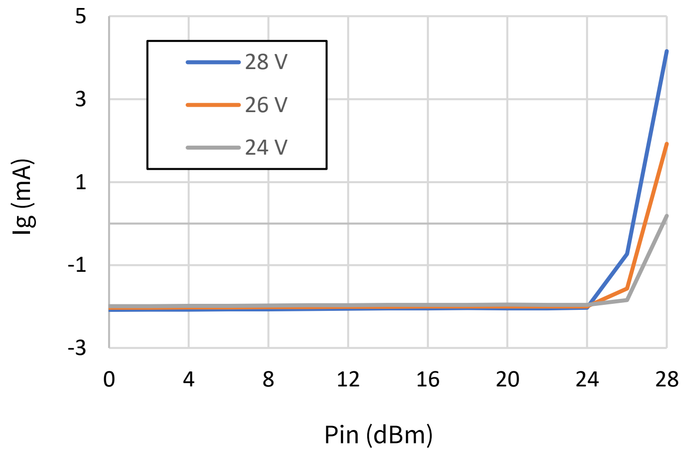
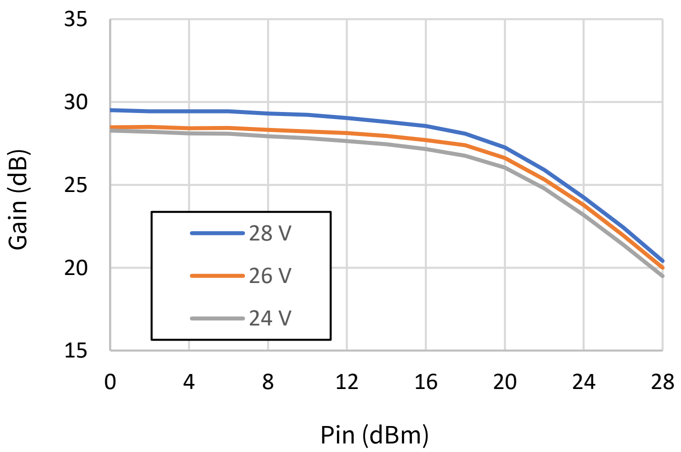


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 33: Pout v. Pin v. Idq

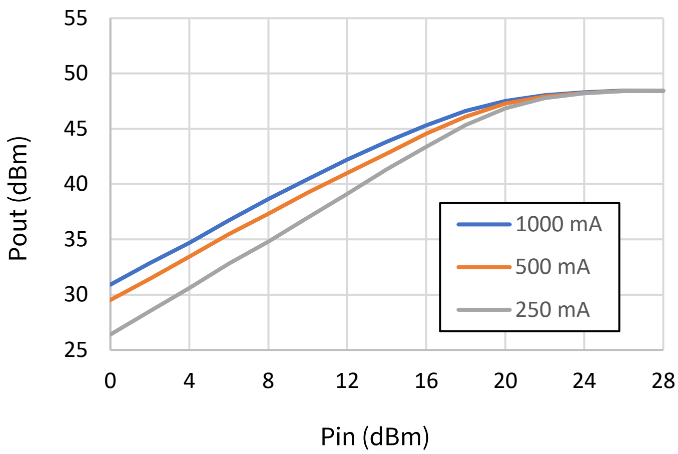


Figure 34: PAE v. Pin v. Idq

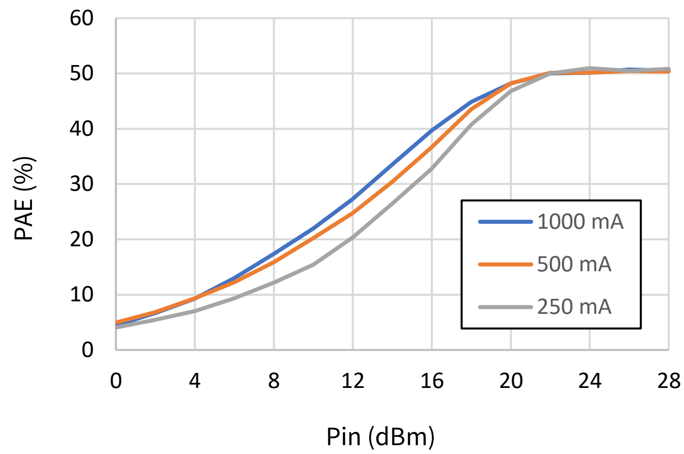


Figure 35: Id v. Pin v. Idq

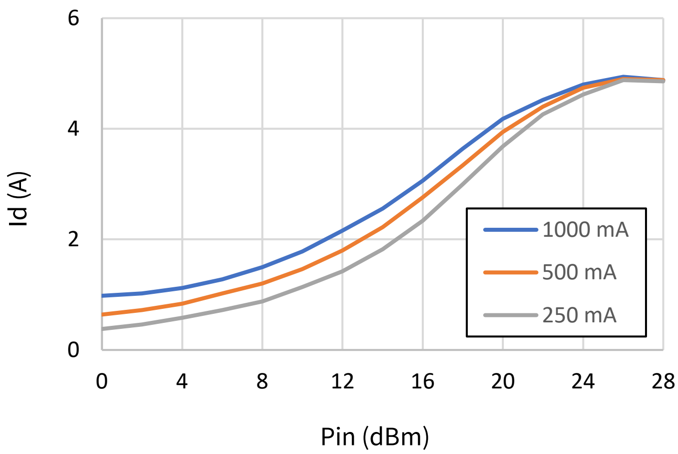


Figure 36: Ig v. Pin v. Idq

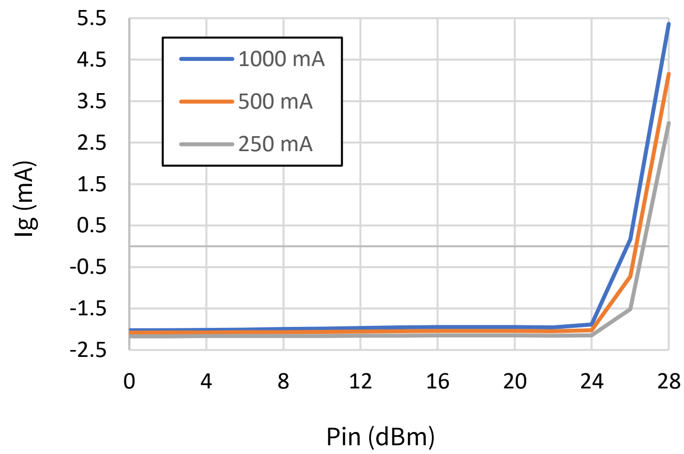
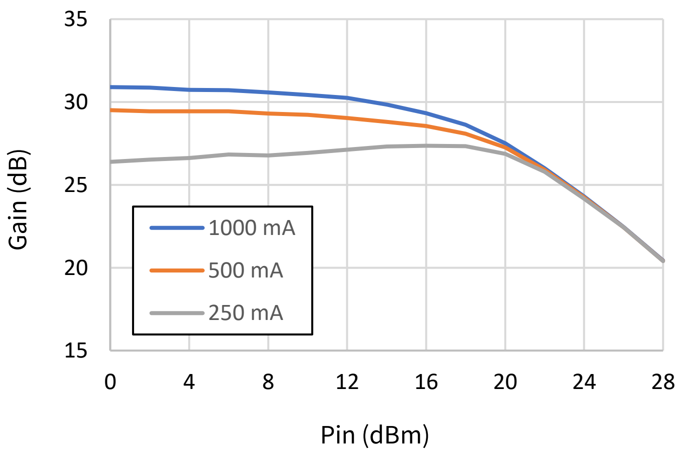


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 38: S21 v. Frequency v. Temperature

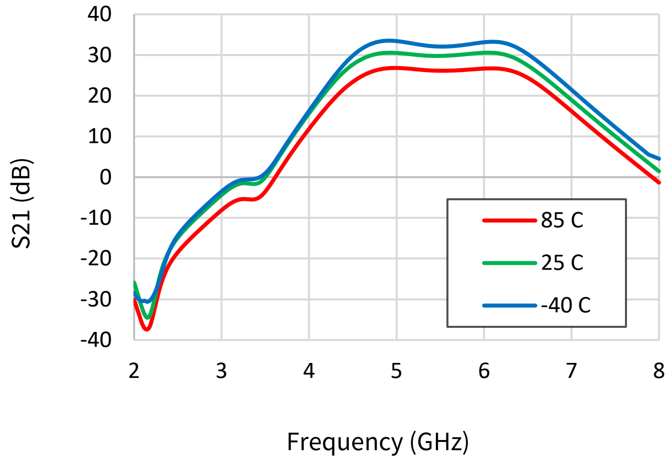


Figure 39: S21 v. Frequency v. Vd

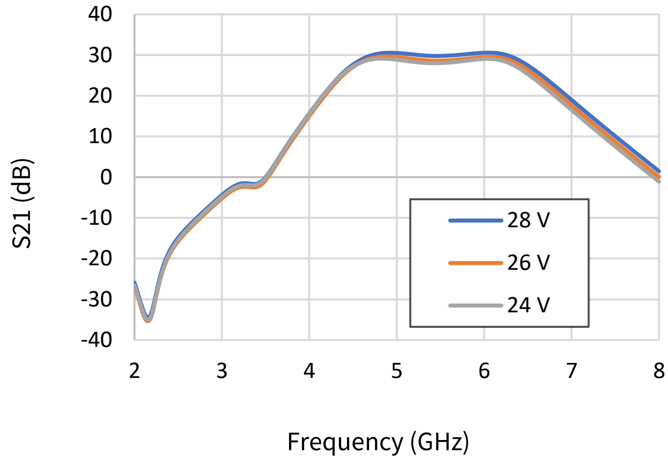


Figure 40: S11 v. Frequency v. Temperature

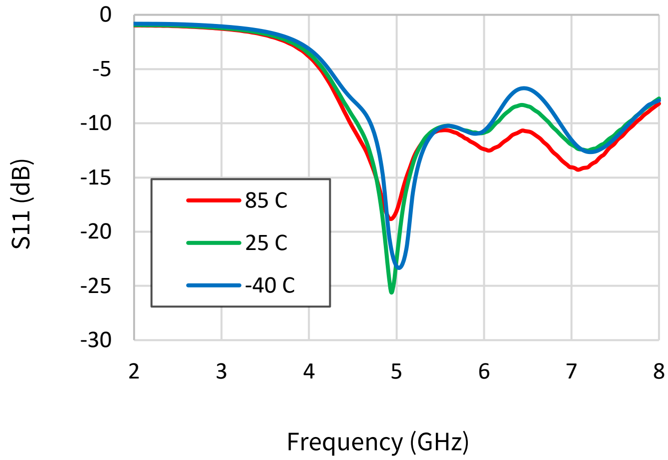


Figure 41: S11 v. Frequency v. Vd

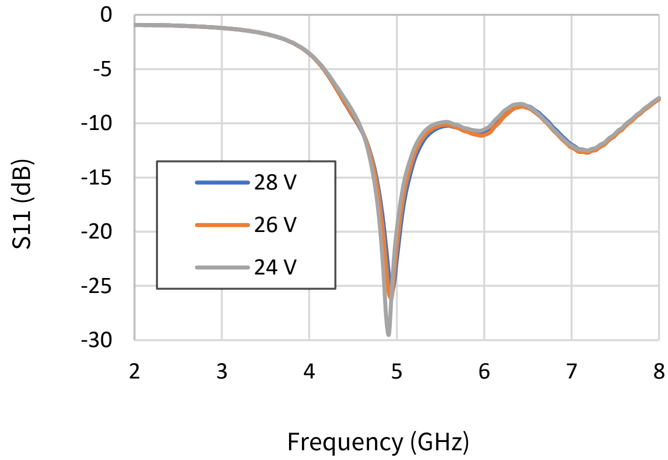


Figure 42: S22 v. Frequency v. Temperature

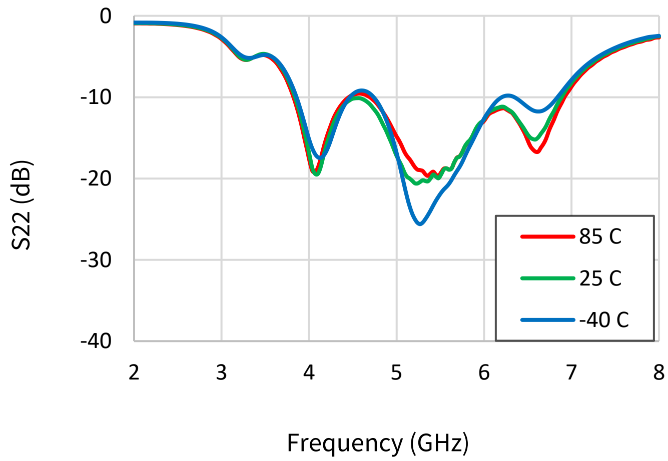
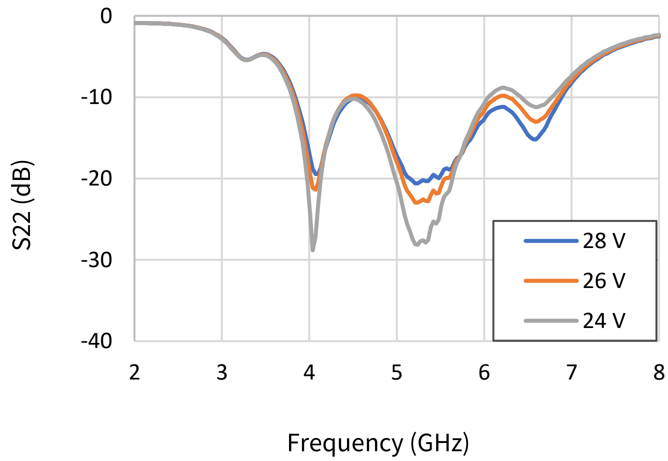


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 44: S21 v. Frequency v. Idq

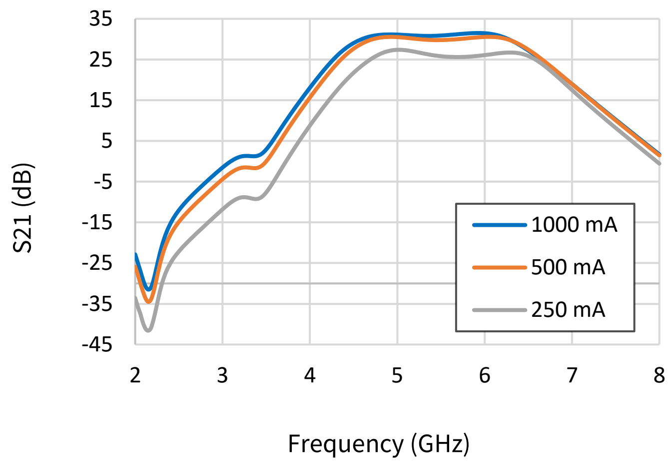


Figure 45: S11 v. Frequency v. Idq

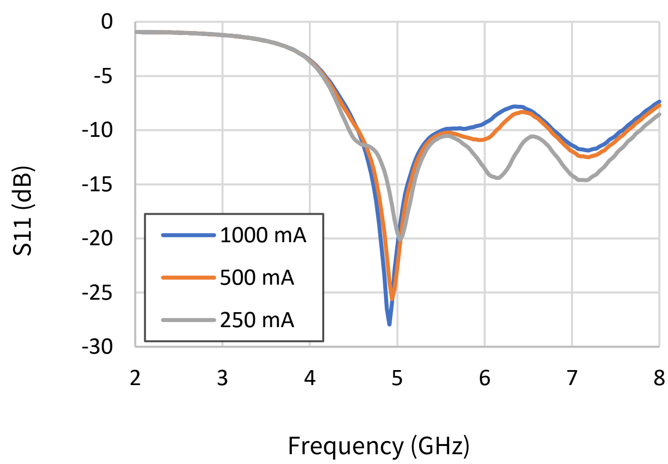
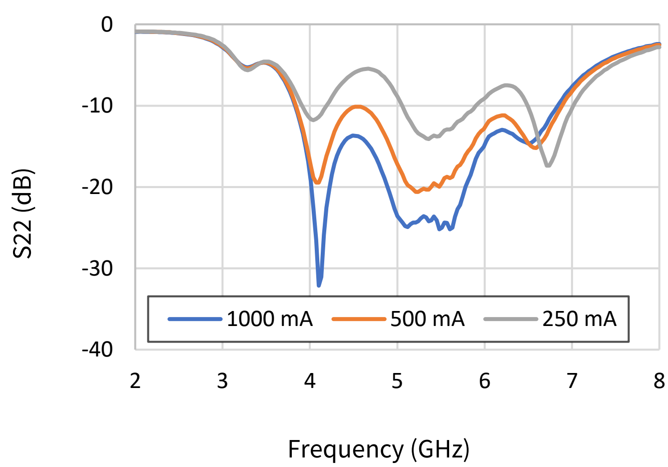


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28 V, Idq=500mA, PW=150uS, DC=20%, Pin = 25 dBm, T_{base}=25 °C, Frequency: 5.55GHz

Figure 47: 2f v. Pout v. Temperature, F1

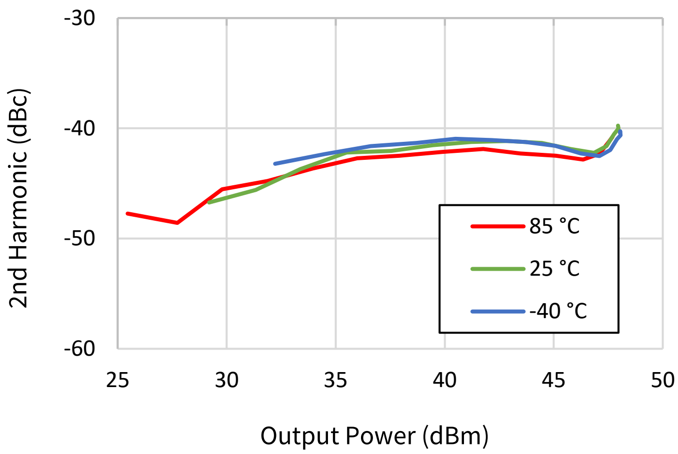


Figure 48: 2f v. Pout v. Vd, F1

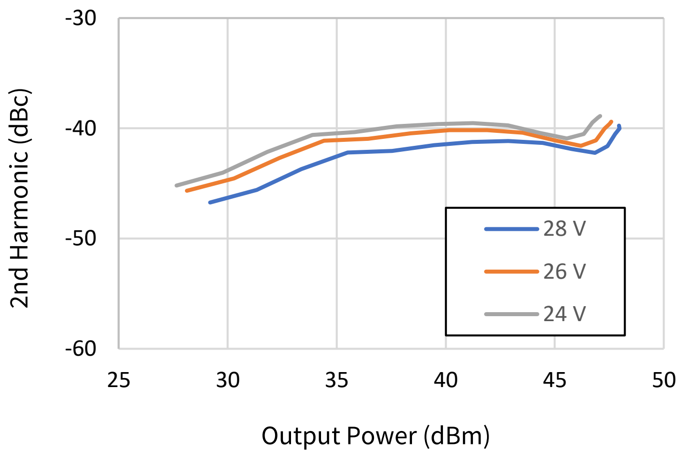


Figure 49: 2f v. Pout v. Temperature, F2

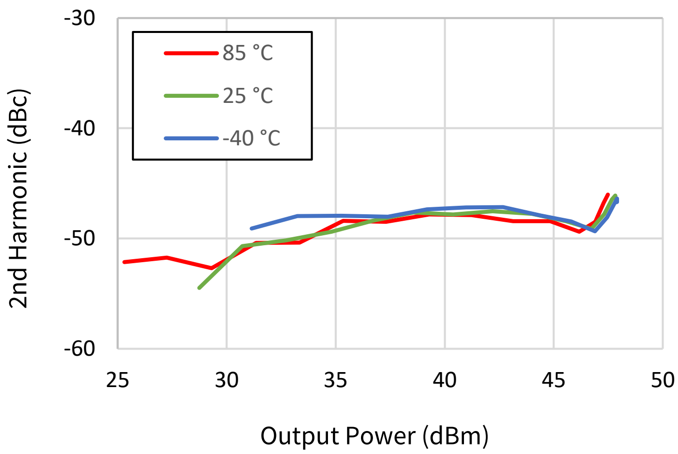


Figure 50: 2f v. Pout v. Vd, F2

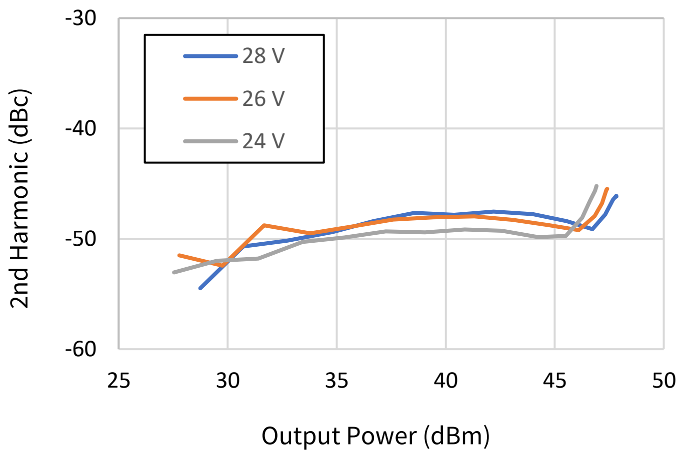


Figure 51: 2f v. Pout v. Temperature, F3

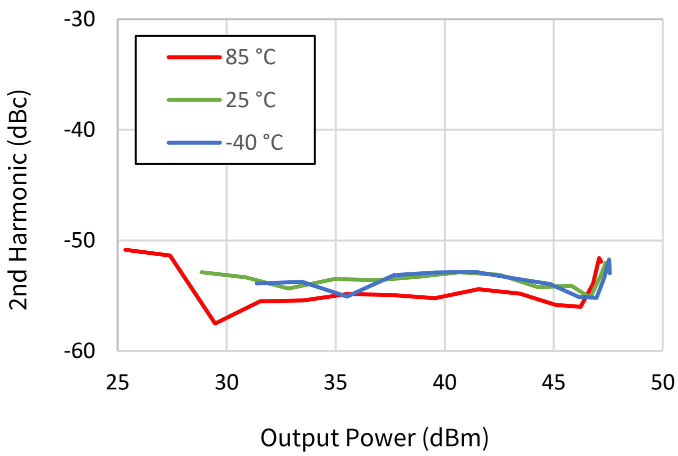
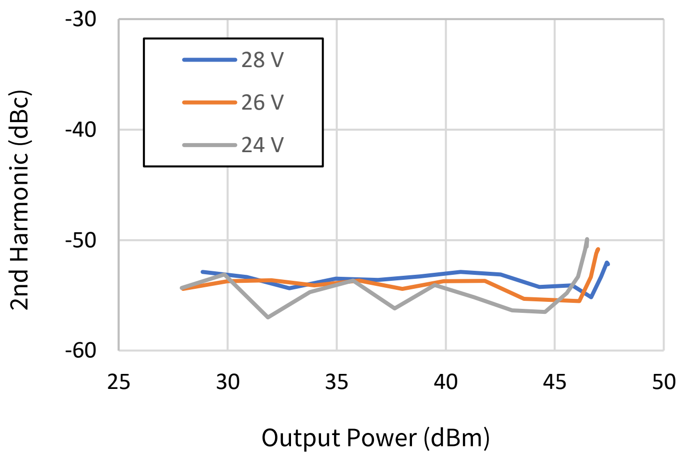


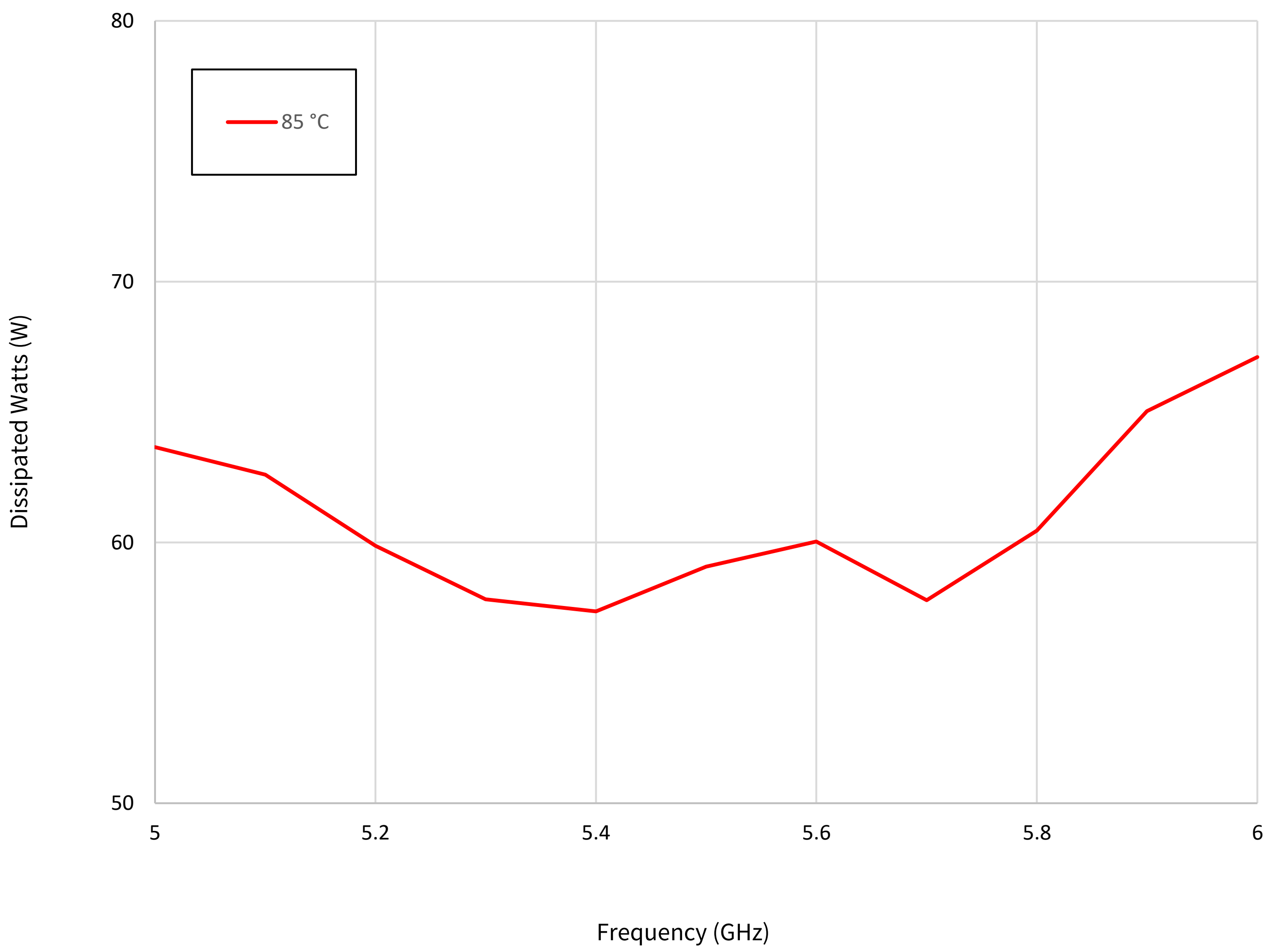
Figure 52: 2f v. Pout v. Vd, F3



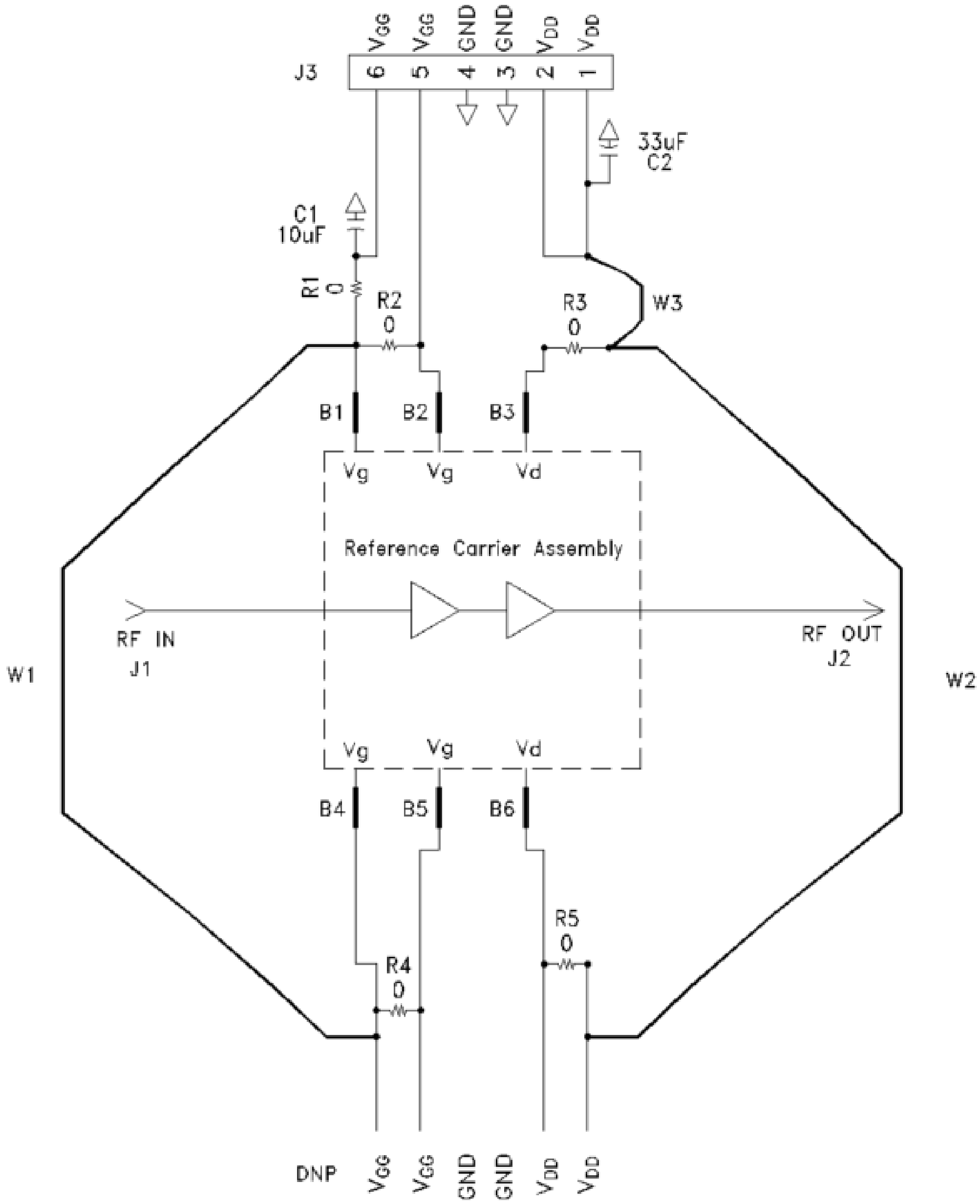
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	141.15°C	Freq = 5.5 GHz, V_d = 28 V, I_{dq} = 500 mA, I_{drive} = 4.32 A , P_{in}= 25 dBm, P_{out} = 47.94 dBm, P_{diss}= 59.1W, T_{case}=85°C, PW=150uS, DC=20%
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.95°C/W	

Power Dissipation v. Frequency (Tcase = 85°C)



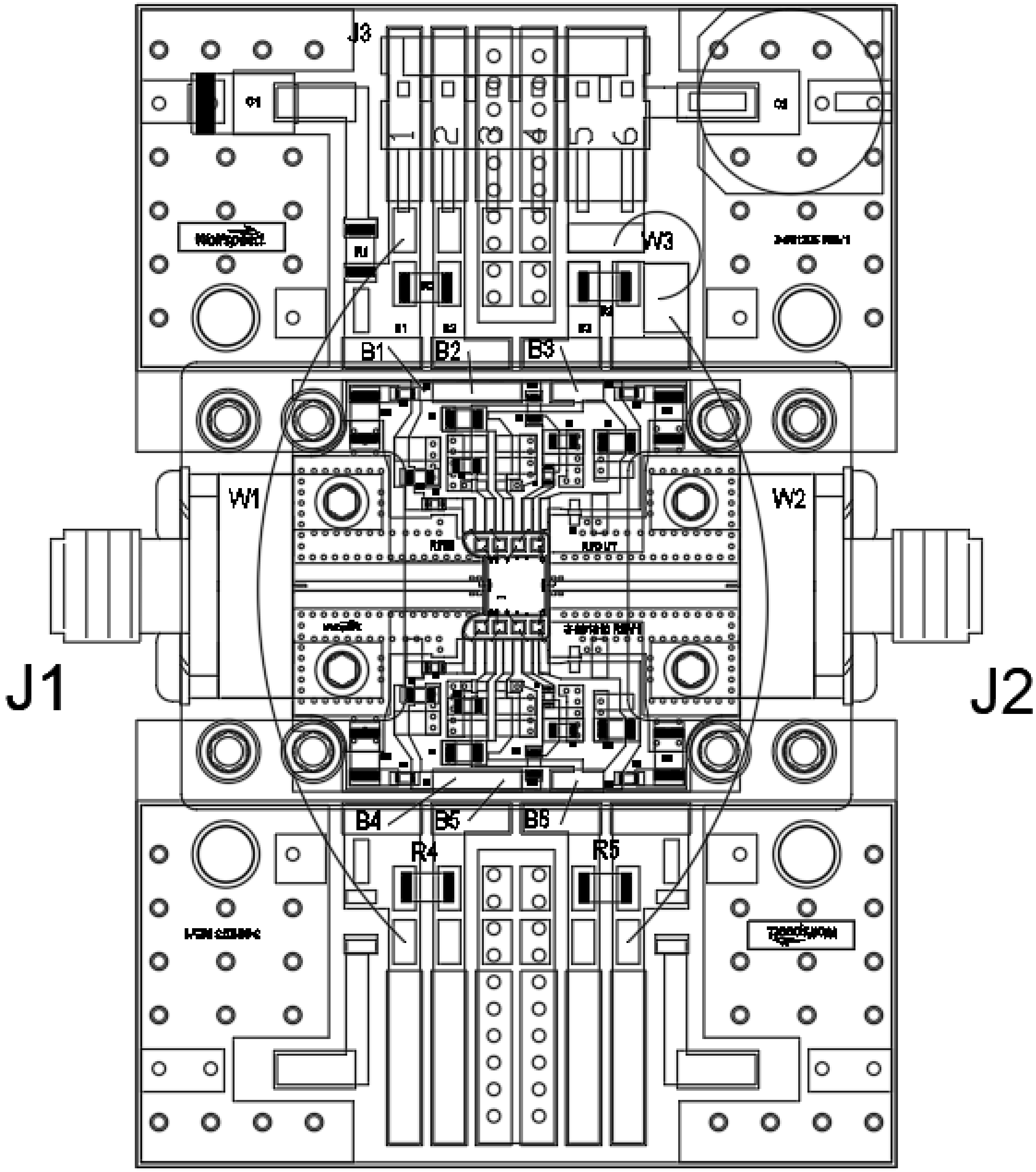
CMPA5259050D1-AMP Evaluation Board Schematic Drawing



CMPA5259050D1-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
J1, J2	CONNECTOR SMA JACK (FEMALE) END LAUNCH	2
J3	6-PIN DC HEADER, RIGHT ANGLE	1
R1-R5	RESISTOR, 0 OHMS, 1206	5
C1	CAPACITOR, 10UF, TANTALUM	1
C2	CAPACITOR, 33UF, ELECTROLYTIC	1
B1-B6	JUMPER WIRE	6
W1-W3	WIRE, BLACK, 22AWG (~2”)	3

CMPA5259050D1-AMP Evaluation Board Assembly Drawing



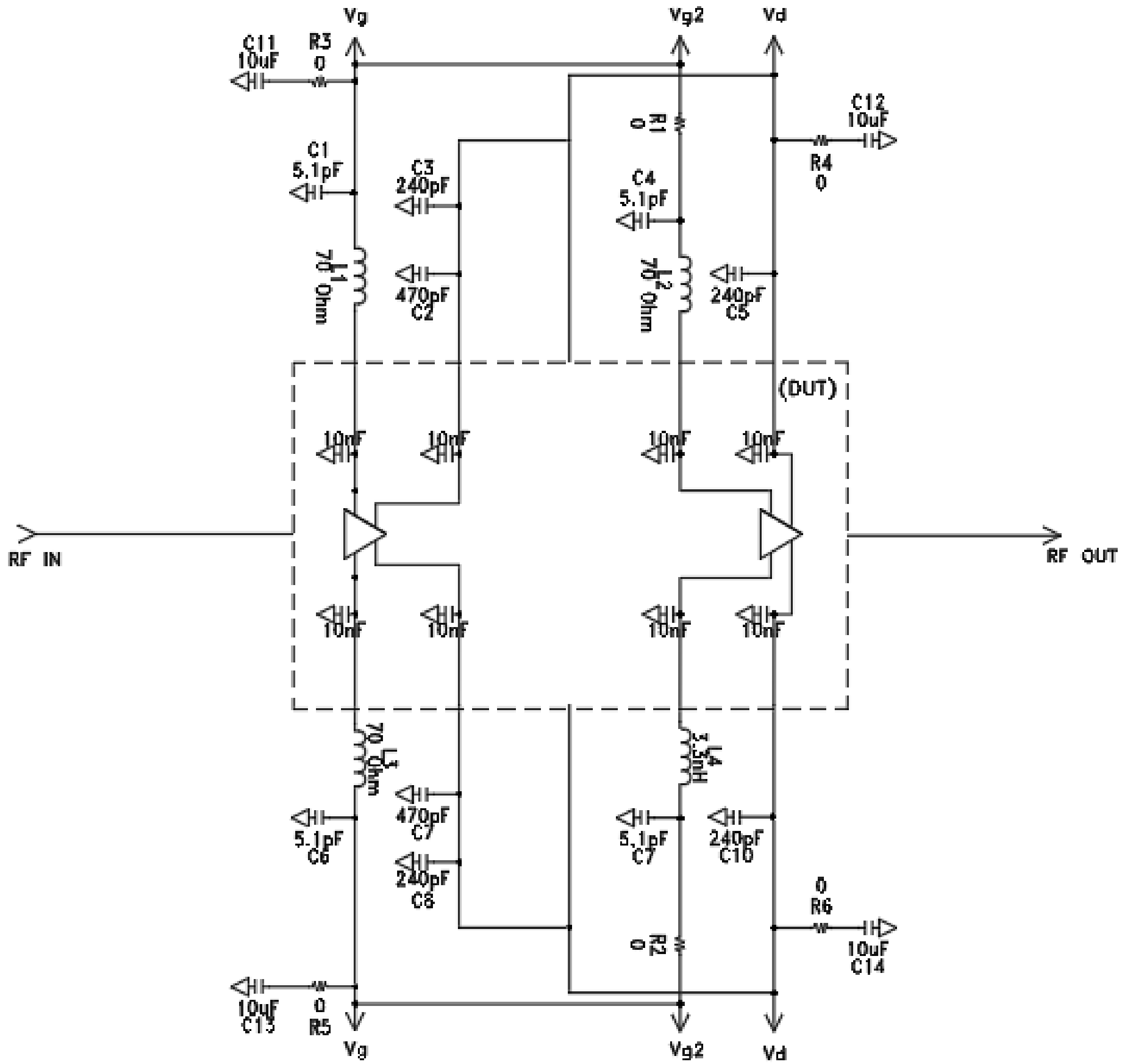
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

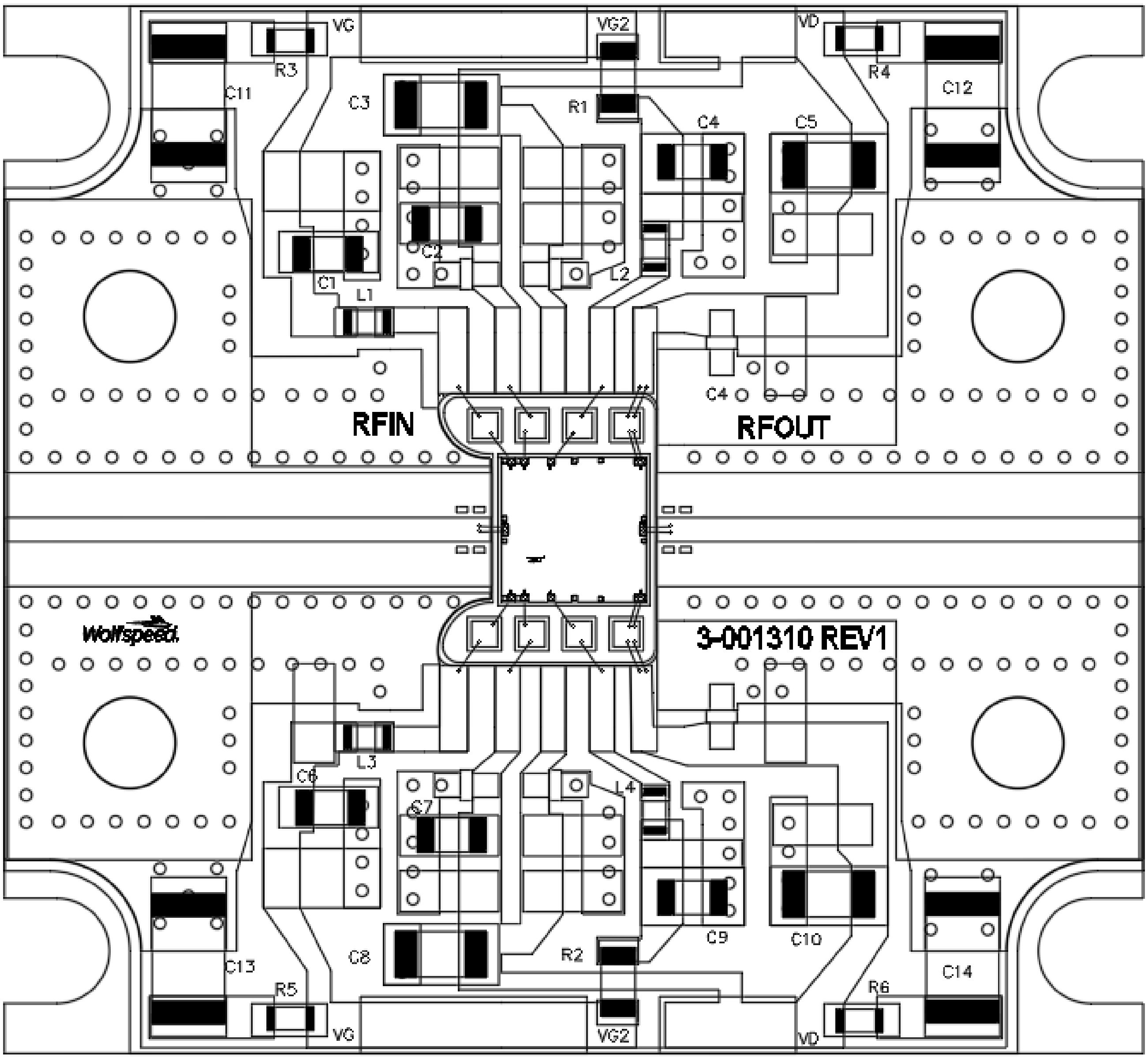
CMPA5259050D1-AMP Carrier Schematic Drawing



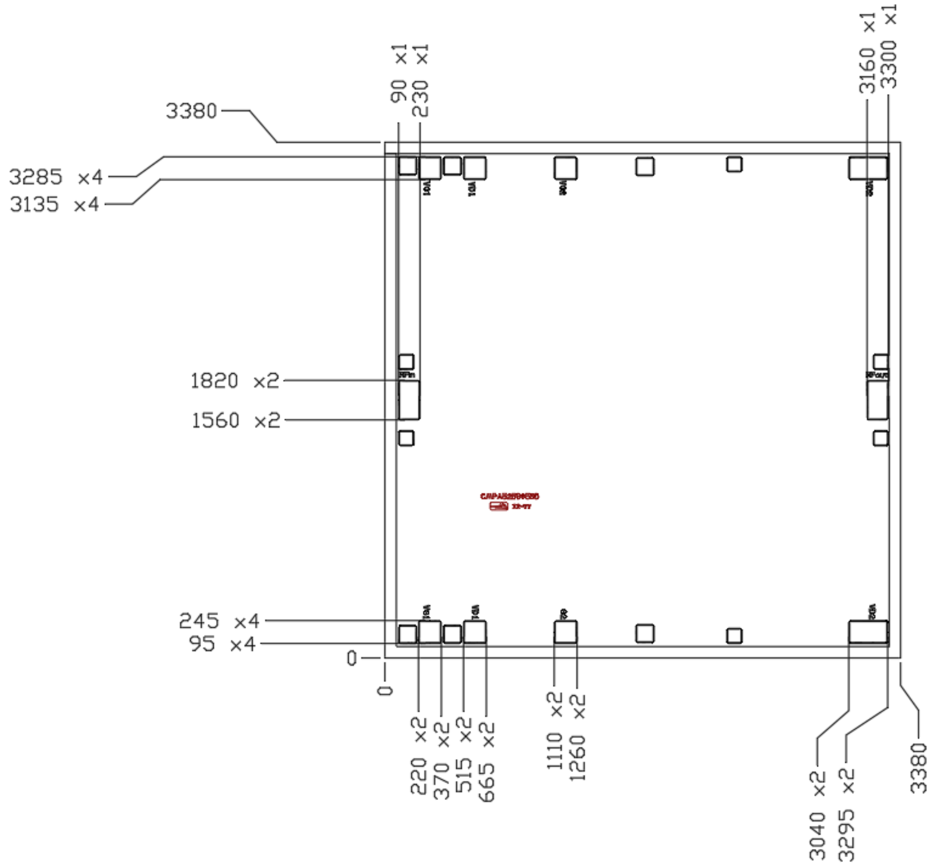
CMPA5259050D1-AMP Carrier Bill of Materials

Reference Designator	Description	Qty
R1 – R2	RESISTOR, 0603, 0 Ohms	2
R3 – R6	RESISTOR, 0402, 0 Ohms	4
C1,C4,C6,C9	CAPACITOR, 5.1 pF, +/-0.5%, 0603	4
C2,C7	CAP, 0603, 100V, NPO/COG material, 470pF +/- 5%	2
C3,C5,C8,C10	CAPACITOR, 240 pF, +/-5%, 0805	4
C11-C14	CAPACITOR, 1uF, +/-15%, 100V, 1206, X7R	4
L1,L3	FERRITE, 70ohm at 100MHz, 0.1ohm at DC, 0402	2
L2,L4	INDUCTOR, 3.3nH, ROHS, 0402, 5%	2

CMPA5259050D1-AMP Carrier Assembly Drawing



Product Dimensions



Overall die size is 3380 x 3380 (+/-50) microns. Die thickness 100 (+/-10) microns.
All Gate and Drain pads must be wire bonded for electrical connection.

Function	Description	Pad Size (um)	Note
RF IN	RF Input pad. Matched to 50 ohm.	140 x 260	6
VG1 (top and bottom)	Gate control for stage 1	150 x 150	1,2
VG2 (top and bottom)	Gate control for stage 2	150 x 150	1,3
VD1 (top and bottom)	Drain Supply for stage 1	150 x 150	1,4
VD2 (top and bottom)	Drain Supply for stage 2	150 x 255	1,5
RF OUT	RF Output pad. Matched to 50 ohms.	140 x 260	6

Notes

[1] Attach bypass capacitor to pads per application circuit.

[2] All VG1 pads are connected internally so it would be enough to connect any one for proper operation.

[3] All VG2 pads are connected internally so it would be enough to connect any one for proper operation.

[4] Both VD1 pads are connected internally so it would be enough to connect any one for proper operation.

[5] Both VD2 pads are connected internally so it would be enough to connect any one for proper operation.

[6] The RF Input and Output pad have a ground-signal-ground with a nominal pitch of 250 um. The RF ground pads are 100 x 100 microns.

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Classification Level	Test Methodology
Human body Model	HBM	TBD	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

Product Ordering Information

Part Number	Description	MOQ Increment	Image
CMPA5259050D1	5.0 – 5.9 GHz, 60W GaN MMIC		
CMPA5259050D1-AMP	Evaluation Board w/ PA	1 Each	

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