ESP32-H2

Datasheet

Bluetooth® Low Energy and IEEE 802.15.4 SoC

(supporting Bluetooth 5 (LE), Bluetooth Mesh, Thread, Matter and Zigbee)

Including:

ESP32-H2FH2 (2 MB In-Package Flash)

ESP32-H2FH4 (4 MB In-Package Flash)

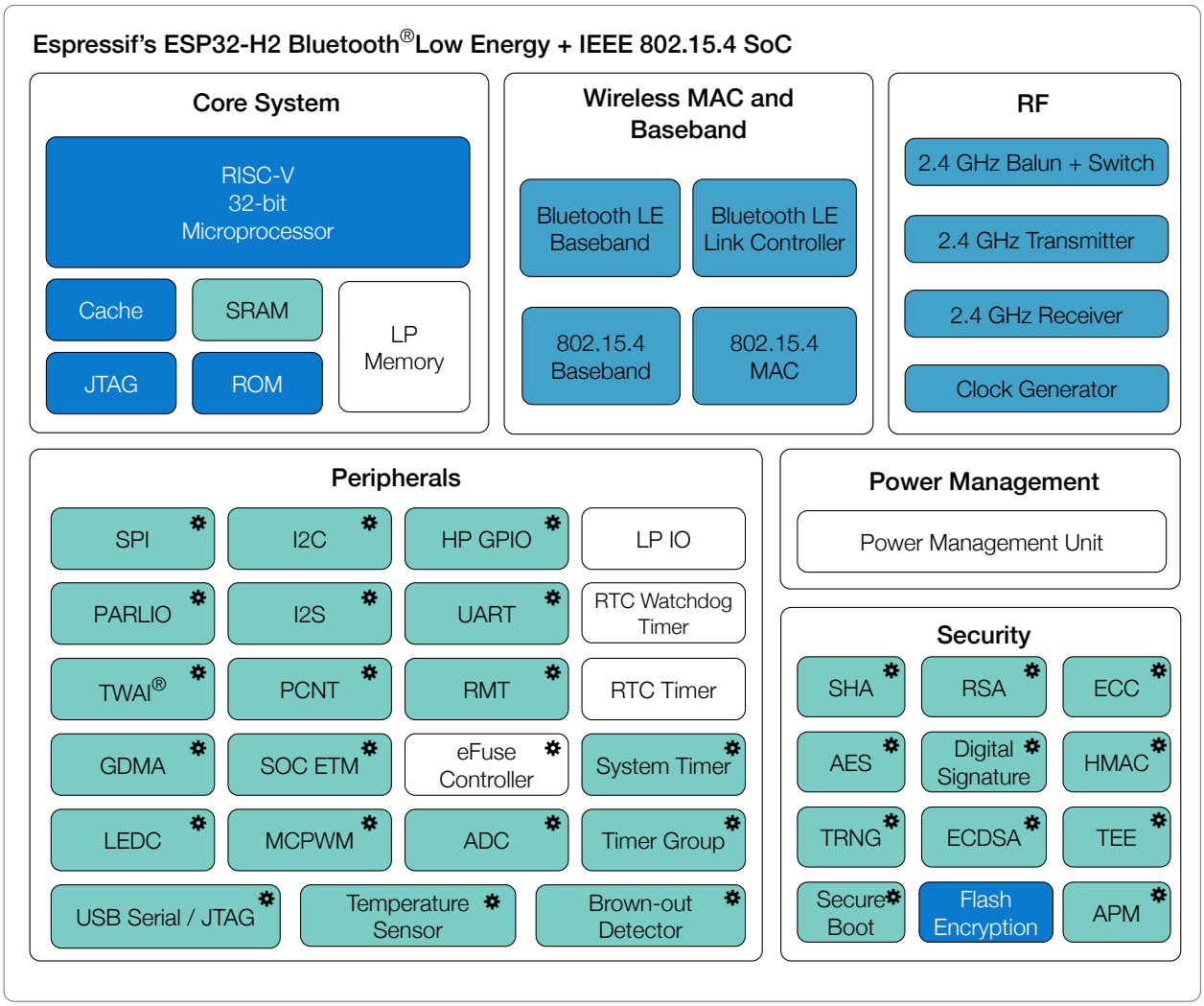
Pre-release v0.7
Espressif Systems

Product Overview

ESP32-H2 is an ultra-low-power Internet of Things (IoT) solution offering multiple protocol support on a single chip. It integrates a 2.4 GHz transceiver compliant with Bluetooth ® Low Energy and IEEE 802.15.4-based technologies, supporting Bluetooth 5 (LE), Bluetooth mesh, Thread, Matter, and Zigbee. It has:

- A Bluetooth LE subsystem that supports features of Bluetooth 5 and Bluetooth mesh
- An IEEE 802.15.4 subsystem that supports Thread and Zigbee
- Radio protocols coexistence in 2.4 GHz band
- State-of-the-art power and RF performance
- 32-bit RISC-V single-core processor with a four-stage pipeline that operates at up to 96 MHz
- 320 KB of SRAM, 128 KB of ROM, 4 KB LP memory, and 2 MB or 4 MB in-package flash inside
- Reliable security features ensured by
  - Cryptographic hardware accelerators that support AES-128/256, Hash, RSA, HMAC, ECC, digital signature and secure boot
  - Random number generator
  - Permission control on accessing internal memory, external memory, and peripherals
  - External memory encryption and decryption
- Rich set of peripheral interfaces and GPIOs, ideal for various scenarios and complex applications

Block Diagram



Block Diagram of ESP32-H2

Features

Bluetooth

- Bluetooth Low Energy (Bluetooth 5.3 certified)
- Bluetooth mesh
- Bluetooth Low Energy long range (Coded PHY, 125 Kbps and 500 Kbps)
- Bluetooth Low Energy high speed (2 Mbps)
- Bluetooth Low Energy advertising extensions and multiple advertising sets
- Simultaneous Broadcaster, Observer, Peripheral and Central
- Multiple connections
- LE power control

IEEE 802.15.4

- IEEE Standard 802.15.4-2015 compliant
- Supports 250 Kbps data rate in 2.4 GHz band and OQPSK PHY
- Supports Thread 1.3
- Supports Zigbee 3.0
- Supports Matter
- Supports other application-layer protocols (HomeKit, MQTT, etc)

CPU and Memory

- 32-bit RISC-V single-core processor, up to 96 MHz
- 128 KB ROM
- 320 KB SRAM
- 4 KB LP Memory
- 2 MB or 4 MB in-package flash

Advanced Peripheral Interfaces

- 19 × programmable GPIOs
- Digital interfaces:
  - 3 × SPI
  - 2 × UART
  - 2 × I2C
  - 1 × I2S
  - Remote control peripheral, with 2 transmit channels and 2 receive channels
  - LED PWM controller, with up to 6 channels
  - Motor control PWM (MCPWM)
  - Pulse count controller (PCNT)
  - 1 × TWAI® controller compatible with ISO 11898-1 (CAN Specification 2.0)
  - Full-speed USB Serial/JTAG controller
  - General DMA controller (GDMA), with 3 transmit channels and 3 receive channels
  - SoC event task matrix (ETM)
  - Parallel IO (PARLIO) controller
- Analog interfaces:
  - 1 × 12-bit SAR ADC, up to 5 channels
  - 1 × temperature sensor
- Timers:
  - 2 × 54-bit general-purpose timer
  - 1 × 52-bit system timer
  - 3 × watchdog timers

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1792 bits for users
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197, against DPA attack)
  - ECB/CBC/CFB/OFB/CTR (FIPS PUB 800-38A)

  - SHA Accelerator (FIPS PUB 180-4)
  - RSA Accelerator
  - ECC Accelerator
  - ECDSA (Elliptic Curve Digital Signature Algorithm)
  - Digital signature
  - HMAC
- Access permission management (APM)
- Random Number Generator (RNG)

Applications (A Non-exhaustive List)

With ultra-low power consumption, ESP32-H2 is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
  - Indoor positioning
  - Meter reading systems
  - Security systems
  - HVAC systems
- Industrial Automation
  - Industrial robot
  - Mesh network
  - Human machine interface (HMI)
  - Industrial field bus
  - Asset management
  - Personnel tracking
- Health Care
  - Health monitor
  - Baby monitor
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Logger toys and proximity sensing toys
  - Gaming consoles
  - Wireless remote controls
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agricultural robot
  - Livestock tracking
- Retail and Catering
  - Service robot
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-h2_datasheet_en.pdf

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1.1 Nomenclature

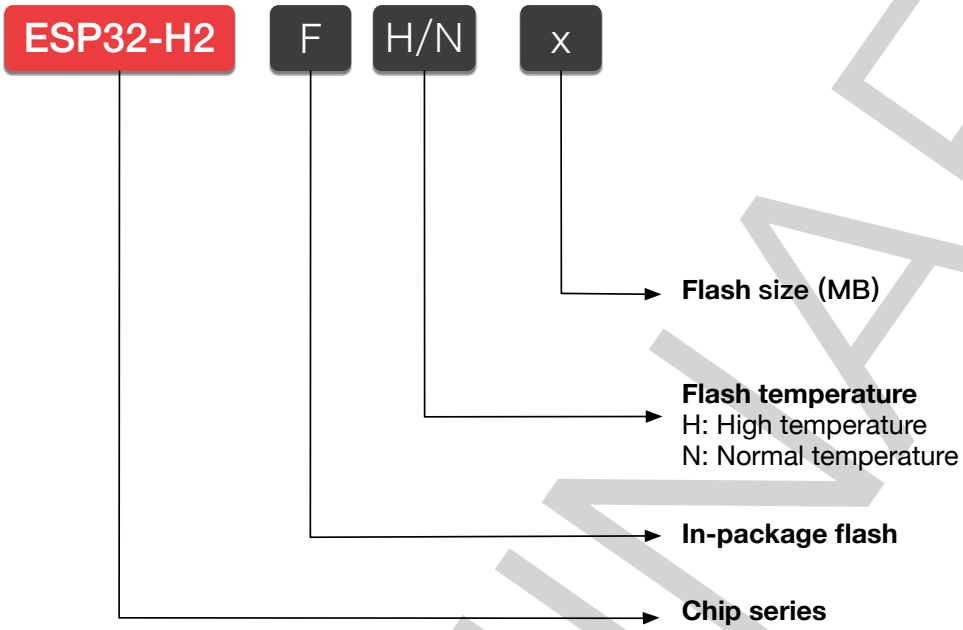

Figure 1-1. ESP32-H2 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32-H2 Series Comparison

Ordering Code	In-package Flash	Ambient Temperature (°C)	SPI Voltage	Package
ESP32-H2FH2	2 MB (Quad SPI)	–40 ~ 105	3.3 V	QFN32
ESP32-H2FH4	4 MB (Quad SPI)	–40 ~ 105	3.3 V	QFN32

2 Pin Definition

2.1 Pin Layout

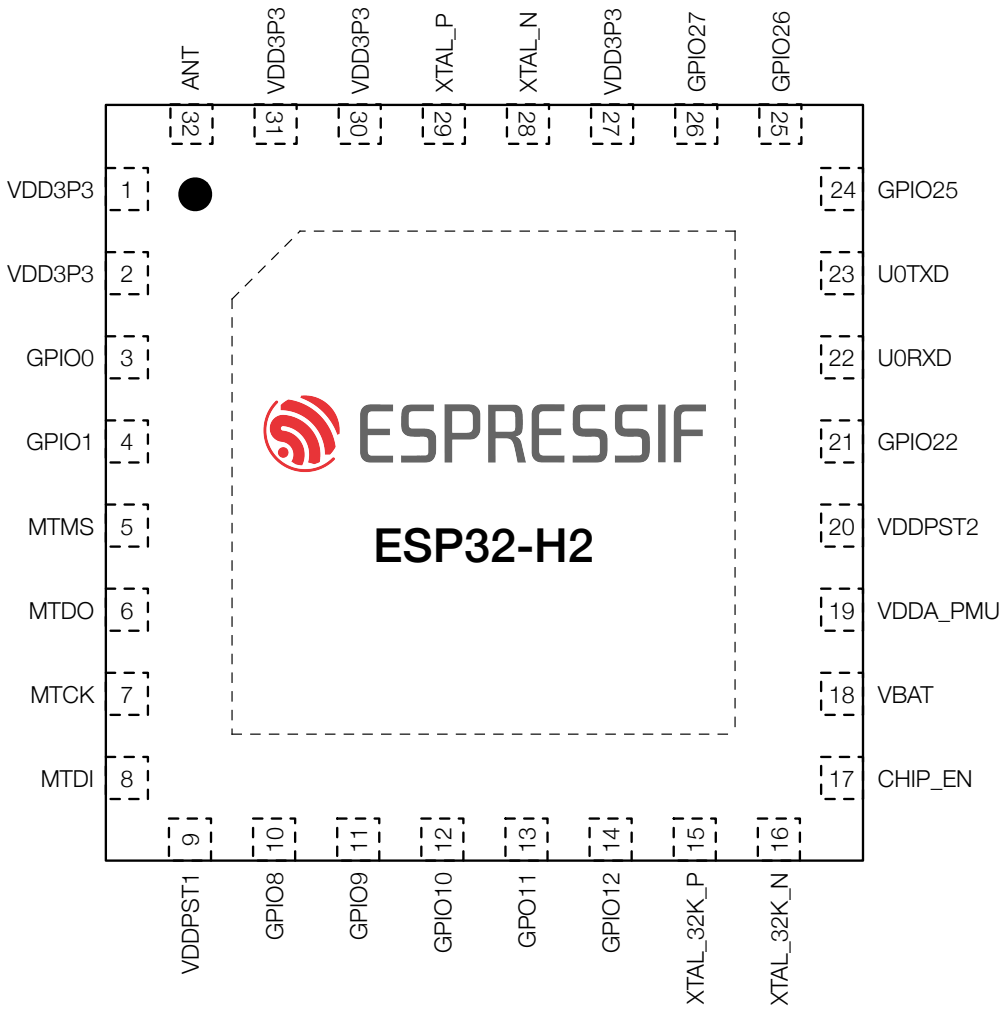

Figure 2-1. ESP32-H2 Pin Layout (Top View)

2.2 Pin Description

Table 2-1. Pin Description

Name	No.	Type[1]	Power Supply Pin	Function
VDD3P3	1	P_A	—	Analog power supply (3.3 V)
VDD3P3	2	P_A	—	Analog power supply (3.3 V)
GPIO0	3	I/O/T	VDDPST1	**GPIO0**, FSPIQ
GPIO1	4	I/O/T	VDDPST1	**GPIO1**, FSPICS0, ADC1_CH0
MTMS	5	I/O/T	VDDPST1	GPIO2, FSPIWP, ADC1_CH1, **MTMS**
MTDO	6	I/O/T	VDDPST1	GPIO3, FSPIHD, ADC1_CH2, **MTDO**

Name	No.	Type	Power Supply Pin	Function
MTCK	7	I/O/T	VDDPST1	GPIO4, FSPICLK, ADC1_CH3, **MTCK**
MTDI	8	I/O/T	VDDPST1	GPIO5, FSPID, ADC1_CH4, **MTDI**
VDDPST1	9	P_{IO}	—	3.3 V IO power supply
GPIO8	10	I/O/T	VDDPST1	**GPIO8**
GPIO9	11	I/O/T	VDDPST1	**GPIO9**
GPIO10	12	I/O/T	VDDPST1	**GPIO10**, ZCD0
GPIO11	13	I/O/T	VDDPST1	**GPIO11**, ZCD1
GPIO12	14	I/O/T	VDDA_PMU/VBAT	**GPIO12**
XTAL_32K_P	15	I/O/T	VDDA_PMU/VBAT	**GPIO13**, XTAL_32K_P
XTAL_32K_N	16	I/O/T	VDDA_PMU/VBAT	**GPIO14**, XTAL_32K_N
CHIP_EN	17	I	VBAT	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_EN pin floating.
VBAT	18	P_A	—	Analog power supply or battery power supply (3.0 ~ 3.6 V)
VDDA_PMU	19	P_A	—	Analog power supply (3.3 V)
VDDPST2	20	P_{IO}	—	3.3 V IO power supply
GPIO22	21	I/O/T	VDDPST2	**GPIO22**
U0RXD	22	I/O/T	VDDPST2	GPIO23, FSPICS1, **U0RXD**
U0TXD	23	I/O/T	VDDPST2	GPIO24, FSPICS2, **U0TXD**
GPIO25	24	I/O/T	VDDPST2	**GPIO25**, FSPICS3
GPIO26	25	I/O/T	VDDPST2	GPIO26, FSPICS4, **USB_D-**
GPIO27	26	I/O/T	VDDPST2	GPIO27, FSPICS5, **USB_D+**
VDD3P3	27	P_A	—	Analog Power supply (3.3 V)
XTAL_N	28	—	—	External crystal output
XTAL_P	29	—	—	External crystal input
VDD3P3	30	P_A	—	Analog power supply (3.3 V)
VDD3P3	31	P_A	—	Analog power supply (3.3 V)
ANT	32	I/O	—	RF input and output
GND	33	G	—	Ground

[1] P_A: analog power supply; P_D: digital power supply; P_{IO}: IO pin power supply; I: input; O: output; T: high impedance.

2.3 Power Scheme

Table 2-2. Description of ESP32-H2 Power Supply Pins

Type	Pin Name	Power Supply to
P_{IO}	VDDPST1	Group0 IO[1]
	VDDPST2	Group1 IO[1]
P_A	VDDA_PMU	Analog System
	VDD3P3	
	VBAT	

[1] For a complete list of IO pins powered by VDDPST1 and VDDPST2, see Table 2-1.

Notes on CHIP_EN:

Figure 2-2 shows the power-up and reset timing of ESP32-H2. Details about the parameters are listed in Table 2-3.

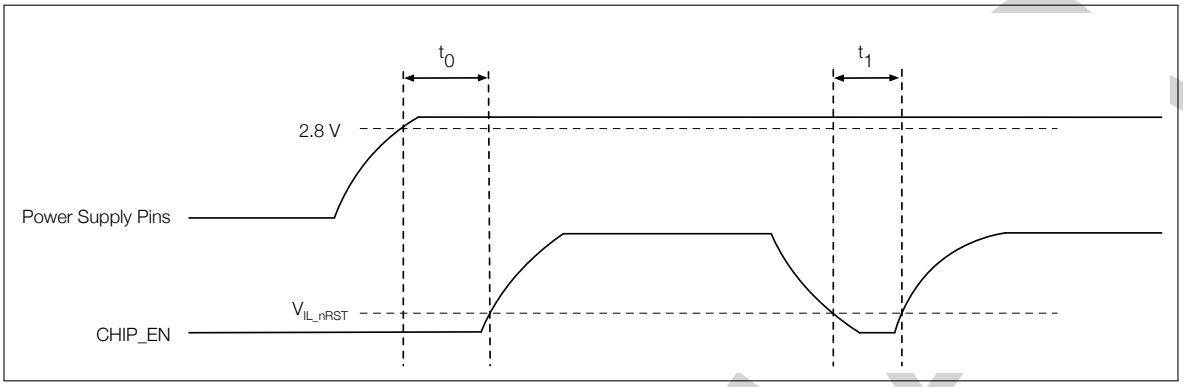

Figure 2-2. ESP32-H2 Power-up and Reset Timing

Table 2-3. Description of ESP32-H2 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the power supply pins * and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} (see Table 4-4) to reset the chip	50

* For a complete list of power supply pins, see Table 2-2.

2.4 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

ESP32-H2 has the following parameters controlled by the given strapping pins at chip reset:

- **Chip boot mode** – GPIO8 and GPIO9
- **ROM message printing** – GPIO8
- **JTAG signal source** – GPIO25

GPIO9 is connected to the chip's internal weak pull-up resistor at chip reset. This resistor determines the default bit value of GPIO9. Also, the resistor determines the bit value if GPIO9 is connected to an external high-impedance circuit.

Table 2-4. Default Configuration of Strapping Pins

Strapping Pin	Default Config	Bit Value
GPIO8	Floating	–
GPIO9	Pull-up	1
GPIO25	Floating	–

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-H2 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IOs after reset.

2.4.1 Chip Boot Mode Control

After the reset is released, the combination of GPIO8 and GPIO9 controls the boot mode. See Table 2-5 Boot Mode Control.

Table 2-5. Boot Mode Control

Boot Mode	GPIO8	GPIO9
Default Config	– (Floating)	1 (Pull-up)
SPI Boot	Any value	1
Joint Download Boot[1]	1	0

[1] Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

In addition to SPI Boot and Joint Download Boot modes, ESP32-H2 also supports SPI Download Boot mode. For details, please see *ESP32-H2 Technical Reference Manual* > Chapter *Chip Boot Control*.

2.4.2 ROM Messages Printing Control

During the ROM boot stage of SPI Boot mode, GPIO8, LP_AON_STORE4_REG[0] and EFUSE_UART_PRINT_CONTROL jointly control the printing of ROM messages.

Table 2-6. ROM Message Printing Control

Register[1]	eFuse[2]	GPIO8	ROM Message Printing
0	0 (0b00)	x[3]	ROM messages are always printed to UART0 during boot
	1 (0b01)	0	Print is enabled during boot
		1	Print is disabled during boot
	2 (0b10)	0	Print is disabled during boot
		1	Print is enabled during boot
	3 (0b11)	x	Print is disabled during boot
1	x	x	Print is disabled during boot

[1] Register: LP_AON_STORE4_REG[0]

[2] eFuse: EFUSE_UART_PRINT_CONTROL

[3] x: x indicates that the value has no effect on the result and can be ignored.

ROM message is printed to UART0 and USB Serial/JTAG Controller by default during power-on. Users can disable the printing to USB Serial/JTAG Controller by setting the eFuse bit EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT.

Note that if EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT is set to 0 to print to USB, but the USB Serial/JTAG Controller has been disabled, then ROM messages will not be printed to USB Serial/JTAG Controller.

Detailed description about the above-mentioned registers can be found in *ESP32-H2 Technical Reference Manual* > Chapter *eFuse Controller (EFUSE)*.

2.4.3 JTAG Signal Source Control

The strapping pin GPIO25 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 2-7 shows, GPIO25 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

Table 2-7. JTAG Signal Source Control

eFuse 1[a]	eFuse 2[b]	eFuse 3[c]	GPIO25	JTAG Signal Source
0	0	0	Ignored	USB Serial/JTAG Controller
		1	0	JTAG pins MTDI, MTCK, MTMS, and MTDO
			1	USB Serial/JTAG Controller
0	1	Ignored	Ignored	JTAG pins MTDI, MTCK, MTMS, and MTDO
1	0	Ignored	Ignored	USB Serial/JTAG Controller
1	1	Ignored	Ignored	JTAG is disabled

[a] eFuse 1: EFUSE_DIS_PAD_JTAG

[b] eFuse 2: EFUSE_DIS_USB_JTAG

[c] eFuse 3: EFUSE_JTAG_SEL_ENABLE

Detailed description about the above-mentioned registers can be found in *ESP32-H2 Technical Reference Manual*

> Chapter *eFuse Controller (EFUSE)*.

Figure 2-3 shows the setup and hold time for the strapping pin before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 2-8.

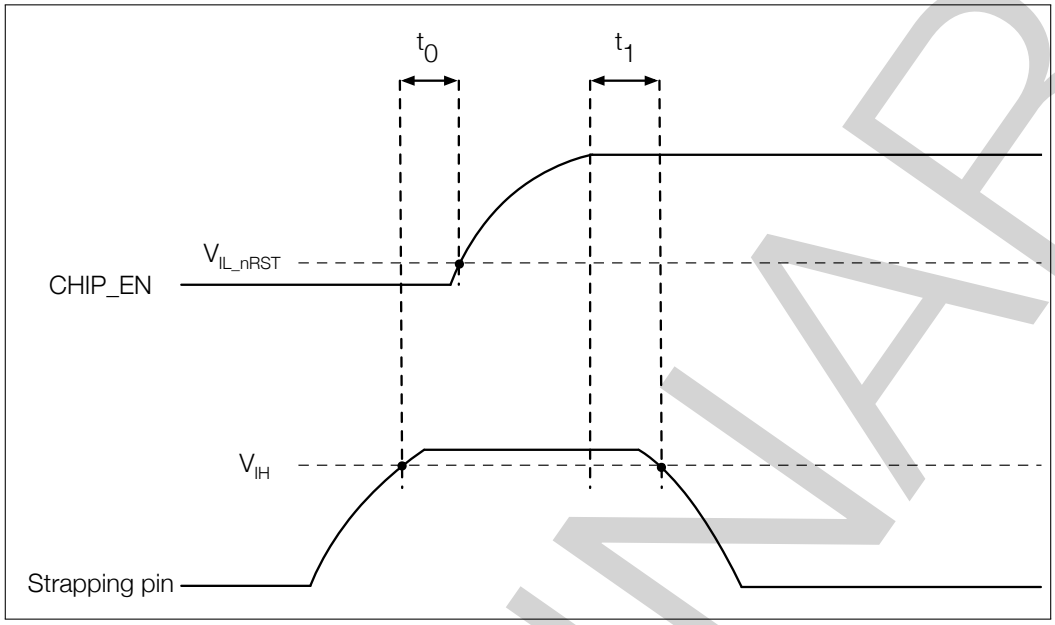

Figure 2-3. Setup and Hold Times for the Strapping Pin

Table 2-8. Parameter Descriptions of the Setup and Hold Time for the Strapping Pin

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

3 Functional Description

3.1 CPU and Memory

3.1.1 CPU

ESP32-H2 has a low-power 32-bit RISC-V single-core microprocessor with the following features:

- Four-stage pipeline that supports a clock frequency of up to 96 MHz
- RV32IMAC instruction set architecture
- 32-bit multiplier and 32-bit divider
- Up to 32 vectored interrupts at 15 priority levels
- Up to 4 hardware breakpoints/watchpoints
- Up to 16 PMP/PMA regions
- JTAG for debugging
- Compliant with RISC-V debug specification v0.13
- Compliant with RISC-V Trace Specification v1.0

3.1.2 Internal Memory

ESP32-H2's internal memory includes:

- **128 KB of ROM**: for booting and core functions
- **320 KB of SRAM**: for data and instructions.
- **LP memory**: 4 KB of SRAM that can be accessed by the CPU. It can retain data in Deep-sleep mode
- **4 Kbit of eFuse**: 1792 bits are reserved for user data, such as encryption key and device ID
- **2 MB or 4 MB of in-package flash**

3.1.3 Cache

ESP32-H2 has an eight-way set associative cache. This cache is read-only and has the following features:

- Size: 16 KB
- Block size: 32 bytes
- Pre-load function
- Lock function
- Critical word first and early restart

3.2 System Clocks

ESP32-H2 clocks can be classified into two types depending on their frequencies:

- High-performance (HP) clocks for devices working at a higher frequency, such as CPU and digital peripherals
  - PLL_F96M_CLK (96 MHz): internal PLL clock. Its reference clock is XTAL_CLK.
  - PLL_F64M_CLK (64 MHz): internal PLL clock. Its reference clock is XTAL_CLK.
  - XTAL_CLK (32 MHz): external crystal clock
- Low-power (LP) clocks for low-power system and some peripherals working in low-power mode
  - XTAL32K_CLK (32 kHz): external crystal clock
  - RC_FAST_CLK (8 MHz by default): internal fast RC oscillator with adjustable frequency
  - RC_SLOW_CLK (130 kHz by default): internal slow RC oscillator with adjustable frequency
  - OSC_SLOW_CLK (32 kHz by default): external slow clock input through XTAL_32K_P and XTAL_32K_N. After configuring these two GPIOs, also configure the Hold function (see *ESP32-H2 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix (GPIO, IO_MUX)* > Section PadHold)
  - PLL_LP_CLK (8 MHz): internal PLL clock, with reference clock XTAL32K_CLK

The application can select the clock source from the clocks above. The selected clock source drives the high-performance clock directly, or after division, depending on the application.

Note:
ESP32-H2 is unable to operate without an external main crystal clock.

3.3 Access Permission Management

3.3.1 Access Permission Management (APM)

ESP32-H2 integrates an APM module to manage access permissions. The module compares information transmitted over the bus with predefined configurations and decides if to grant access.

3.3.2 Timeout Protection

ESP32-H2 integrates 3 timeout protection modules in CPU peripherals, HP peripherals and LP peripherals, respectively, against bus being stuck. These modules have the following features:

- Integrate a 16-bit timeout counter for each timeout period
- Support for interrupts
- Exception records

3.4 Analog Peripherals

3.4.1 Analog-to-Digital Converter (ADC)

ESP32-H2 integrates one 12-bit SAR ADC which supports measurements on 5 channels (analog-enabled pins).

3.4.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –40 °C to 125 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

3.4.3 Analog Comparator

ESP32-H2 provides one analog PAD voltage comparator including two PADs. This peripheral can be used to compare the voltages of the two PADs or compare the voltage of one PAD with a stable internal voltage that can be adjustable.

3.5 Digital Peripherals

3.5.1 General Purpose Input/Output Interface (GPIO)

ESP32-H2 has 19 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pins. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pins while peripheral output signals can be configured to any IO pins. Table 3-1 shows the IO MUX functions of each pin. For more information about IO MUX and GPIO matrix, please refer to *ESP32-H2 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix (GPIO, IO_MUX)*.

Table 3-1. IO MUX Pin Functions

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
GPIO0	3	GPIO0	GPIO0	FSPIQ	0	—
GPIO1	4	GPIO1	GPIO1	FSPICS0	0	R
MTMS	5	MTMS	GPIO2	FSPIWP	1	R
MTDO	6	MTDO	GPIO3	FSPIHD	1	R
MTCK	7	MTCK	GPIO4	FSPICLK	1*	R
MTDI	8	MTDI	GPIO5	FSPID	1	R
GPIO8	10	GPIO8	GPIO8	—	1	—
GPIO9	11	GPIO9	GPIO9	—	3	—
GPIO10	12	GPIO10	GPIO10	—	0	R
GPIO11	13	GPIO11	GPIO11	—	0	R
GPIO12	14	GPIO12	GPIO12	—	0	—
XTAL_32K_P	15	GPIO13	GPIO13	—	0	R

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
XTAL_32K_N	16	GPIO14	GPIO14	—	0	R
GPIO22	21	GPIO22	GPIO22	—	0	—
U0RXD	22	U0RXD	GPIO23	FSPICS1	3	—
U0TXD	23	U0TXD	GPIO24	FSPICS2	4	—
GPIO25	24	GPIO25	GPIO25	FSPICS3	1	—
GPIO26	25	GPIO26	GPIO26	FSPICS4	1	R, USB
GPIO27	26	GPIO27	GPIO27	FSPICS5	3*	R, USB

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up registor enabled (OE = 1, WPU = 1)
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
  0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
  1, input enabled, in high impedance state (IE = 1)
- **3*** - input enabled, pull-up resistor enabled (IE = 1, WPU = 0, USB_WPU = 1). See details in Notes

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design, or enable internal pull-up and pull-down resistors during software initialization.

GPIO Input Mode

The input function of GPIO can be configured as hysteresis or normal mode:

- Hysteresis mode: In the hysteresis mode, the threshold voltage for flipping between high and low levels of GPIO input depends on the direction of level flipping. Specifically, the voltage threshold for flipping from high to low level is slightly lower than the voltage threshold for flipping from low to high level. For details, see *ESP32-H2 Technical Reference Manual* > Chapter *IO_MUX and GPIO Matrix (GPIO, IO_MUX)*.
- Normal mode: The threshold voltage for flipping between high and low levels of GPIO input is independent of the direction of level flipping. In other words, the voltage threshold for flipping from high to low level is the same as the voltage threshold for flipping from low to high level.

Notes

- **R** - These pins have analog functions.
- **USB** - USB pull-up resistor enabled
  - By default, the USB function is enabled for USB pins (i.e., GPIO26 and GPIO27), and the pin pull-up is decided by the USB pull-up. The USB pull-up is controlled by USB_SERIAL_JTAG

_DP/DM_PULLUP and the pull-up resistor value is controlled by USB_SERIAL_JTAG_PULLUP_VALUE. For details, see *ESP32-H2 Technical Reference Manual* > Chapter *USB Serial/JTAG Controller*.

- When the USB function is disabled, USB pins are used as regular GPIOs and the pin's internal weak pull-up and pull-down resistors are disabled by default (configurable by IO_MUX_GPIO*n*_FUN_WPU/WPD). For details, see *ESP32-H2 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix (GPIO, IO MUX)*).

3.5.2 Serial Peripheral Interface (SPI)

ESP32-H2 features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can only be configured to operate in SPI memory mode, while SPI2 can be configured to operate in both SPI memory and general-purpose SPI modes.

- **SPI Memory mode**

  In SPI memory mode, SPI0, SPI1 and SPI2 interface with in-package flash. Data is transferred in bytes. Up to four-line SDR reads and writes are supported. The clock frequency is configurable to a maximum of 64 MHz in SDR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. SPI2 supports two-line full-duplex communication and single-/two-/four-line half-duplex communication in both master and slave modes. The host's clock frequency is configurable. Data is transferred in bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface can be connected to GDMA.

  - In master mode, the clock frequency is 48 MHz at most, and the four modes of SPI transfer format are supported.
  - In slave mode, the clock frequency is 48 MHz at most, and the four modes of SPI transfer format are also supported.

3.5.3 Universal Asynchronous Receiver Transmitter (UART)

ESP32-H2 has two UART interfaces, i.e. UART0 and UART1, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF). Both UART interfaces are connected to GDMA via UHCI0, and can be accessed by the GDMA controller or directly by the CPU.

3.5.4 I2C Interface

ESP32-H2 has two I2C bus interfaces which are used for I2C master mode or slave mode, depending on the user's configuration. The I2C interfaces support:

- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- Up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- Double addressing mode

- 7-bit broadcast address

Users can configure instruction registers to control the I2C interfaces for more flexibility.

3.5.5 I2S Interface

ESP32-H2 includes a standard I2S interface. This interface can operate as a master or a slave in full-duplex mode or half-duplex mode, and can be configured for 8-bit, 16-bit, 24-bit, or 32-bit serial communication. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface supports TDM PCM, TDM MSB alignment, TDM standard, and PDM TX interface. It connects to the GDMA controller.

3.5.6 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channels of infrared remote transmission and two channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All four channels share a 192 × 32-bit memory block to store transmit or receive waveform.

3.5.7 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller supports:

- Generating digital waveform with configurable periods and duty cycle. The resolution of duty cycle can be up to 20 bits.
- Multiple clock sources, including 96 MHz PLL clock, 64 MHz PLL clock, external main crystal clock, and internal fast RC oscillator.
- Operation when the CPU is in Light-sleep mode.
- Gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.
- Up to 16 duty cycle ranges for gamma curve generation, each can be independently configured in terms of duty cycle direction (increase or decrease), step size, the number of steps, and step frequency

3.5.8 General DMA Controller

ESP32-H2 has a general DMA controller (GDMA) with six independent channels, i.e. three transmit channels and three receive channels. These six channels are shared by peripherals with DMA feature. The GDMA controller supports fixed priority arbiter or round robin arbiter among these channels.

The GDMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal RAM.

Peripherals on ESP32-H2 with DMA feature are SPI2, UHCI0, I2S, PARLIO, AES, SHA, and ADC.

3.5.9 USB Serial/JTAG Controller

ESP32-H2 integrates a USB Serial/JTAG controller. This controller has the following features:

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)

- CDC-ACM virtual serial port and JTAG adapter functionality
- Programming the chip's flash
- CPU debugging with compact JTAG instructions
- A full-speed USB PHY integrated in the chip

3.5.10 SoC Event Task Matrix (ETM)

ESP32-H2 integrates a SOC ETM with multiple channels. Each input event on channels is mapped to an output task. Events are generated by peripherals, while tasks are received by peripherals. The SOC ETM has the following features:

- up to 50 mapping channels, each connected to an event and a task and controlled independently
- an event or a task can be mapped to any tasks or events in the matrix. That is to say, one event can be mapped to different tasks via multiple channels, or different events can be mapped to the same task via their individual channels
- peripherals supporting ETM include GPIO, LED PWM, general-purpose timers, RTC timer, system timer, MCPWM, temperature sensor, ADC, I2S, GDMA, and PMU

3.5.11 Motor Control PWM (MCPWM)

ESP32-H2 integrates a MCPWM that can be used to drive digital motors and smart light. This controller has a clock divider (prescaler), three PWM timers, three PWM operators, and a dedicated capture submodule.

PWM timers are used to generate timing references. The PWM operators generate desired waveform based on the timing references. By configuration, a PWM operator can use the timing reference of any PWM timer, and use the same timing reference with other PwM operators. PWM operators can also use different PWM timers' values to produce independent PWM signals. PWM timers can be synchronized.

3.5.12 Pulse Count Controller (PCNT)

The pulse count controller (PCNT) in ESP32-H2 captures pulses and counts pulse edges in seven modes. It has the following features:

- Four independent pulse counters (units) that count from 1 to 65535
- Each unit consists of two independent channels sharing one pulse counter
- All channels have input pulse signals (e.g. sig_ch0_u*n*) with their corresponding control signals (e.g. ctrl_ch0_u*n*)
- Independently filter glitches of input pulse signals (sig_ch0_u*n* and sig_ch1_u*n*) and control signals (ctrl_ch0_u*n* and ctrl_ch1_u*n*) on each unit
- Each channel has the following parameters:
  1. Selection between counting on positive or negative edges of the input pulse signal
  2. Configuration to Increment, Decrement, or Disable counter mode for control signal's high and low states

3.5.13 TWAI® Controller

ESP32-H2 has one TWAI® controllers with the following features:

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- 64-byte receive FIFO
- Acceptance filter (single and dual filter modes)
- Error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

3.5.14 Parallel IO (PARLIO) Controller

ESP32-H2 contains a Parallel IO controller (PARLIO) capable of transferring data between external devices and internal memory on a parallel bus through GDMA. It is composed of a TX unit and a RX unit, which are fixed as a transmitter and a receiver respectively. With the two units combined, PARLIO achieves full-duplex communication.

Due to the flexibility of IO data, PARLIO can function as a general interface to connect various peripherals. For example, a peer-to-peer transfer can be achieved by taking SPI as the master device and PARLIO as the slave device.

3.6 Radio

The ESP32-H2 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- Bias and regulators
- Balun and transmit-receive switch
- Clock generator

3.6.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to baseband signals and converts them to the digital domain with two high-resolution ADCs. To adapt to varying signal channel conditions, ESP32-H2 integrates RF filters, Automatic Gain Control (AGC), DC offset cancellation circuits, and baseband filters.

3.6.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the baseband signals to the 2.4 GHz RF signal, and drives the antenna with a CMOS power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- Carrier leakage
- I/Q amplitude/phase matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

3.6.3 Clock Generator

The clock generator produces clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.7 Bluetooth Low Energy

ESP32-H2 includes a Bluetooth Low Energy subsystem that integrates a link controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5 and Bluetooth mesh.

3.7.1 Bluetooth LE PHY

ESP32-H2's Bluetooth Low Energy PHY supports:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- Coded PHY for longer range (125 Kbps and 500 Kbps)
- HW Listen before talk (LBT)

3.7.2 Bluetooth LE Link Controller

ESP32-H2's Bluetooth Low Energy Link Controller supports:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- Multiple advertisement sets
- Simultaneous advertising and scanning
- Multiple connections in simultaneous central and peripheral roles
- Adaptive frequency hopping and channel assessment
- Channel selection algorithm #2
- LE power control
- Connection parameter update
- High duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension

- Link layer extended scanner filter policies
- Low duty cycle connectable directed advertising
- Link layer encryption
- LE Ping

3.8 802.15.4

ESP32-H2 includes an IEEE Standard 802.15.4 subsystem that integrates PHY and MAC layers. It supports various software stacks includes Thread, Zigbee, Matter, HomeKit, MQTT and so on.

3.8.1 802.15.4 PHY

ESP32-H2 's 802.15.4 PHY supports:

- O-QPSK PHY in 2.4 GHz
- 250 Kbps data rate
- RSSI and LQI supported

3.8.2 802.15.4 MAC

ESP32-H2 supports most key features defined in IEEE Standard 802.15.4-2015, includes:

- CSMA/CA
- Active scan and energy detect
- HW frame filter
- HW auto acknowledge
- HW auto frame pending
- Coordinated sampled listening (CSL)

3.9 Radio Protocols Coexistence

ESP32-H2 has a 2.4 GHz radio protocols coexistence controller (COEX) for radio resource management. This controller supports:

- The coexistence of Bluetooth and IEEE 802.15.4 protocols inside the chip
- External coexistence as a master device
- External coexistence as a slave device
- Multiple external coexistence modes (1-wire PTA, 2-wire PTA and 3-wire PTA)

3.10 Low-power Management

With the use of advanced power-management technologies, ESP32-H2 can switch between different power modes.

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.

- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. Wireless base band and radio are disabled, but Wireless connection can remain active.
- Light-sleep mode: The CPU is paused. Any wake-up events (RTC timer, or external interrupts) will wake up the chip. Wireless base band and radio are disabled, but Wireless connection can remain active. CPU (excluding SRAM) and most peripherals (See ESP32-H2 Block Diagram) can also be powered down to further reduce the power consumption.
- Deep-sleep mode: CPU (including SRAM) and most peripherals (See ESP32-H2 Block Diagram) are powered down. Only the LP memory is powered on. Wireless connection data are stored in the LP memory.

For power consumption in different power modes, please refer to Section 4.6.

3.11 Timers

3.11.1 General Purpose Timers

ESP32-H2 is embedded with two 54-bit general-purpose timers, which are based on 16-bit prescalers and 54-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- A 16-bit clock prescaler, from 1 to 65536
- A 54-bit time-base counter programmable to be incrementing or decrementing
- Able to read real-time value of the time-base counter
- Halting and resuming the time-base counter
- Programmable alarm generation
- Level interrupt generation

3.11.2 System Timer

ESP32-H2 integrates a 52-bit system timer, which has two 52-bit counters and three comparators. The system timer has the following features:

- Counters with a fixed clock frequency of 16 MHz
- Three types of independent interrupts generated according to alarm value
- Two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- Automatic reload of counter value
- Counters can be stalled if the CPU is stalled or in OCD mode

3.11.3 Watchdog Timers

The ESP32-H2 contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and the MWDT in timer group 0 (TIMG0) are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- Four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- Interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- Write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- Flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

3.12 Cryptographic Hardware Accelerators

ESP32-H2 is equipped with hardware accelerators of general algorithms, such as AES-128/AES-256 (FIPS PUB 197, against DPA attack), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), SHA1/SHA224/SHA256 (FIPS PUB 180-4), RSA3072, and ECC accelerator. The chip also supports independent arithmetic, such as large-number multiplication and large-number modular multiplication. The maximum operation length for RSA and large-number modular multiplication is 3072 bits. The maximum operator length for large-number multiplication is 1536 bits.

This chip is also equipped with ECDSA accelerator that supports generating and verifying ECDSA signatures, which offers higher security compared to software implementation.

3.13 Physical Security Features

- Transparent off-package flash encryption (AES-XTS algorithm) with software inaccessible key prevents unauthorized readout of user application code or data.
- Secure boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module can use a software inaccessible MAC key to generate MAC signatures for identity verification and other purposes.
- Digital Signature module can use a software inaccessible secure key to generate RSA signatures for identity verification.
- TEE controller provides four security modes for masters in the system. Hardware resources can be granted different access permissions by APM module in these four modes, so as to establish a security boundary between the four modes.

3.14 Peripheral Pin Configurations

Table 3-2. Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO1	12-bit SAR ADC
	ADC1_CH1	MTMS	
	ADC1_CH2	MTDO	
	ADC1_CH3	MTCK	
	ADC1_CH4	MTDI	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	U0RXD	Two UART channels with hardware flow control and GDMA
	U0CTS_in	Any GPIO pins	
	U0DSR_in		
	U0TXD_out	U0TXD	
	U0RTS_out	Any GPIO pins	
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		
I2C	I2CEXT0_SCL_in	Any GPIO pins	One I2C channel in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
LED PWM	ledc_ls_sig_out0~5	Any GPIO pins	Six independent PWM channels
I2S	I2SO_BCK_in	Any GPIO pins	Stereo input and output from/to the audiocodec
	I2S_MCLK_in		
	I2SO_WS_in		
	I2SI_SD_in		
	I2SI_BCK_in		
	I2SI_WS_in		
	I2SO_BCK_out		
	I2S_MCLK_out		
	I2SO_WS_out		
	I2SO_SD_out		
	I2SI_BCK_out		
	I2SI_WS_out		
	I2SO_SD1_out		
Remote Control Peripheral	RMT_SIG_IN0~1	Any GPIO pins	Two channels for an IR transceiver of various waveforms
	RMT_SIG_OUT0~1		

Interface	Signal	Pin	Function
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	• Master mode and slave mode of SPI, Dual SPI, Quad SPI, and QPI • Connection to in-package flash, RAM, and other SPI devices • Four modes of SPI transfer format • Configurable SPI frequency • 64-byte FIFO or GDMA buffer
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		
TWAI®	TWAI0_RX	Any GPIO pins	Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
	TWAI0_TX		
	TWAI0_BUS_OFF_ON		
	TWAI0_CLKOUT		
	TWAI0_STANDBY		
Pulse counter	PCNT_SIG_CH0_in0~3	Any GPIO pins	Capture pulse and count pulse edges in seven modes
	PCNT_SIG_CH1_in0~3		
	PCNT_CTRL_CH0_in0~3		
	PCNT_CTRL_CH1_in0~3		
MCPWM	PWM0_SYNC0~2_in	Any GPIO pins	1 MCPWM input and output pins. Signals include: • PWM differential output signals • fault input signals to be detected • input signals to be captured • external clock synchronization signals
	PWM0_out0a		
	PWM0_out0b		
	PWM0_out1a		
	PWM0_F0~2_in		
	PWM0_out1b		
	PWM0_out2a		
	PWM0_out2b		
	PWM0_CAP0~2_in		
PARLIO	PARL_RX_DATA0~7	Any GPIO pins	A module for parallel data transfer, with • 8 pins to receive parallel data • 8 pins to transmit parallel data • 1 receiver clock pin (clock input and output) • 2 transmitter clock pins (clock input and output)
	PARL_TX_DATA0~7		
	PARL_RX_CLK_in/_out		
	PARL_TX_CLK_in/_out		

Interface	Signal	Pin	Function
USB Serial/JTAG	USB_D-	GPIO26	USB-to-serial converter, and USB-to-JTAG converter. Note: the pin functions of USB_D+ and USB_D- are interchangeable.
	USB_D+	GPIO27	

4 Electrical Characteristics

The values presented in this section are preliminary and may change with the final release of this datasheet.

4.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD3P3, VBAT, VDDA_PMU, VDDPST1, VDDPST2	Voltage applied to power supply pins per power domain	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	150	°C

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD3P3, VBAT, VDDA_PMU, VDDPST1, VDDPST2	Power Supply Pin	3.0	3.3	3.6	V
I_{VDD}[1]	Current delivered by external power supply	0.35	—	—	A
T_A	Ambient temperature	-40	—	105	°C

[1] If you use a single power supply, the recommended output current is 350 mA or more.

4.3 VDD_SPI Output Characteristics

Table 4-3. VDD_SPI Output Characteristics

Symbol	Parameter	Typ	Unit
R_{SPI}	On-resistance in 3.3 V mode	7.5	Ω

In real-life applications, when VDD_SPI works in 3.3 V output mode, VDDPST2 may be affected by R_{SPI}. For example, when VDDPST2 is used to drive a 3.3 V flash, it should comply with the following specifications:

VDDPST2 > VDD_flash_min + I_flash_max * R_{SPI}

Among which, VDD_flash_min is the minimum operating voltage of the flash, and I_flash_max the maximum current.

For more information, please refer to section 2.3 *Power Scheme*.

4.4 DC Characteristics (3.3 V, 25 °C)

Table 4-4. DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for a particular power domain of pins.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.5 ADC Characteristics

The measurements in this section are taken with an external 100 nF capacitor connected to the ADC, using DC signals as input, 3.3 V power supply, and at an ambient temperature of 25 °C with disabled Wi-Fi.

Table 4-5. ADC Characteristics

Symbol	Min	Max	Unit
DNL (Differential nonlinearity) [1]	–8	12	LSB
INL (Integral nonlinearity)	–10	10	LSB
Sampling rate	—	100	kSPS [2]

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

The calibrated ADC results after hardware calibration and software calibration are shown in Table 4-6. For higher accuracy, you may implement your own calibration methods.

Table 4-6. ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 1000	–7	7	mV
	ATTEN1, effective measurement range of 0 ~ 1300	–8	8	mV
	ATTEN2, effective measurement range of 0 ~ 1900	–12	12	mV
	ATTEN3, effective measurement range of 0 ~ 3300	–23	23	mV

Note:

The above ADC measurement range and accuracy are applicable to chips manufactured on and after the Date Code **342023** on shielding cases, or assembled on and after the D/C 1 and D/C 2 **2334** on bar-code labels. For chips manufactured or assembled earlier than these date codes, please ask our sales team to provide the actual range and accuracy according to batch.

For details of Date Code and D/C, please refer to *Espressif Chip Packaging Information*.

4.6 Current Consumption Characteristics

4.6.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 4-7. Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 20.0 dBm	148
		Bluetooth LE @ 9.0 dBm	76
		Bluetooth LE @ 0 dBm	38
		Bluetooth LE @ –24.0 dBm	26

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Table 4-7 – cont'd from previous page

Work Mode	RF Condition	Description	Peak (mA)
	RX	Bluetooth LE	25

Table 4-8. Current Consumption for 802.15.4 in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.15.4 @ 20.0 dBm	153
		802.15.4 @ 9.0 dBm	75
		802.15.4 @ 0 dBm	38
		802.15.4 @ –24.0 dBm	26
	RX	802.15.4	27

4.6.2 Current Consumption in Other Modes

Table 4-9. Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled[1]
Modem-sleep[2]	96	CPU is running	10	17
		CPU is idle	6	13
	64	CPU is running	8	13
		CPU is idle	5	10
	48	CPU is running	7	11
		CPU is idle	5	9
	32	CPU is running	4	8
		CPU is idle	3	7

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, the consumption might be higher when accessing flash.

Table 4-10. Current Consumption in Low-Power Modes

Mode	Description	Typ (μA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	85
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	25
Deep-sleep	LP timer and LP memory are powered on	7
Power off	CHIP_EN is set to low level, the chip is powered off	1

5 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The front-end circuit is a 0 Ω resistor.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

5.1 Bluetooth 5 (LE) Radio

Table 5-1. Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–24.0 ~ 20.0 dBm

5.1.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 5-2. Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	1.5	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	2.8	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.3	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	2.3	—	kHz
Modulation characteristics	$\Delta\ F1_{avg}$	—	251.8	—	kHz
	Min. $\Delta\ F2_{max}$ (for at least 99.9% of all $\Delta\ F2_{max}$)	—	217.0	—	kHz
	$\Delta\ F2_{avg}/\Delta\ F1_{avg}$	—	0.87	—	—
In-band emissions	± 2 MHz offset	—	–28	—	dBm
	± 3 MHz offset	—	–32	—	dBm
	> ± 3 MHz offset	—	–34	—	dBm

Table 5-3. Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	3.3	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	3.3	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.6	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	2.3	—	kHz

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Table 5-3 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Modulation characteristics	$\Delta\ F1_{avg}$	—	499.9	—	kHz
	Min. $\Delta\ F2_{max}$ (for at least 99.9% of all $\Delta\ F2_{max}$)	—	492.0	—	kHz
	$\Delta\ F2_{avg}/\Delta\ F1_{avg}$	—	0.90	—	—
In-band emissions	± 4 MHz offset	—	–31	—	dBm
	± 5 MHz offset	—	–34	—	dBm
	> ± 5 MHz offset	—	–36	—	dBm

Table 5-4. Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n\rvert_{n=0,\ 1,\ 2,\ 3,\ \ldots k}$	—	1.0	—	kHz
	Max. $\lvert f_0 - f_n\rvert_{n=1,\ 2,\ 3,\ \ldots k}$	—	0.5	—	kHz
	$\lvert f_0 - f_3\rvert$	—	0.4	—	kHz
	Max. $\lvert f_n - f_{n-3}\rvert_{n=7,\ 8,\ 9,\ \ldots k}$	—	0.9	—	kHz
Modulation characteristics	$\Delta\ F1_{avg}$	—	250.5	—	kHz
	Min. $\Delta\ F1_{max}$ (for at least 99.9% of all $\Delta\ F1_{max}$)	—	234.0	—	kHz
In-band emissions	± 2 MHz offset	—	–23	—	dBm
	± 3 MHz offset	—	–34	—	dBm
	> ± 3 MHz offset	—	–42	—	dBm

Table 5-5. Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n\rvert_{n=0,\ 1,\ 2,\ 3,\ \ldots k}$	—	2.3	—	kHz
	Max. $\lvert f_0 - f_n\rvert_{n=1,\ 2,\ 3,\ \ldots k}$	—	0.7	—	kHz
	$\lvert f_0 - f_3\rvert$	—	0.3	—	kHz
	Max. $\lvert f_n - f_{n-3}\rvert_{n=7,\ 8,\ 9,\ \ldots k}$	—	1.1	—	kHz
Modulation characteristics	$\Delta\ F2_{avg}$	—	230.6	—	kHz
	Min. $\Delta\ F2_{max}$ (for at least 99.9% of all $\Delta\ F2_{max}$)	—	221.8	—	kHz
In-band emissions	± 2 MHz offset	—	–28	—	dBm
	± 3 MHz offset	—	–33	—	dBm
	> ± 3 MHz offset	—	–35	—	dBm

Note that the In-band emissions in Table 5-2 and Table 5-5 above are tested at 15 dBm of TX power. However, the test result still meets the Bluetooth SIG standard even if the TX power is increased up to 20 dBm.

5.1.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 5-6. Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–99.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	2	—	dB
		F = F0 – 1 MHz	—	0	—	dB
		F = F0 + 2 MHz	—	–29	—	dB
		F = F0 – 2 MHz	—	–29	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–36	—	dB
		F ≥ F0 + 4 MHz	—	–30	—	dB
		F ≤ F0 – 4 MHz	—	–36	—	dB
	Image frequency	—	—	–30	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–32	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–16	—	dBm
		2003 MHz ~ 2399 MHz	—	–12	—	dBm
		2484 MHz ~ 2997 MHz	—	–16	—	dBm
		3000 MHz ~ 12.75 GHz	—	0	—	dBm
Intermodulation		—	—	–35	—	dBm

Table 5-7. Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–96.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	5	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	1	—	dB
		F = F0 – 2 MHz	—	–2	—	dB
		F = F0 + 4 MHz	—	–27	—	dB
		F = F0 – 4 MHz	—	–32	—	dB
		F = F0 + 6 MHz	—	–33	—	dB
		F = F0 – 6 MHz	—	–36	—	dB
		F ≥ F0 + 8 MHz	—	–36	—	dB
		F ≤ F0 – 8 MHz	—	–36	—	dB
	Image frequency	—	—	–26	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–33	—	dB
		F = F_{image} – 2 MHz	—	1	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–17	—	dBm
		2003 MHz ~ 2399 MHz	—	–27	—	dBm
		2484 MHz ~ 2997 MHz	—	–17	—	dBm
		3000 MHz ~ 12.75 GHz	—	0	—	dBm
Intermodulation		—	—	–27	—	dBm

Table 5-8. Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–106.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	0	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–4	—	dB
		F = F0 – 1 MHz	—	–6	—	dB
		F = F0 + 2 MHz	—	–31	—	dB
		F = F0 – 2 MHz	—	–34	—	dB
		F = F0 + 3 MHz	—	–39	—	dB
		F = F0 – 3 MHz	—	–48	—	dB
		F $\geq$ F0 + 4 MHz	—	–35	—	dB
		F $\leq$ F0 – 4 MHz	—	–48	—	dB
	Image frequency	—	—	–39	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–38	—	dB
		F = F_{image} – 1 MHz	—	–39	—	dB

Table 5-9. Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–102.5	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	2	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–1	—	dB
		F = F0 – 1 MHz	—	–4	—	dB
		F = F0 + 2 MHz	—	–28	—	dB
		F = F0 – 2 MHz	—	–29	—	dB
		F = F0 + 3 MHz	—	–38	—	dB
		F = F0 – 3 MHz	—	–41	—	dB
		F $\geq$ F0 + 4 MHz	—	–33	—	dB
		F $\leq$ F0 – 4 MHz	—	–41	—	dB
	Image frequency	—	—	–33	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–38	—	dB

5.2 802.15.4 Radio

Table 5-10. 802.15.4 RF Characteristics

Name	Description
Center frequency range of operating channel	2405 ~ 2480 MHz

[1] Zigbee in the 2.4 GHz range supports 16 channels at 5 MHz spacing from channel 11 to channel 26.

5.2.1 802.15.4 RF Transmitter (TX) Characteristics

Table 5-11. 802.15.4 Transmitter Characteristics - 250 Kbps

Parameter	Min	Typ	Max	Unit
RF transmit power range	–24.0	—	20.0	dBm
EVM	—	3.5%	—	—

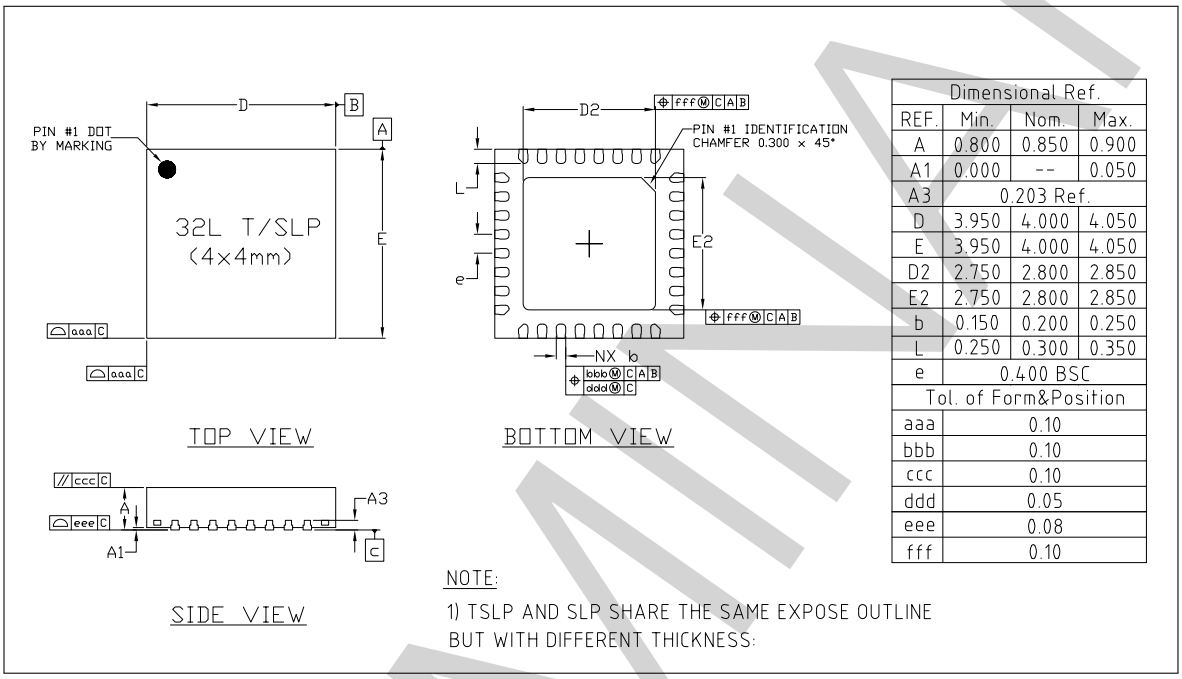
5.2.2 802.15.4 RF Receiver (RX) Characteristics

Table 5-12. 802.15.4 Receiver Characteristics - 250 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @1% PER		—	—	–102.5	—	dBm
Maximum received signal @1% PER		—	—	8	—	dBm
Relative jamming level	Adjacent channel	F = F0 + 5 MHz	—	31	—	dB
		F = F0 – 5 MHz	—	43	—	dB
	Alternate channel	F = F0 + 10 MHz	—	49	—	dB
		F = F0 – 10 MHz	—	54	—	dB

6 Packaging

- For information about tape, reel, and chip marking, please refer to Espressif Chip Packaging Information.
- The pins of the chip are numbered in anti-clockwise order starting from Pin 1 in the top view. For pin numbers and pin names, see also Figure 2-1 ESP32-H2 Pin Layout (Top View).
- Please go to Chipsets to view the recommended PCB package source file (asc). The source file can be imported using software such as PADS or AD (Altium Designer).



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	--	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	2.750	2.800	2.850
E2	2.750	2.800	2.850
b	0.150	0.200	0.250
L	0.250	0.300	0.350
e	0.400 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 6-1. QFN32 (4×4 mm) Package

7 Related Documentation and Resources

Related Documentation

- ESP32-H2 Technical Reference Manual – Detailed information on how to use the ESP32-H2 memory and peripherals.
- ESP32-H2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-H2 into your hardware product.
- ESP32-H2 Series SoC Errata – Descriptions of known errors in ESP32-H2 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-H2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-H2
- *ESP32-H2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-H2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-H2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-H2 Series SoCs* – Browse through all ESP32-H2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-H2
- *ESP32-H2 Series Modules* – Browse through all ESP32-H2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-H2
- *ESP32-H2 Series DevKits* – Browse through all ESP32-H2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-H2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2023-10-17	v0.7	• Added Section 4.5; • Updated the description in Section 3.5.1; • Updated measurements in Table 4-9.
2023-08-02	v0.6	• Updated the description in Section 2.4.1; • Updated the note about USB under Table 3-1; • Updated the description in Section 3.2; • Updated the list of peripherals that support ETM in Section 3.5.10; • Reordered the table content in Table 4-9 from the highest CPU frequency to lowest CPU frequency; • Updated all the measurements in Table 4-9 and Table 4-10 to integers; • Added two notes in Chapter 6.
2023-05-24	v0.5	Preliminary release

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