

ESP8266

System Description



Version 2.2
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About This Guide

The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP8266 series of products, including the ESP8266EX, the ESP-WROOM modules, and ESP-LAUNCHER—the development board.

The document is structured as follows:

Chapter	Title	Subject
Chapter 1	ESP8266EX	Hardware description of the ESP8266EX, including technical specifications, pin definitions, layout, and typical applications.
Chapter 2	ESP-LAUNCHER	Technical description of ESP-LAUNCHER with a built-in ESP8266EX.
Chapter 3	ESP-WROOM	Technical description of ESP-WROOM-01 and ESP-WROOM-02 with built-in ESP8266EX.

Release Notes

Date	Version	Release notes
2015.12	V1.3	First release.
2016.01	V1.4	Sections 1.5.2, 1.5.3 & 1.6 updated.
2016.06	V1.5	Section 3.1 updated.
2016.07	V1.6	Section 2.1 updated.
2017.01	V2.0	Changed the minimum working voltage of ESP8266EX from 3.0V to 2.5V. Updated Table 1-1.
2017.04	V2.1	Changed the chip output impedance from 50Ω to 39+j6 Ω; Stated that Flash1 and Flash2 on ESP-LAUNCHER are both 32 Mbit; Updated Section 1.4.5.
2017.06	V2.2	Updated Section 1.4.2; Added ESP-WROOM-02 module's dimensional tolerance.

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1.

ESP8266EX

1.1. Overview

Espressif's ESP8266EX delivers a highly integrated Wi-Fi SoC solution to meet the continuous demand for efficient power usage, compact design and reliable performance in the industry.

With its complete and self-contained Wi-Fi networking capabilities, ESP8266EX can perform either as a standalone application, or as a slave to a host MCU. When ESP8266EX hosts an application, it promptly boots up from the external flash. The integrated high-speed cache optimizes the system's performance and memory.

Also, ESP8266EX can be applied to any micro-controller design as a Wi-Fi adaptor through SPI/SDIO or I2C/UART interfaces.

Besides the Wi-Fi functionalities, ESP8266EX also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor and on-chip SRAM. It can be interfaced with external sensors and other devices through the GPIOs, resulting in low development cost at early stage and minimum footprint. Software Development Kit (SDK) provides sample codes for various applications.

ESP8266EX integrates antenna switches, RF balun, power amplifier, low-noise receive amplifier, filters and power management modules. The compact design minimizes the PCB size and the external circuitry.

ESP8266EX enables sophisticated features, such as:

- Fast switching between sleep and wake-up modes for efficient energy use;
- Adaptive radio biasing for low-power operation;
- Advanced signal processing;
- Spur cancellation;
- Radio co-existence mechanisms for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

Figure 1-1 shows the functional blocks of ESP8266EX.

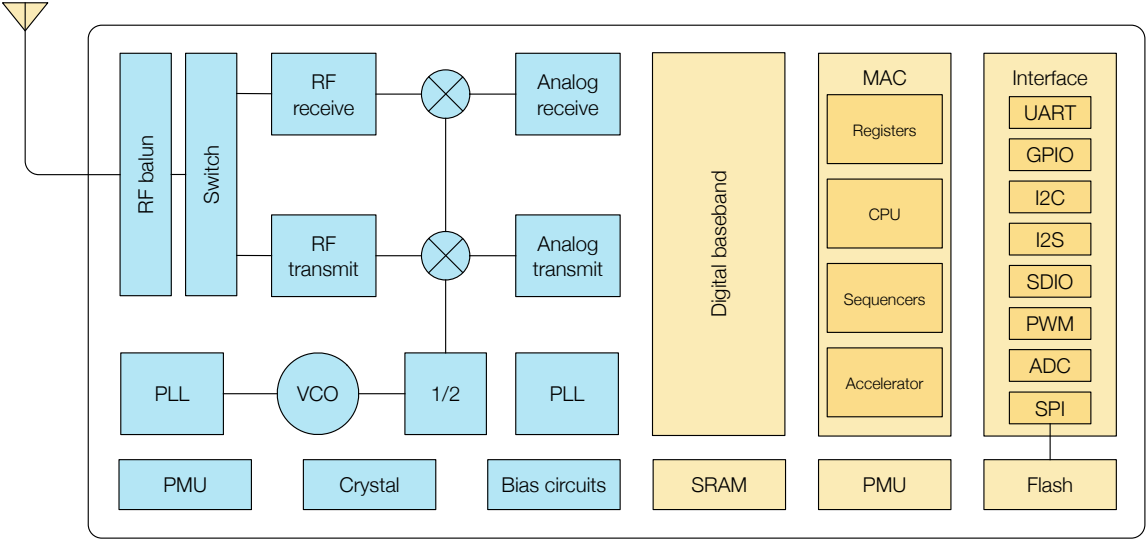


Figure 1-1. ESP8266EX Block Diagram

1.2. Specifications

Table 1-1. ESP8266EX Specifications

Categories	Items	Parameters
Wi-Fi	Standard	FCC/CE/TELEC/SRRC
	Protocols	802.11 b/g/n/e/i
	Frequency Range	2.4G ~ 2.5G (2400M ~ 2483.5M)
	Tx power	802.11 b: +20 dBm
		802.11 g: +17 dBm
		802.11 n: +14 dBm
	Rx Sensitivity	802.11 b: -91 dBm (11 Mbps)
		802.11 g: -75 dBm (54 Mbps)
		802.11 n: -72 dBm (MCS7)
Hardware	Antenna	on-board, external, IPEX connector, ceramic chip
	Peripheral interface	UART/SDIO/SPI/I2C/I2S/IR Remote Control
		GPIO/PWM
	Operating voltage	2.5V ~ 3.6V
	Operating current	Average: 80 mA
	Operating temperature range	-40°C ~ 125°C
	Storage temperature range	-40°C ~ 125°C



Categories	Items	Parameters
	Package size	QFN32-pin (5 mm x 5 mm)
	External interface	N/A
Software	Wi-Fi mode	Station/SoftAP/SoftAP+Station
	Security	WPA/WPA2
	Encryption	WEP/TKIP/AES
	Firmware upgrade	UART Download/OTA (via network)
	Software development	SDK for customized development/cloud server development
	Network Protocols	IPv4, TCP/UDP/HTTP/FTP
	User configuration	AT Instruction Set, Cloud Server, Android/ iOS app

1.3. Pin Definitions

The pin layout for the 32-pin QFN package is illustrated in Figure 1-2.

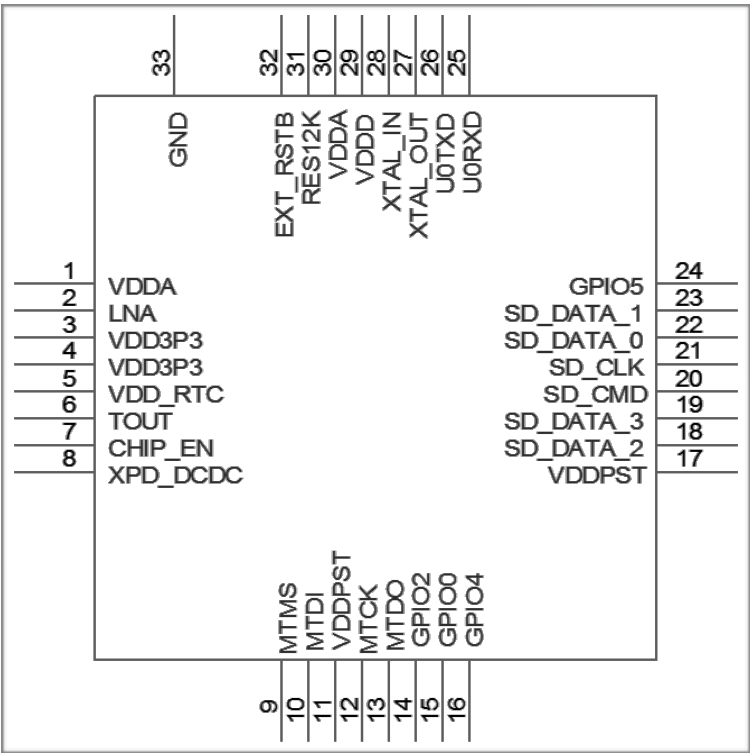


Figure 1-2. ESP8266EX Pin Layout

Table 1-2 lists the definitions and functions of each pin.



Table 1-2. ESP8266EX Pin Definitions

Pin	Name	Type	Function
1	VDDA	P	Analog Power 2.5V ~ 3.6V
2	LNA	I/O	RF antenna interface Chip output impedance=39+j6 Ω . It is suggested that users retain the π -type matching network which matches the antenna.
3	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
4	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
5	VDD_RTC	P	NC (1.1V)
6	TOUT	I	ADC pin. It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin 6). However, these two functions cannot be used simultaneously.
7	CHIP_PU	I	Chip Enable High: On, chip works properly Low: Off, small current consumed
8	XPD_DCDC	I/O	Deep-sleep wakeup (need to be connected to EXT_RSTB); GPIO16
9	MTMS	I/O	GPIO 14; HSPI_CLK
10	MTDI	I/O	GPIO 12; HSPI_MISO
11	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)
12	MTCK	I/O	GPIO 13; HSPI_MOSI; UART0_CTS
13	MTDO	I/O	GPIO 15; HSPI_CS; UART0_RTS
14	GPIO2	I/O	UART Tx during flash programming; GPIO2
15	GPIO0	I/O	GPIO0; SPI_CS2
16	GPIO4	I/O	GPIO 4
17	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)
18	SDIO_DATA_2	I/O	Connects to SD_D2 (Series R: 200 Ω); SPIHD; HSPiHD; GPIO 9
19	SDIO_DATA_3	I/O	Connects to SD_D3 (Series R: 200 Ω); SPIWP; HSPiWP; GPIO 10
20	SDIO_CMD	I/O	Connects to SD_CMD (Series R: 200 Ω); SPI_CS0; GPIO 11
21	SDIO_CLK	I/O	Connects to SD_CLK (Series R: 200 Ω); SPI_CLK; GPIO 6
22	SDIO_DATA_0	I/O	Connects to SD_D0 (Series R: 200 Ω); SPI_MSIO; GPIO 7
23	SDIO_DATA_1	I/O	Connects to SD_D1 (Series R: 200 Ω); SPI_MOSI; GPIO 8
24	GPIO5	I/O	GPIO 5



Pin	Name	Type	Function
25	U0RXD	I/O	UART Rx during flash programming; GPIO 3
26	U0TXD	I/O	UART Tx during flash programming; GPIO 1; SPI_CS1
27	XTAL_OUT	I/O	Connects to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connects to crystal oscillator input
29	VDDD	P	Analog Power 2.5V ~ 3.6V
30	VDDA	P	Analog Power 2.5V ~ 3.6V
31	RES12K	I	Serial connection with a 12 kΩ resistor and connect to the ground
32	EXT_RSTB	I	External reset signal (Low voltage level: Active)

Note:

GPIO2, GPIO0, and MTDO are configurable on PCB as the 3-bit strapping register that determines the booting mode and the SDIO timing mode.

1.4. Schematic Checklist

The highly-integrated design of ESP8266EX reduces the number of components required. Besides ESP8266EX, less than 10 resistors and capacitors, one crystal oscillator and one SPI flash are needed to make a complete module with wireless communication capability.

The following is a detailed description of ESP8266EX schematics, and the layout design which ensures optimum functionality.

The complete circuit diagram of ESP8266EX is illustrated in Figure 1-3.

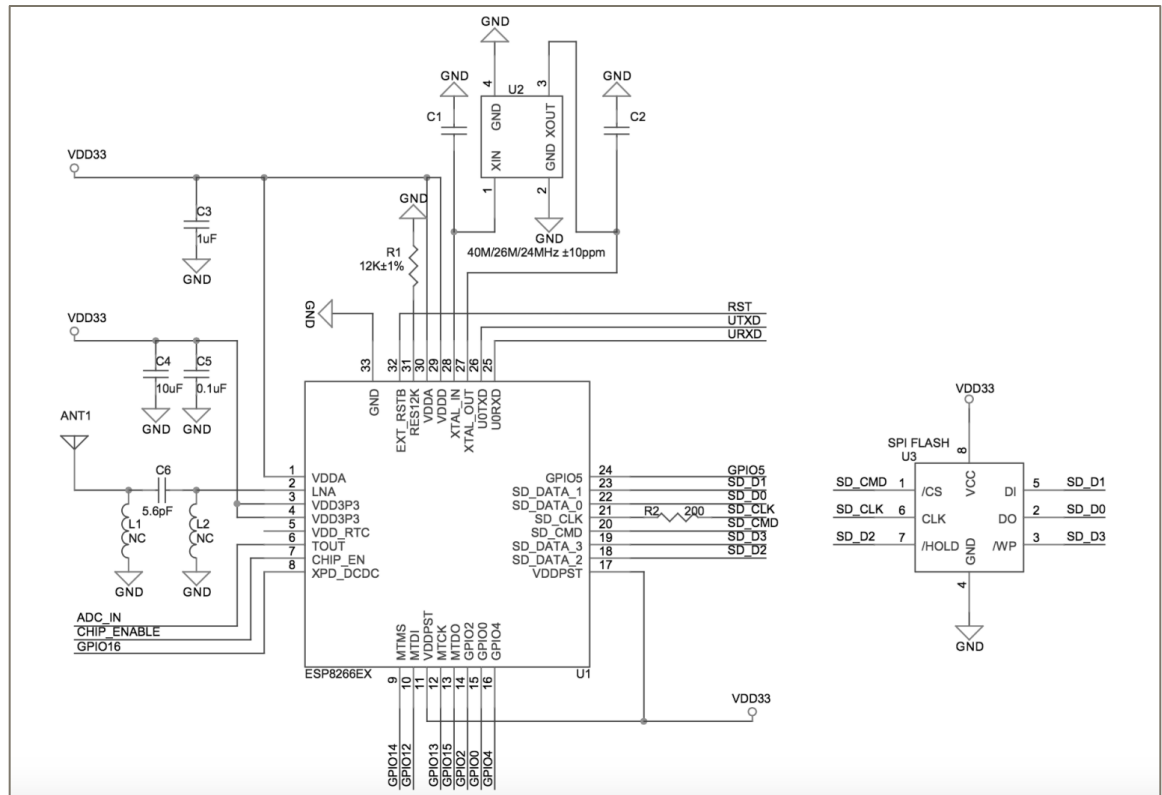


Figure 1-3. ESP8266EX Schematics

The ESP8266EX schematics include six aspects:

- Power supply
- Power-on sequence and reset
- Flash
- Crystal oscillator
- RF
- External resistor

1.4.1. Power Supply

Digital Power Supply

ESP8266EX has two digital pins for power supply, Pin11 and Pin17. For digital power supply, there is no need to add additional filter capacitors. The operating voltage range of digital power supply pins is 1.8V ~ 3.3V.

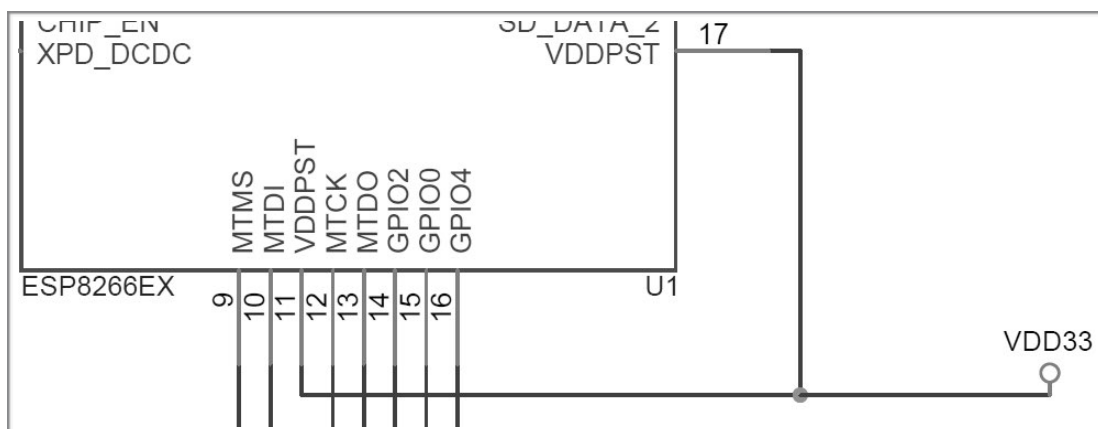


Figure 1-4. ESP8266EX Digital Power Supply Pins

Analog Power Supply

ESP8266EX has five analog pins for power supply, including Pin1, Pin3, Pin4 that are the power supply for internal PA and LNA; and Pin28, Pin29 for the internal PLL. The operating voltage for analog power supply pins is 1.8V ~ 3.3V.

Note that the power supply channel might be damaged due to the sudden increase of current when ESP8266EX is transmitting analog signals. Therefore, an additional 10 μ F capacitor with a 0603 or 0805 package is needed to match the 0.1 μ F capacitor in a 0402 package.

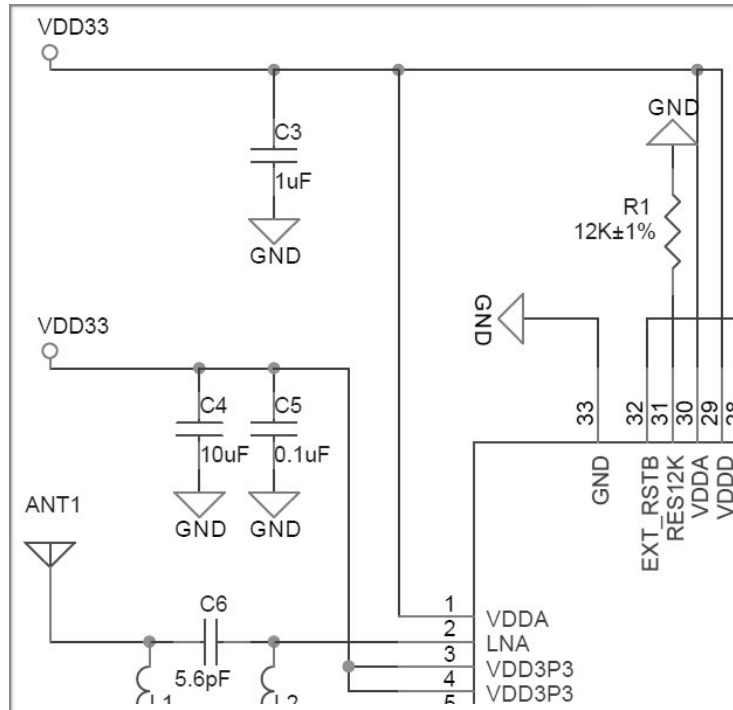


Figure 1-5. ESP8266EX AVDD

**Note:**

ESP8266EX's EMC is in conformity with FCC and CE requirements. There is no need to add ferrite beads in the analog power-supply circuit.

1.4.2. Power-on Sequence and Power Reset

Power-on Sequence

ESP8266EX uses a 3.3V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CH_EN (Pin7) by time T after the 3.3V rails have been brought up. The recommended delay time (T) is given by the parameter of the RC circuit. For reference design, please refer to Figure ESP-WROOM-02 Peripheral Schematics in the [ESP-WROOM-02 Datasheet](#).

Notice:

If CHIP_EN is driven by a power management chip, then the power management chip controls the ESP8266EX power state. When the power management chip turns on/off Wi-Fi through the high/low level on GPIO, a pulse current may be generated. To avoid level instability on CHIP_EN, an RC delay ($R=10\text{ k}\Omega$, $C=100\text{ nF}$) circuit is required.

Reset

Pin32 serves as an RST pin which can be left floating when it is not used. The reset pin is held low when the chip is enabled. In order to avoid resets caused by external interference, the lead is generally required to be short, and no external pull-up resistor is necessary.

Pin7 CH_EN can also be used as a reset pin. ESP8266EX will power off when CH_EN pin is held low and the input level is below 0.6V and stays for at least 200 μs .

Notice:

Pin7 CH_EN cannot be left floating.

1.4.3. Flash

The demo flash used on ESP8266EX is an SPI Flash with 2-MB ROM in an SOIC_8 (SOP_8) package. Pin21 SD_CLK is connected to the flash CLK pin together with a 0402 resistor in serial connection, which reduces the drive current and eliminates external interruption. The initial resistance of the resistor is 200 Ω .

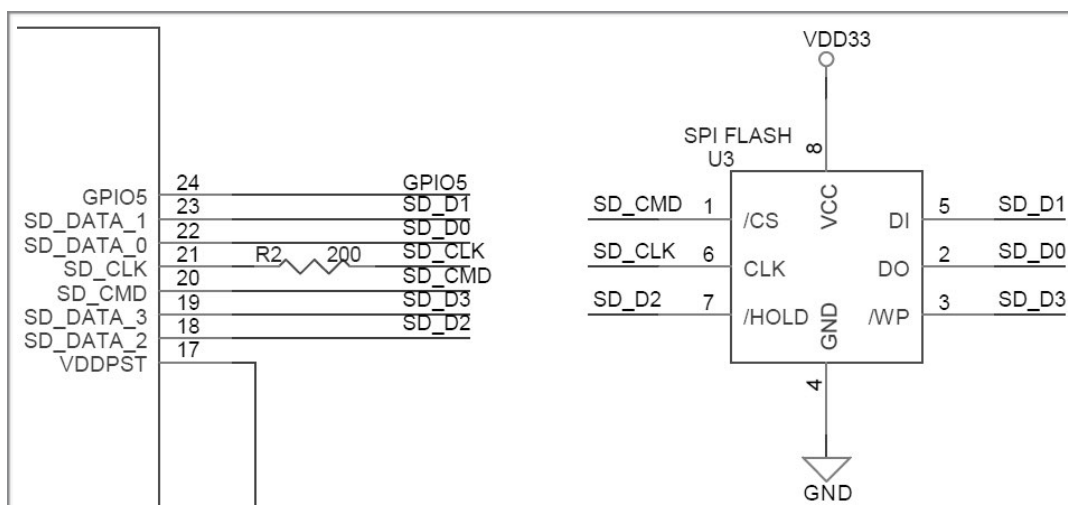


Figure 1-6. ESP8266EX Flash

1.4.4. Crystal Oscillator

ESP8266EX can support 40 MHz, 26 MHz and 24 MHz crystal oscillators. The accuracy of crystal oscillators should be ± 10 PPM, and the operating temperature range should be between -20°C and 85°C .

Please select the right type of crystal oscillator that is used in the ESP Flash Download Tool. In circuit design, capacitors C1 and C2, which are connected to the earth are added to the input and output terminals of the crystal oscillator respectively. The values of the two capacitors can be flexible, ranging from 6 pF to 22 pF. However, the specific capacitive values of C1 and C2 depend on further testing of and adjustment to the overall performance of the whole circuit. Normally, the capacitive values of C1 and C2 are within 10 pF if the crystal oscillator frequency is 26 MHz, while the values of C1 and C2 are 10 pF $< C1, C2 < 22$ pF if the crystal oscillator frequency is 40 MHz.

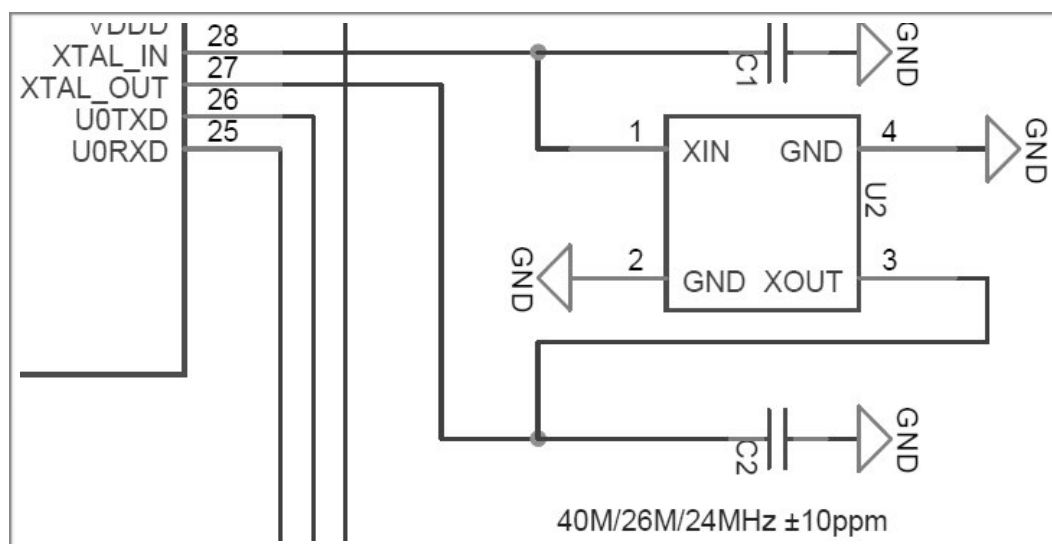


Figure 1-7. ESP8266EX Crystal Oscillator

**! Notice:**

Defects in the craftsmanship of the crystal oscillators (for example, high frequency deviation and unstable working temperature) may lead to the malfunction of ESP8266EX, resulting in the decrease of overall performance.

1.4.5. RF

The impedance of the ESP8266 PA output end is $(39+j6)\Omega$, so the matched impedance is $(39-j6)\Omega$ (from antenna to the chip).

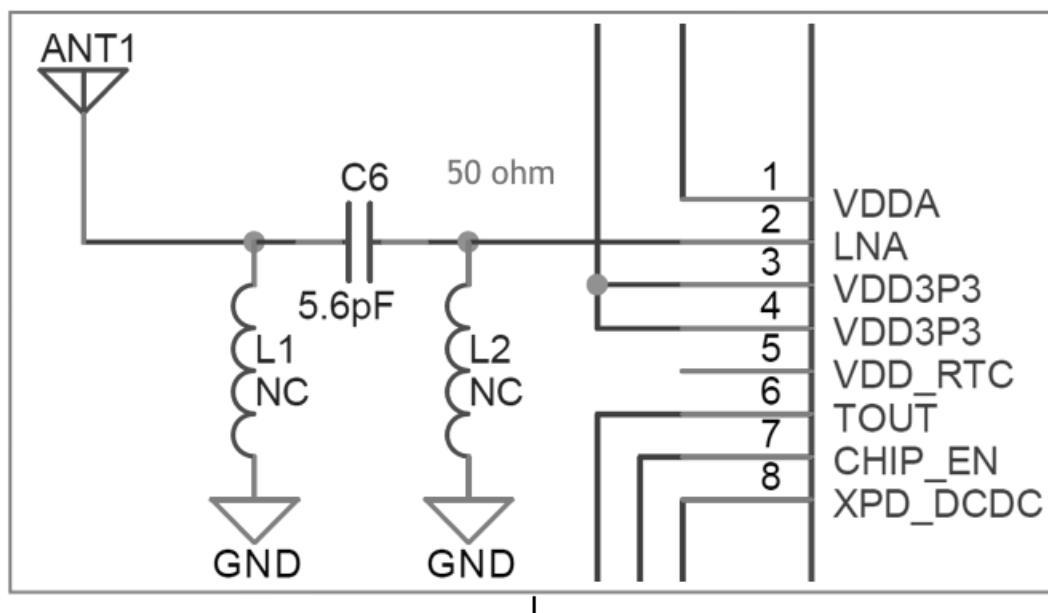


Figure 1-8. ESP8266EX RF

1.4.6. External Resistor 12K

An external ground resistor should be connected to the ERS12K pin (Pin31). The ground resistor requires high accuracy when controlling the bias current. An accuracy of $12K \pm 1\%$ is recommended.



Figure 1-9. ESP8266EX External Resistor



1.5. PCB Layout Design

The PCB layout design guidelines are applicable to cases when

- the ESP8266EX module functions as a standalone device, and when
- the ESP8266EX functions as a slave device.

1.5.1. Standalone ESP8266EX Module

Layout Design

The PCB has four layers:

- The first layer is the TOP layer for signal lines and components.
- The second layer is the GND layer, where no signal lines are laid to ensure a complete GND plane.
- The third layer is the POWER layer where only power lines can be placed. It is acceptable to place some signal lines under unavoidable circumstances.
- The forth layer is the BOTTOM layer. Only signal lines can be laid. Placing components on this layer is not recommended.

Power Supply Design

The 3.3V power lines are highlighted in yellow in Figure 1-10. The width of the power lines should be greater than 15 mil.

Before the power lines reach the analog power-supply pins (including Pin1, 3, 4, 28, 29) of ESP8266EX, a 10- μ F 0603 or 0805 capacitor (C6 in Figure 1-10) needs to be added. The capacitor should be placed close to the analog power-supply pins of the ESP8266EX.

Power lines should be placed on the third layer. When the power lines reach the pins of the chipset, vias are needed so that the power lines can go through the layers and connect to the pins of the chipset on the TOP layer. The diameter of the via holes should exceed the width of the power lines and the diameter of the drill should be a little larger than the radius of the vias.

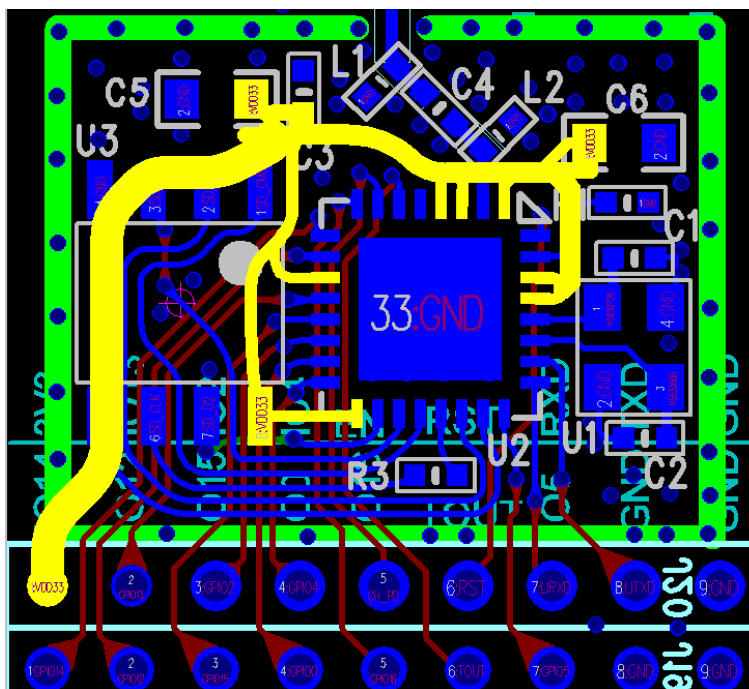


Figure 1-10. ESP8266EX PCB Layout

Crystal Oscillator Design

The crystal oscillator should be placed as close to the XTAL pins as possible (without the traces being too long). It is good practice to use via stitching around the clock trace for low ground-plane impedance.

There should be no vias on the input and output traces, which means the traces cannot cross layers. In addition, the input and output traces should not be routed over one another, not even on different layers.

Place the input and output bypass capacitors on the near left or right side of the chip. Do not place them on the traces.

Do not route high-frequency digital signal lines under the crystal oscillator. It is best not to route any signal line under the crystal oscillator. The larger the copper area on the top layer is, the better. As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, for example, power-switching converter components or unshielded inductors.

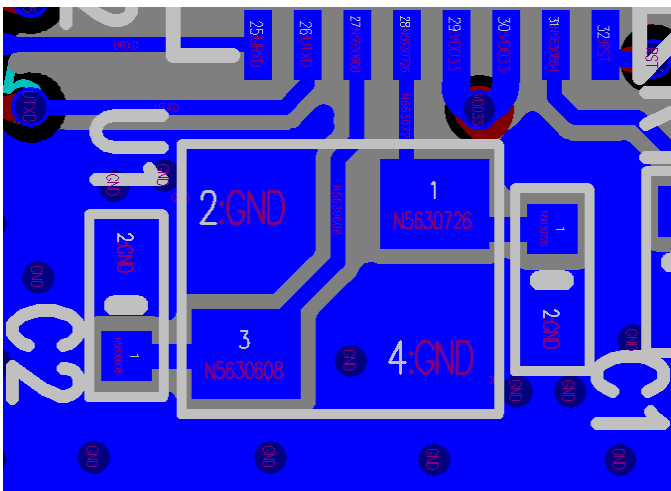


Figure 1-11. ESP8266EX Crystal Oscillators

RF Design

The characteristic RF impedance is 50Ω . The ground plane should be complete. The RF trace should be as short as possible with dense ground via stitching around it for isolation. The width of RF lines should be no less than 6 mil, while a width of over 10 mil is better.

π -type matching circuitry should be reserved on the RF trace and placed close to the RF pin.

There should be no vias for the RF trace. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.

The RF antenna should be set away from high-frequency transmitting devices, such as crystal oscillators, DDR, and certain high frequency clocks (SDIO_CLK, etc).

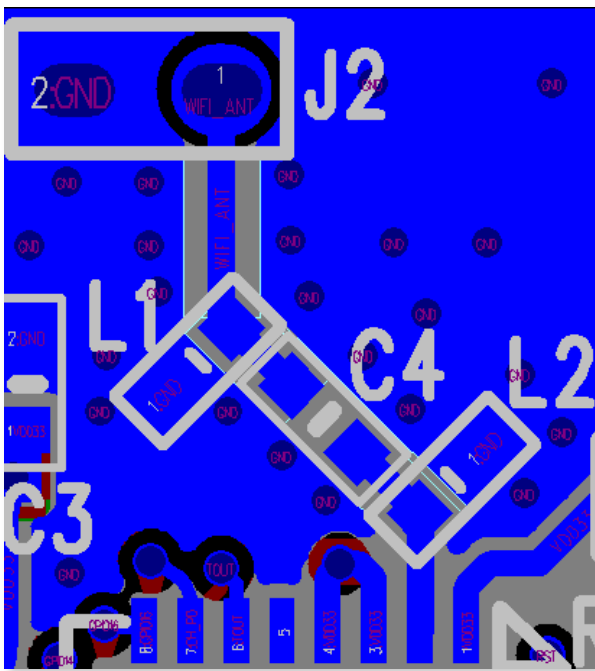
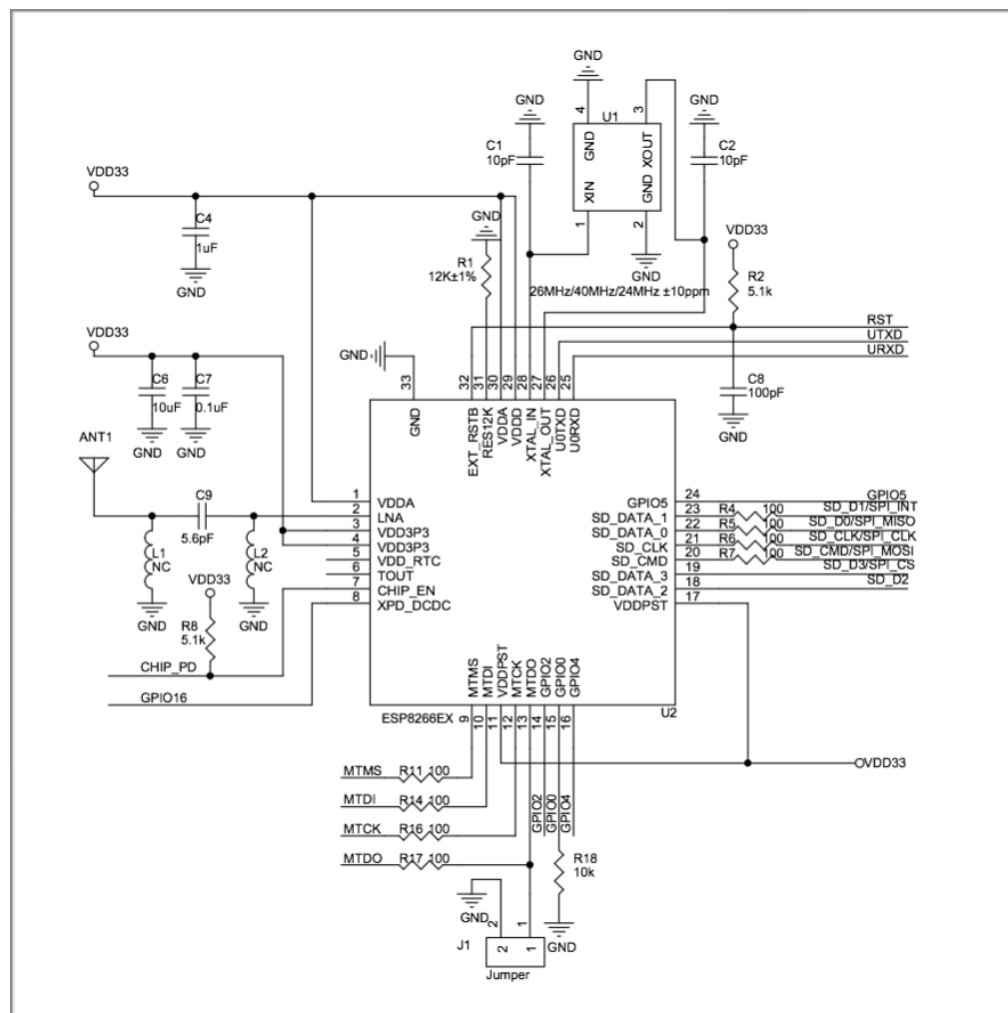


Figure 1-12. ESP8266EX RF



1.5.2. ESP8266EX as a Slave Device

When ESP8266EX works as a slave device in a system, users need to pay more attention to signal integrity in the PCB design. It is important to keep ESP8266EX away from the interferences caused by the complexity of the system and an increased number of high-frequency signals.



1. UART Download mode: short this jumper
2. SDIO Boot mode: disconnect this jumper

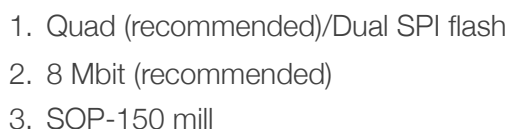


Figure 1-13. Schematics of ESP8266EX as a Slave Device

1. *CHIP_PD*, as an enable pin, should be connected to a GPIO of the host CPU.
2. *Dual SPI Flash (DIO/DOUT)*: Remove R12, R13, R15 and keep R10, R9.
3. *Quad SPI Flash (QIO/QOUT)*: Remove R9, R10 and keep R13, R12, R15.
 - a. *1 bit SDIO*: No need to connect SD_D2 and SD_D3 to the host.
 - b. *SPI*: SD_D3 is reused as SPI_CS and there is no need to connect it to the host.

We use the mainboard of a PAD or TV Box as an example here to provide guidelines for the PCB layout and design.





As shown in Figure 1-14, ESP8266EX should be placed near the edge of the PCB and away from the CPU and DDR, the main high-frequency noise sources. The distance between the chip and the noise sources decreases the interference and reduces the coupled noise.

It is suggested that a 200Ω series resistor is added to the six signal traces when ESP8266EX communicates with the CPU via SDIO to decrease the drive current and any interferences, and also to eliminate the sequencing problem caused by the inconsistent length of the SDIO traces.

On-board PCB antenna is not recommended, as it receives much interference and coupling noise, both of which impact the RF performance. We suggest that you use an external antenna which should be directed away from the PCB board via a cable, in order to weaken the high frequency interference with Wi-Fi.

The high-frequency signal traces between the CPU and associated memory should be routed strictly according to the routing guidelines (please refer to the DDR trace routing guidelines). CLK and data/addr lines should be laid underground.

The GND of the Wi-Fi circuit and that of other high-power devices should be separated and connected through wires if there are high-power components, such as motors, in the design.

The antenna should be kept away from high-frequency noise sources, such as LCD, HDMI, Camera Sensor, USB, etc.

1.5.3. Typical Layout Problems and Solutions

- **Q: The current ripple is not large, but the Tx performance of RF is rather poor.**

Analysis:

Ripple has a strong impact on the performance of RF Tx. It should be noted that ripple must be tested when ESP8266EX is in the normal working mode. The ripple increases when the power gets high. Generally, the ripple should be <80 mV when sending 11n MCS7 packets, and <120 mV when sending 11b packets.

Solution:

Add a $10\text{-}\mu\text{F}$ filter capacitor to the branch of source circuit (ESP8266EX AVDD pin). The $10\text{-}\mu\text{F}$ capacitor should be adjacent to the VDDA pin.

- **Q: The power ripple is small, but the Tx performance is poor.**

Analysis:

The RF Tx performance can be affected not only by power ripples, but also by the crystal oscillator itself. Poor quality and big frequency offsets (more than ± 40 ppm) of the crystal oscillator decrease the RF Tx performance. The crystal oscillator clock may be corrupted by other interfering signals, such as high-speed output or input signals. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:



This problem is caused by improper layout and can be solved by re-layout. See Section 1.5 for details.

- **Q: When ESP8266EX sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.**

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna.

Solution:

Match the antenna's impedance with the reserved π -type circuit on the RF trace, so that the resistance from the RF pin to the antenna approaches $(39-j6)\Omega$.

- **Q: TX performance is not bad, but the Rx sensitivity is low.**

Analysis:

Good Tx performance indicates proper RF impedance matching. External coupling to the antenna can affect the Rx performance. For instance, the crystal oscillator signal harmonics could couple to the antenna. If ESP8266EX serves as slave device, there will be other high-frequency interference sources on the board, which may affect the Rx performance.

Solution:

Keep the antenna away from crystal oscillators. Do not route high-frequency signal traces close to the RF trace.

1.6. Applications

1.6.1. UART to Wi-Fi Smart Device

The two UART interfaces are defined in Table 1-3.

Table 1-3. Pin definitions of UART Interfaces

Category	Pin definition	Function
UART0	(Pin 25) U0RXD+ (Pin 26) U0TXD	Receive and transmit user's data packages.
UART1	(Pin 14) GPIO2 (U1TXD)	Print information.

AT instruction and examples are provided here:

http://www.espressif.com/en/support/download/documents?keys=&field_type_tid%5B%5D=14

Application example: ESP8266EX development board (please see Chapter 2).



1.6.2. Sensor

ESP8266EX can be used for developing sensor products by using the I2C interface. The I2C works in the master mode and can connect to multiple sensors. The slave devices are identified through the addressing mode, as each slave device has a unique address.

The sensor products send real-time data to ESP8266EX via the I2C interface, and ESP8266EX uploads the data to the server wirelessly. Users can acquire information from the server through the mobile app when their mobile phones connect to the internet.

1.6.3. Smart Light

ESP8266EX can be used for developing such smart home products as smart light by using the PWM and infrared interfaces. The three PWM interfaces control red, blue, and green LEDs respectively. The minimal PWM duty ratio is $1/2^{14}$. In addition, the infrared interface allows specific control on LEDs, such as reset, power on/off, color switch, etc.

1.6.4. Smart Plug

ESP8266EX can be used for developing smart plug products. The GPIOs control the power switch through the high/low-level switch and connection/disconnection of relay. A smart plug requires three modules: 220V to 3.3V power conversion module, ESP8266EX Wi-Fi module and relay control module.



2. ESP-LAUNCHER

2.1. Overview

Espressif provides ESP8266EX development board—ESP-LAUNCHER for quick configuration and further development. The size of the board is 46 mm x 78.5 mm (see Figure 2-1).

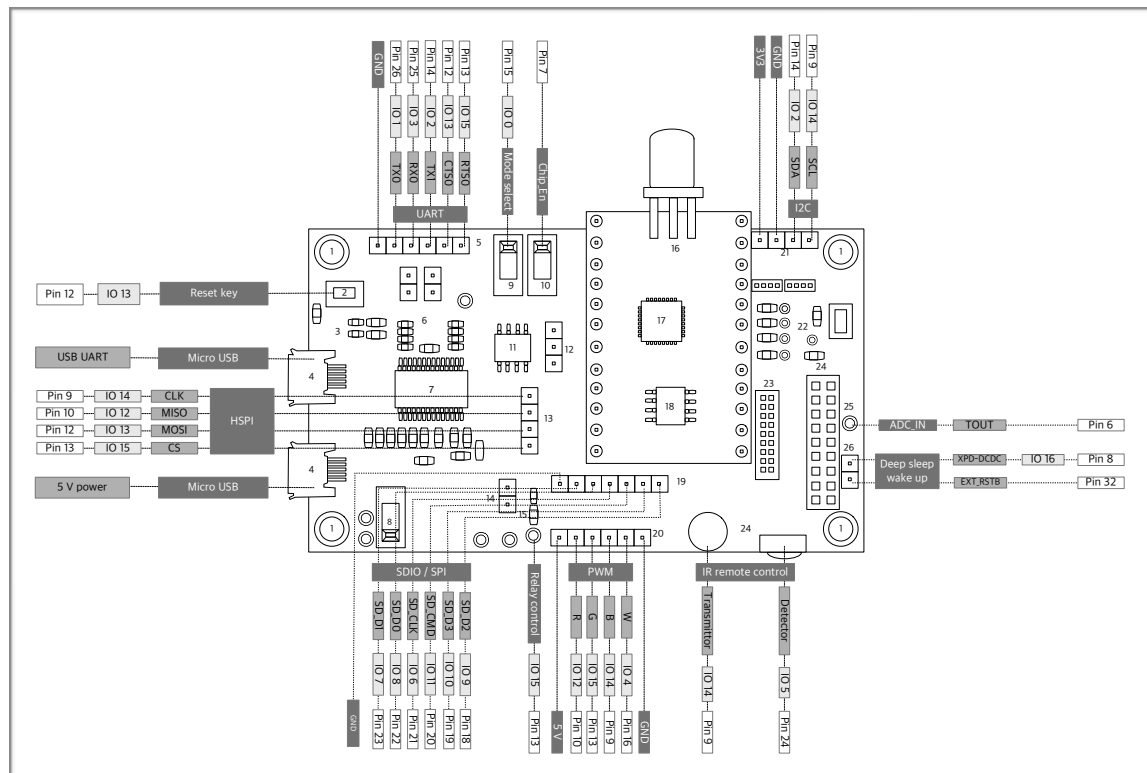


Figure 2-1. ESP-LAUNCHER

1 Location hole	8 5V power switch	15 Relay control	22 Undefined LEDs and keys
2 Reset key	9 IO0 control	16 SMA ANT	23 1.27 mm double pitch
3 Wi-Fi LED, Link LED	10 CH_EN switch	17 Test board	24 2.0 mm double pitch
4 Micro USB: USB-UART, 5V power	11 Flash2: HSPI	18 Flash1: SPI	25 ADC_IN
5 UART	12 CS of Flash2	19 SDIO/SPI	26 Deep-sleep wake up
6 UART SWAP	13 HSPI	20 IR_T, IR_R	
7 USB-UART chip	14 3.3V power	21 I2C	

ESP-LAUNCHER can be configured through USB serial or Wi-Fi connection. The modules/ interfaces integrated on the development board are described in Table 2-1 and 2-2.



Table 2-1. ESP-LAUNCHER Module Description

Module	Functional description
Micro USB interface	There are two USB interfaces. Both can be used as a 5V power supply or for serial communication (2-1-4).
Power supply	The USB interface provides 5V power supply which can be converted to 3.3V through a DC-to-DC converter. An LED light indicates the power, and a header pin is used for testing the power current.
Slide switch	<p>Three slide switches are used for the 5V power supply (2-1-8), GPIO0 voltage level switch (2-1-9) and chip enable pin CH_EN (2-1-10), respectively. When the switches are toggled to the outer side, the voltage level is high, while when the switches are toggled to the inner side, the voltage level is low.</p> <ul style="list-style-type: none">• For the 5V power switch:<ul style="list-style-type: none">- Toggled to the inner side, the board is powered on;- Toggled to the outer side, the board is powered off.• For the GPIO0 Control:<ul style="list-style-type: none">- Toggle to the inner side, the UART download mode is enabled and users can download firmware with ESP Flash Download Tool;- Toggle to the outer side, the Flash boot mode is enabled and the UART debug tool can be used for debugging.
Reset Key	SW1 is connected to MTCK (GPIO13) for application reset and clearing the Wi-Fi configuration (2-1-2). SW2 is not defined (2-1-22).
Indicator light	<ul style="list-style-type: none">• Red light (D2) indicates Wi-Fi work status (2-1-3).• Blue (D3) indicates communication with server (2-1-3)• Green light (D1) indicates relay switch control (2-1-15)• Blue light (D11) and red light (D10) indicate Rx and Tx work status, respectively (2-1-7)• Red light (D12) indicates a 5V power supply (2-1-8)• D4/13/14/16 are not defined (2-1-22).
Jumper	<ul style="list-style-type: none">• J82: It needs to be shorted by a jumper, so that the 3.3V power supply can be channeled into other circuits. It can also be used to test the power current (2-1-14).• J3: CS of HSPI flash. HSPI flash is disabled when the two upper pins are shorted by a jumper. HSPI flash is enabled when the two lower pins are shorted by a jumper (2-1-12).• J14 and J67: Short-circuit J14 to connect GPIO13 to U0CTS. Short-circuit J67 to connect GPIO15 to U0RTS (2-1-6).• J77: Short-circuit J77 to connect GPIO16 to EXT_RSTB for Deep-sleep wake up (2-1-26).
Interfaces	UART, HSPI, SDIO/SPI, I2C, ADC_IN, GPIO16, relay control, PWM and IR TX/RX
Flash	<ul style="list-style-type: none">• 32-Mbit Flash1 (mounted on the test board): Flash1 is connected to the chip via the SPI interface. Currently, Flash1 is used when the chip is working in the Wi-Fi standalone mode. R9 and R85 can be used for the CS of Flash1. By default, Flash1 is enabled (2-1-18).• 32-Mbit Flash2 (mounted on the baseboard): Flash2 is connected to the chip via the HSPI interface. HSPI is used in SIP mode. For the ESP-LAUNCHER, when ESP8266EX works as a slave device, it connects to the host MCU via the SPI interface that is defined in SDIO specifications. HSPI is connected to Flash2. J3 can be used for the CS of Flash2 (2-1-11).



Module	Functional description
Test modules	<p>There are multiple modules that can be connected to the ESP-LAUNCHER for testing and development, through the 1.27mm double-row pin headers (2-1-23) and 2.00 mm double-row pin headers (2-1-24).</p> <p>Please note that module pins should be connected to their corresponding pins on the board. Besides, only one module at a time can be used.</p>

Table 2-2: ESP-LAUNCHER interfaces

Interfaces	Function description
HSPI	It can interface SPI flash (Flash2), display screen, MCU, etc (2-1-13).
SDIO/SPI	It can interface flash, host MCU, display screen, etc (2-1-19).
PWM	Currently the PWM interface has four channels, and users can extend the channels as needed. The PWM interface can be used to control LED lights, buzzers, relays, motors, etc (2-1-20).
IR	The functionality of the infrared remote control interface can be implemented via software programming. NEC coding, modulation and demodulation are used by this interface. The frequency of the modulated carrier signal is 38 KHz (2-1-24).
ADC	The interface is used to test the power supply voltage of VDD3P3 (pin3 and pin4), as well as the input voltage of TOUT (pin6). It can also be used in sensors (2-1-25).
I2C	It can interface sensors and display screens with 2.54 mm or 1.27 mm pin headers (2-1-21).
UART	<p>UART0: U0TXD, U0RXD, MTDO (U0RTS), MTCK (U0CTS) UART1: GPIO2 (U1TXD) It can interface other UART devices (2-1-5).</p> <ul style="list-style-type: none">• For firmware downloading: U0TXD+U0RXD or GPIO2+U0RXD• For communication: UART0: U0TXD, U0RXD, MTDO(U0RTS), MTCK(U0CTS)• For debugging: UART1_TXD (GPIO2) can be used to print debugging information. <p>By default, UART0 will output some printed information when the device is powered on. For the applications that are sensitive to this feature, users can exchange the pins of UART during system initialization, that is, exchange U0TXD, U0RXD with U0RTS, U0CTS. R1/3/5/7 should not be mounted with other components, while R2/4/6/8 can be mounted with other components. J14 and J67 should be shorted.</p>
Relay control terminal	It is used to control, with an indicator light, the on-and-off switch of the relay in a smart plug application (2-1-15).

To use the SDIO/SPI interfaces on ESP-LAUNCHER, please follow the steps below:

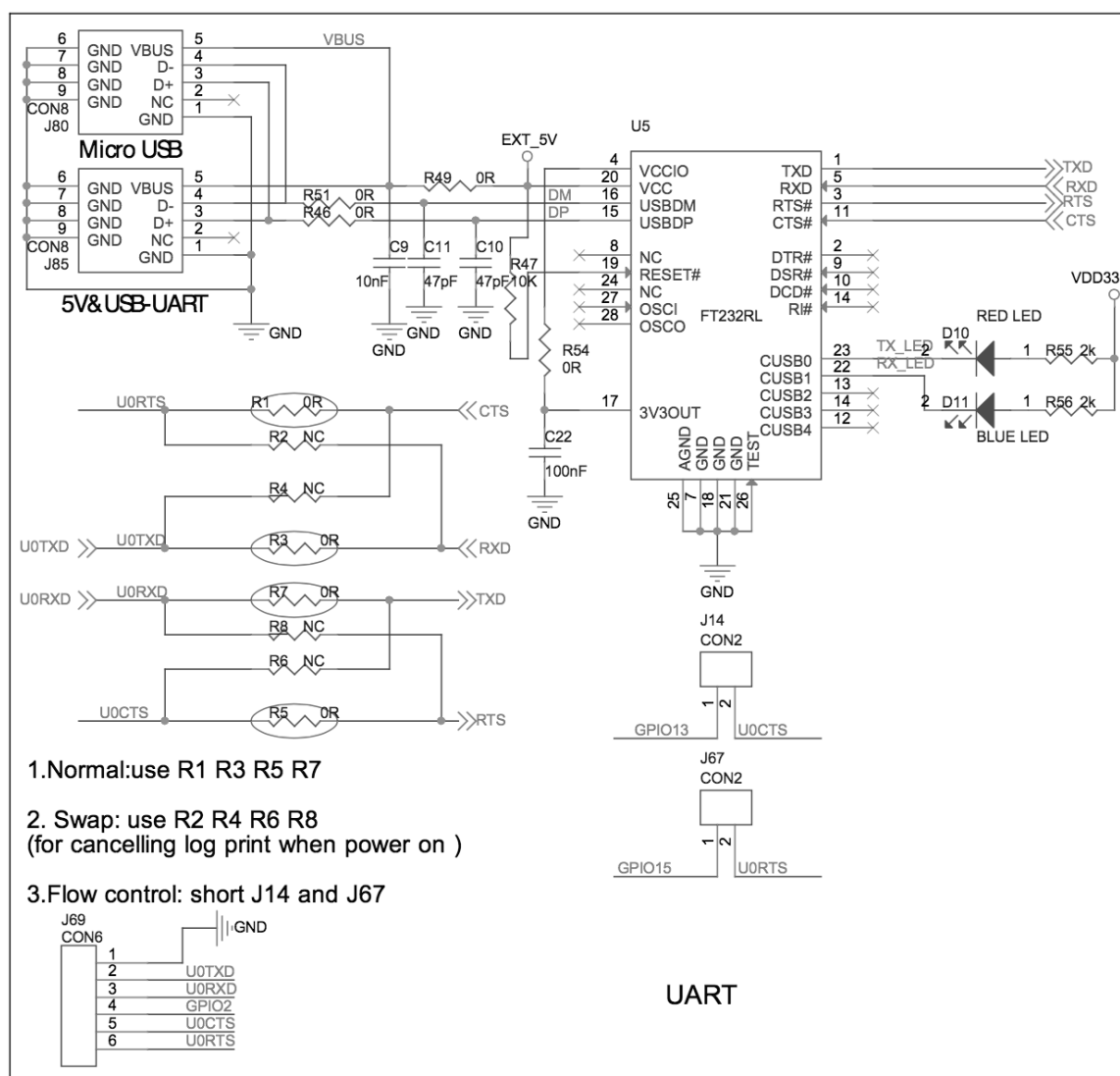
1. Move the 0R at R85 to R9, and then disable the flash on the ESP_Test Board;
2. Short-circuit the two lower pins on J3 with a jumper to enable HSPI flash;
3. Remove C8 (next to the Reset key on the left of the PCB);
4. Remove R58 on the PCB and disconnect GPIO14 with the infrared transmitting tube;



5. Remove the pull-down resistor R29 of MTDO/IO15 (next to J11);
6. When downloading firmware, pull the IO15/CS at J11 to low level and toggle the switch of GPIO0 inwards to enable UART Download mode;
7. When downloading is completed, release IO15/CS to enable SDIO Boot mode;
8. Connect SDIO/SPI at J5 to host for communication.

2.2. Schematics

2.2.1. Interfaces



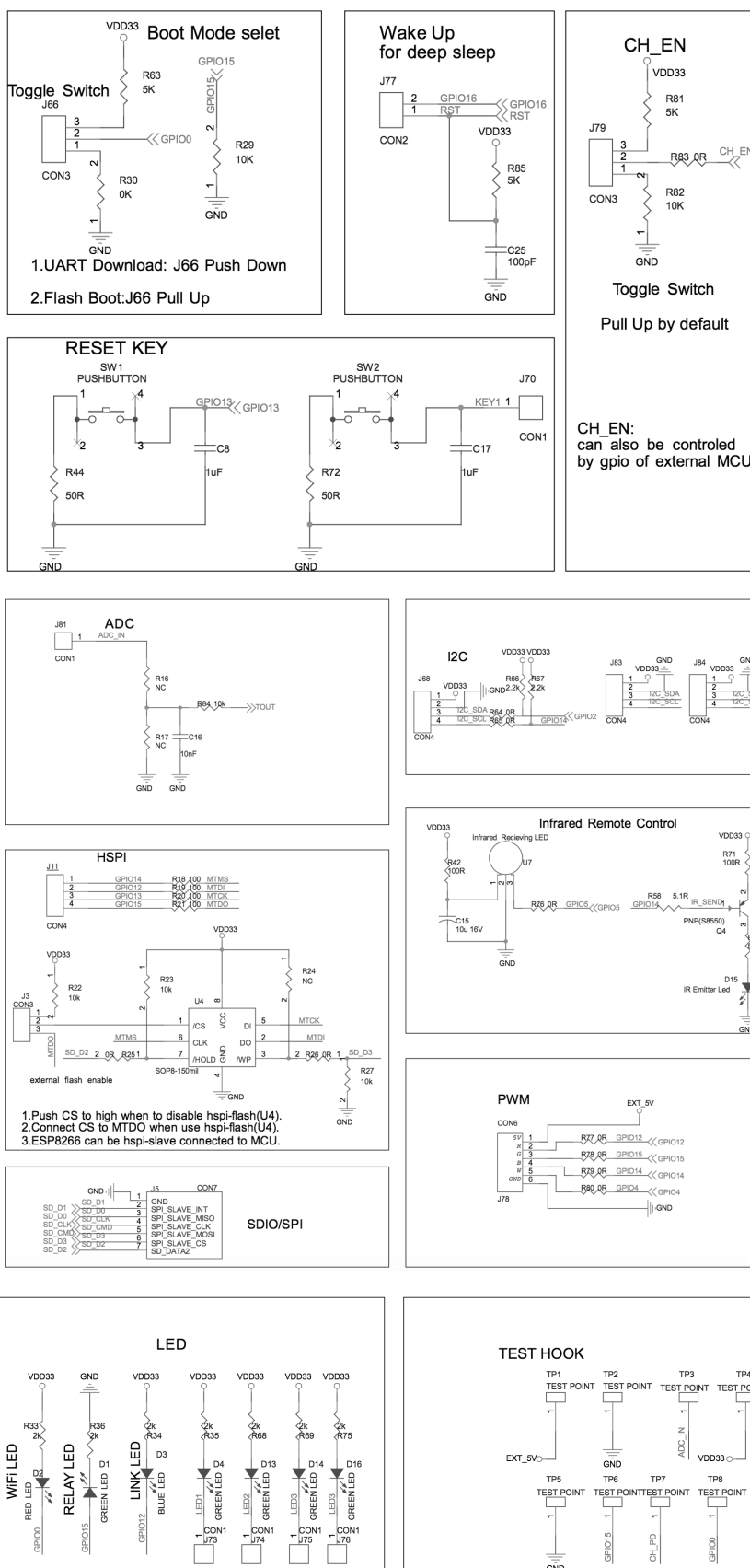
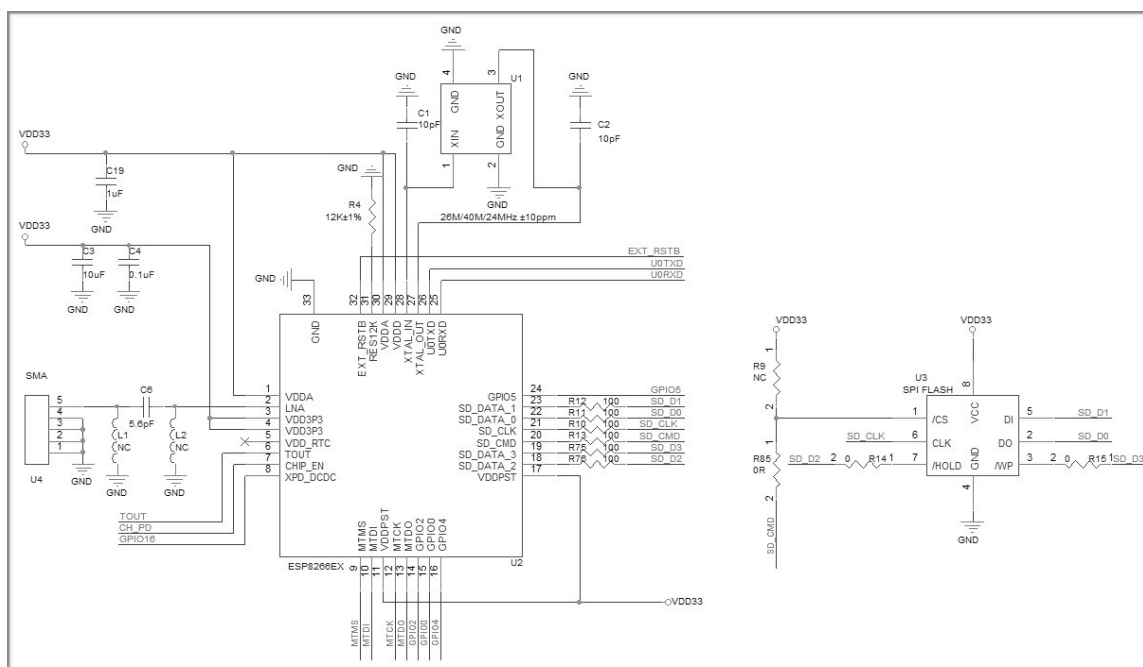
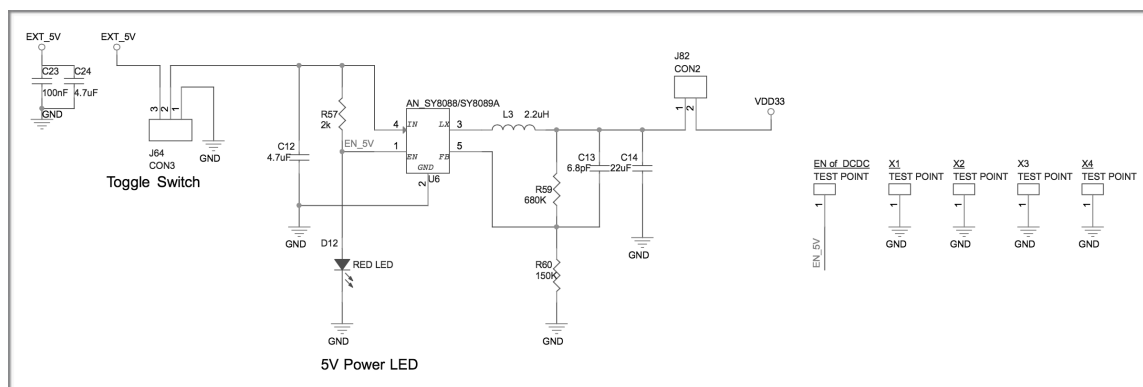


Figure 2-2. ESP-LAUNCHER Interface Schematics



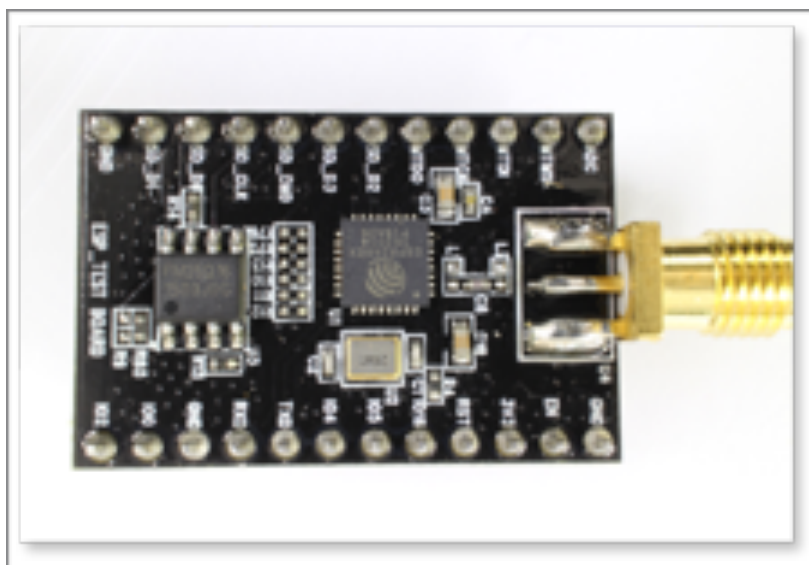


Figure 2-5. ESP-LAUNCHER Test Board

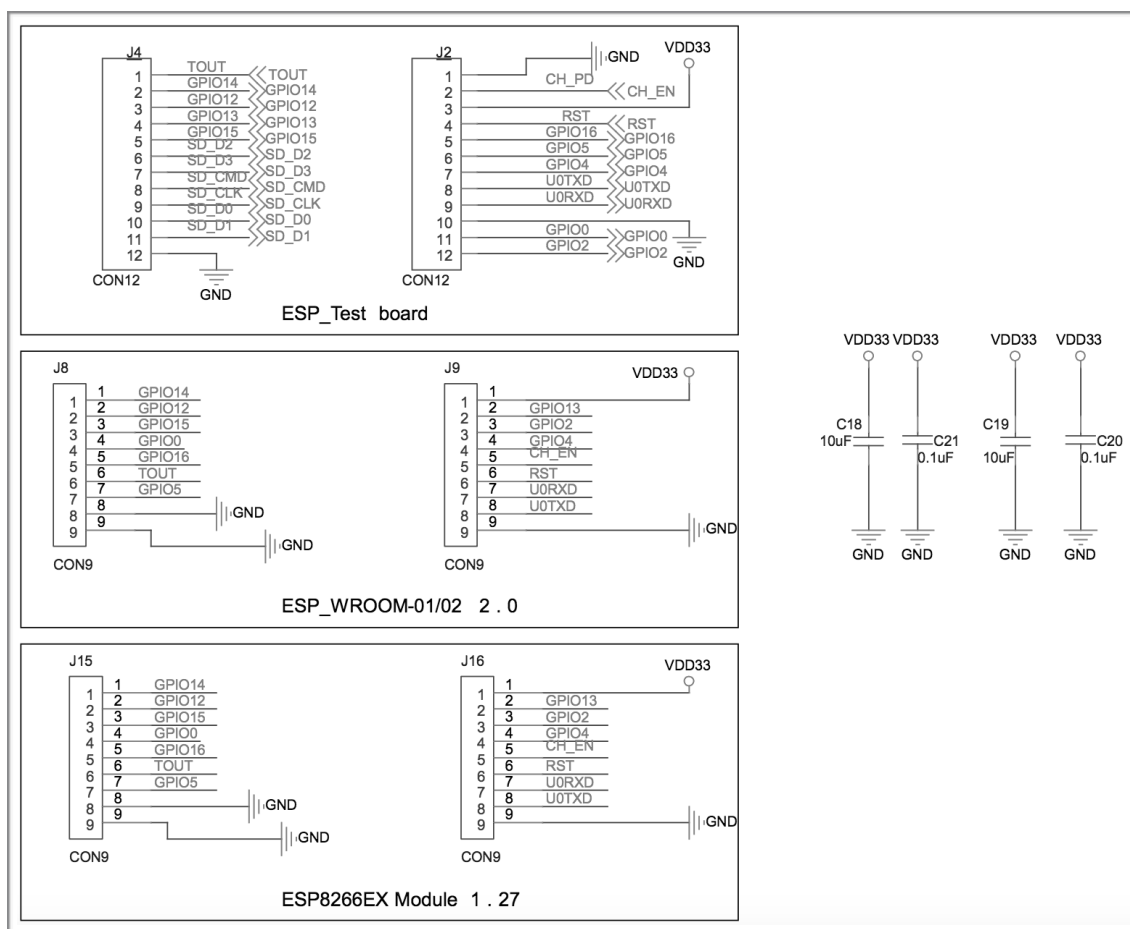


Figure 2-6. ESP-LAUNCHER Test Board Schematics



3.

ESP-WROOM

Espressif provides two types of modules, the SMD module (ESP-WROOM-02) and the DIP module (ESP-WROOM-01). The modules have been improved to achieve the optimum RF functionality. It is recommended that users use these modules for testing or further development.

3.1. SMD Module—ESP-WROOM-02

The pin distribution of the SMD Module is illustrated in Figure 3-1. The size of the module is $18 (\pm 0.2)$ mm x $20 (\pm 0.2)$ mm. The type of flash used on this module is an SPI flash with a package of SOP8-150 mil. The antenna used for this module is a 2-dBi PCB-on-board antenna.

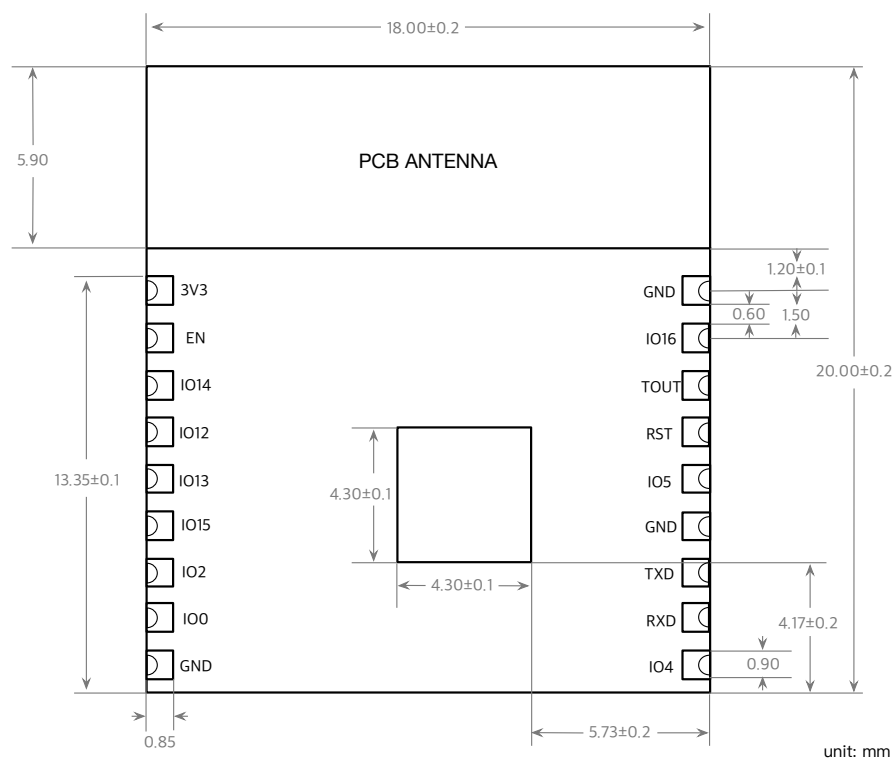
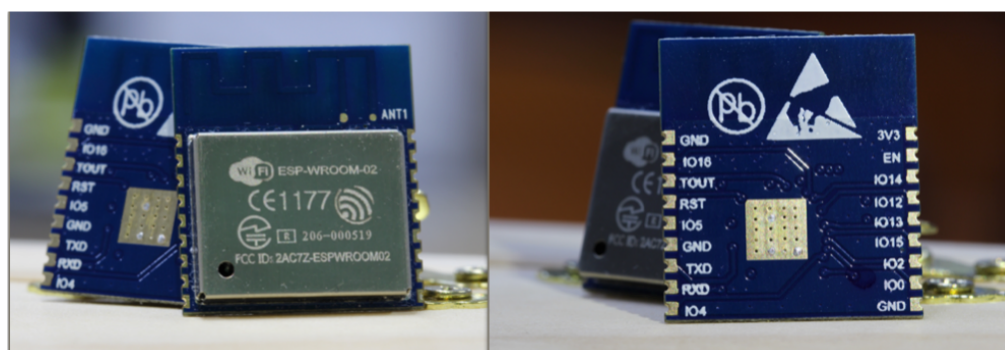


Figure 3-1. Top View of ESP-WROOM-02



There are altogether 18 pinouts. The pin distribution and definitions are listed in Table 3-1 below:

Table 3-1. ESP-WROOM-02 Pin Definitions

No.	Pin Name	Functional Description
1	3V3	3.3V power supply (VDD) Note: <i>It is recommended the maximum output current a power supply provides be of 500 mA or above.</i>
2	EN	Chip enable pin. Active high.
3	IO14	GPIO14; HSPI_CLK
4	IO12	GPIO12; HSPI_MISO
5	IO13	GPIO13; HSPI_MOSI; UART0_CTS
6	IO15	GPIO15; MTDO; HSPI_CS; UART0_RTS Pull down.
7	IO2	GPIO2; UART1_TXD Floating (internal pull-up) or pull up.
8	IO0	GPIO0 • UART download: pull down. • Flash boot: floating or pull up.
9	GND	GND
10	IO4	GPIO4
11	RXD	UART0_RXD, receive end in UART download; GPIO3
12	TXD	UART0_TXD, transmit end in UART download, floating or pull up; GPIO1
13	GND	GND
14	IO5	GPIO5
15	RST	Reset
16	TOUT	It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin6). These two functions cannot be used simultaneously.
17	IO16	GPIO16; used for Deep-sleep wake-up when connected to RST pin.
18	GND	GND

**Notes:**

1. The SMD module uses one single pin as the power supply pin. Users can connect the module to a 3.3V power supply. The 3.3V power supply works both for the analog circuit and the digital circuit.
2. The EN pin is used for enabling the Wi-Fi functionality. Set the EN pin high for normal working mode.
3. The SMD module features two working modes: the UART Download mode and the Flash Boot mode. In the UART Download mode, firmware can be downloaded into the flash memory or the internal memory by configuring the flash download tool. If the firmware is burnt into the internal memory, it can only run this time when the module is powered on. Once the module is powered down, the internal memory will clear up. However, if the firmware is burnt into the flash, it will be stored and can be recalled at any time.
4. Lead the GND RXD TXD pins out and connect them to a USB-to-TTL tool (FT232R is recommended) for firmware download, log-printing and communication.
5. During the whole process, users can check the status of the chip with the log printed through UART. If the firmware cannot be downloaded or executed, users can check if the working mode is normal during the chip initialization by looking at the log.
6. The serial tool cannot be opened for both the log-print and flash-download tools simultaneously.

By default the flash is empty. To download firmware into flash, please follow the steps below:

1. Pull IO15 and IO0 low, and leave IO2 floating to set the module to work in the UART Download mode.
2. Download the firmware into flash with ESP Flash Tool. For more information, please refer to [ESP8266 SDK Getting Started Guide](#).
3. After downloading the firmware into Flash, pull down IO15 to low, keep IO2 floating, and pull up IO0 to high. The module is then shifted from the UART Download mode to the Flash Boot mode.
4. Power on the chip, and the firmware will be read and executed during initialization.

3.2. DIP Module—ESP-WROOM-01

The size of the DIP module is 18 mm x 19 mm. The Flash type applied is an SPI flash packed in SOP8-150 mil. The antenna used is a 1-dBi metal antenna. The 2.00 mm pin headers can be either vertical or horizontal, depending on specific applications. Please refer to Table 3-1 for pin definitions of this module.

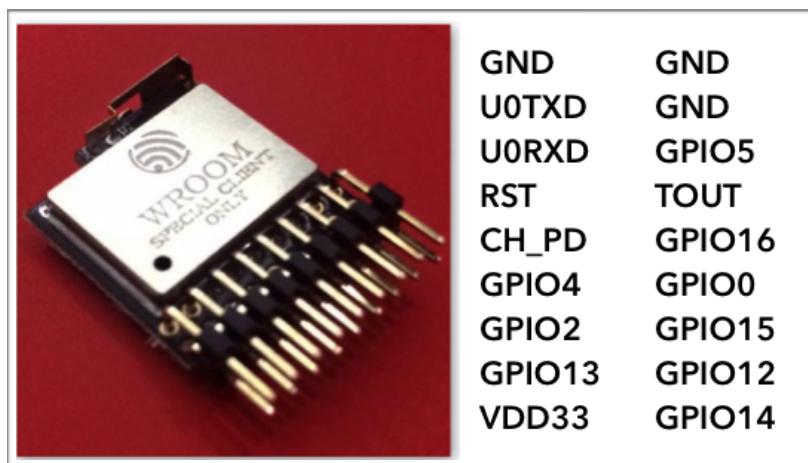


Figure 3-2. ESP-WROOM-01

Notice:

The DIP metal antenna is thin and prone to distortion. Change the antenna immediately if the shape and appearance are abnormal.

3.3. Schematics

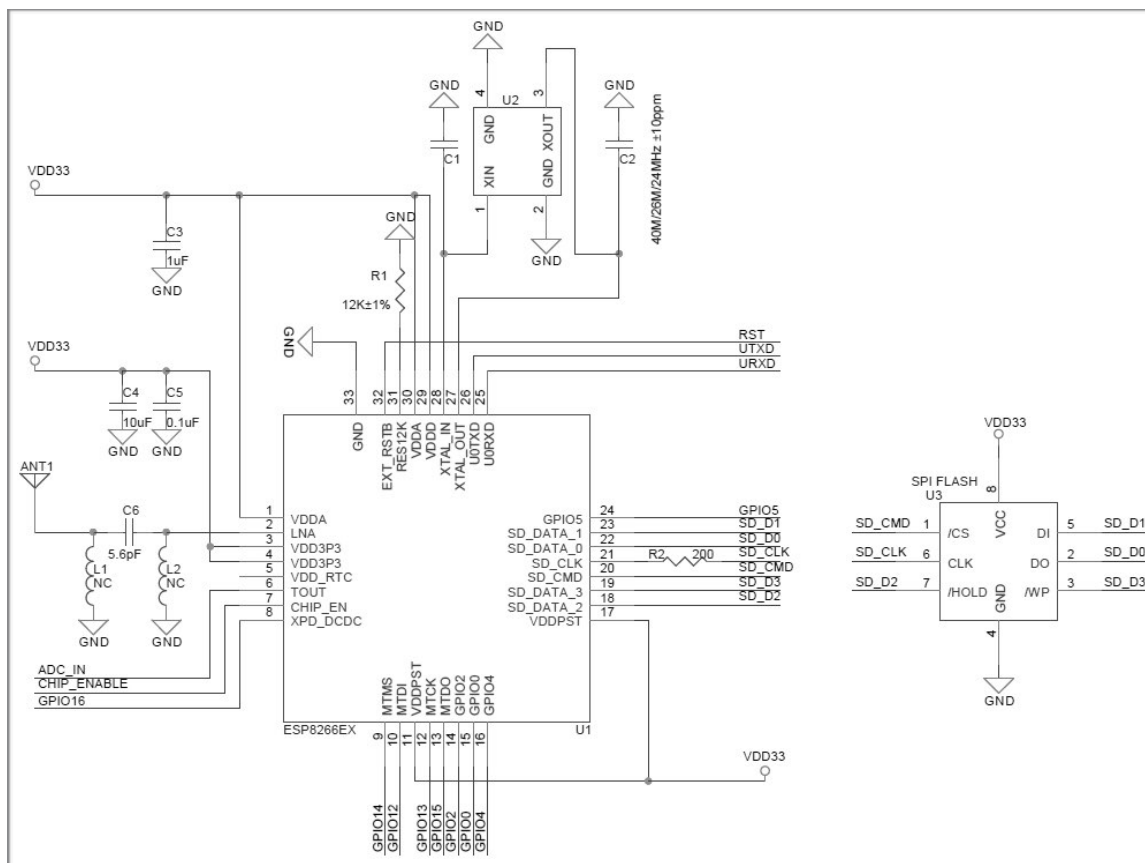


Figure 3-3. ESP-WROOM Schematics



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