NovTech System On Chip

NOVSOM™i.MX6x

User's Guide

Document Number: NOVSOM_iMX6x_001

Rev. 0.1

08/2012

Contact Information:

Home Page:
www.novtech.com

E-mail:
sales@novtech.com

USA/Europe or Locations Not Listed:
11788 W. Sample Road, Suite 105
Coral Springs, FL 33067
United States
+1-(888) 701-7466 or
+1-(954) 341-3320
sales@novtech.com

Canada:
429 St. Clements Ave.
Toronto, ON M5N-1M2
Canada
+1-(418) 807-6646
gkatz@novtech.com

Europe, Middle East, and Africa:
30 HaShahar St.
Ra'anana, 43565
Israel
+972 (0)52-830-8870
gguy@novtech.com

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About This Document

This manual explains how to implement and develop for the NOVSOM™ i.MX6x.

Audience

This manual is intended for software, hardware, and system engineers who are planning to use the NOVSOM™ i.MX6x.

Revision History

2012.08 Ver 0.1

Related Documents

FREESCALE IMX6DQRM (www.freescale.com), Rev. D, 08/2012

FREESCALE IMX6DQAEC or IMX6DQCEC (www.freescale.com)

FREESCALE IMX6QDCE (www.freescale.com)

NOVPEK™ i.MX6x UM

Acronyms and Abbreviations

The following acronyms and abbreviations are used in this manual. This list does not include signal, register, and software mnemonics.

B2B	Board to Board
CPU	Central Processing Unit
CSPI	Serial Peripheral Interface
DDR	Double Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input/Output
I2C	Inter-integrated Circuit
I/O	Input/Output
JTAG	Joint Test Access Group

MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card
OTG	On the go
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on reset
RAM	Random access memory
SD	Secure digital (smart media)
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus

1. General Information

The NOVSOM™ resolves some of the biggest challenges faced by designers when working with the SoC, such as:

- ✓ DDR Routing
- ✓ Boot Configuration
- ✓ Dense Routing of BGA Packages,
- ✓ High Board Layer Count

All while maintaining the full flexibility available on the SoC. A key element of the SoC is the IOMUXING and the voltage options for different IO groups. All of these are available on the NOVSOM™.

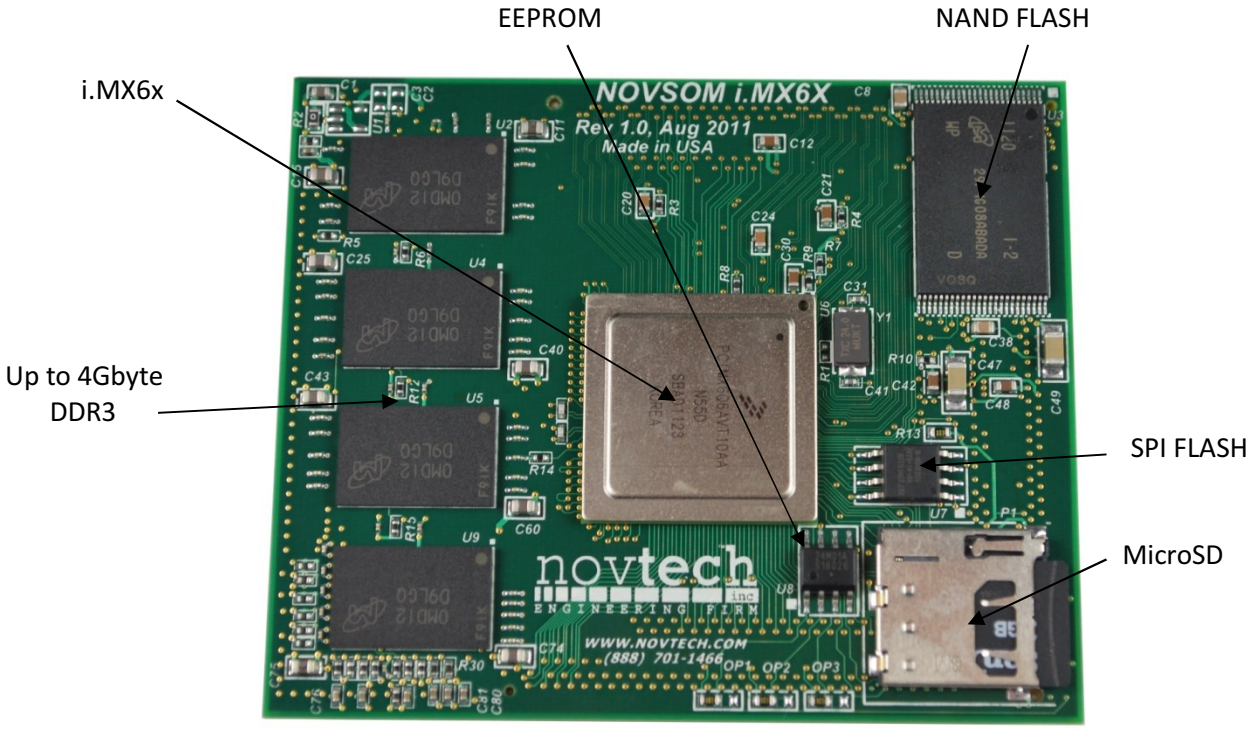


Figure 1 - Top view of the NOVSOM™ i.MX6x

Table 1 - Specifications

Characteristic	Specifications
Clock	Up to 1.2GHz
Temperature: Operating Storage	 -40°C to +85°C -40°C to +85°C
Relative Humidity	0 to 90% (non-condensing)
Power Requirements	Requires Power Management
Dimension	2.83 inch x 2.33 inch

2. SoM Details

The heart of the NOVSOM™ is the i.MX6x SoC, in addition, the NOVSOM™ includes the following:

2.1 SoC

The NOVSOM™ can support these variants of the i.MX6x Series: i.MX6 Quad, i.MX6 Dual, i.MX6 DualLite and i.MX6 Solo.

2.2 Boot Configuration

2.2.1 Setting Pins

There are two setting pins that need to be set correctly to allow the SoC to boot, the JTAG_MOD pin (SoC ball h6) and TEST_MODE pin (SoC ball E12). Both signals are pulled low via a 10K resistor.

2.2.2 Mode Pins

There are two BOOT_MODE pins on the SoC (see section 7.2.1 of the i.MX6x UM), both signals are pulled low via a 10K resistor and are routed to the B2B connectors allowing the user to change their setting on the carrier board. Pulling the signal via a 1K resistor on the carrier board will set the logic level of the signal to 'high'.

2.2.3 Bootstrap Pins

All bootstrap pins are available via the B2B connectors, please review section 7.3.2 of the i.MX6x UM for the proper setting to meet your design requirements.

2.3 Clocking

2.3.1 XTAL

A 24MHz crystal is connected to this clock interface on the NOVSOM™.

2.3.2 RTC_XTAL

A 32.786KHz crystal is connected to this clock interface on the NOVSOM™. A path is provided to use a clock signal from the carrier board to feed this clock, please consult with NovTech for this option.

2.3.3 CLK1 (P/N)

CLK1 is a differential I/O clock, both signals are routed to the B2B. Please consult the i.MX6 UM for proper usage.

2.3.4 CLK 2 (P/N)

CLK2 is a differential I/O clock, both signals are routed to the B2B. Please consult the i.MX6 UM for proper usage.

2.4 Board to Board Connectors

There are three B2B connectors that connect the NOVSOM™ to the carrier board, they carry all dedicated peripheral signals, all IOMUX signals and all Power signals, see section 4.0 for mechanical information and section 5.0 for the pinout assignment.

2.5 Unexposed Pins

The following signals that reside on the i.MX6x SoC are not exposed on the NOVSOM™ B2B connectors:

- DDR Signals.
- 24 MHZ Crystal Pins (XTAL), SoC Balls A7 & B7.
- JTAG Mode Pin, SoC Ball H6.
- SoC Test Mode Pin, SoC Ball E12.
- GPANAIO, left unconnected on NOVSOM, SoC Ball C8.
- FA_ANA, left unconnected on NOVSOM, SoC Ball A5.
- SATA_REXT Pin, on-board 191 Ohm Resistor to Ground, SoC Ball C14.
- HDMI_REXT Pin , on-board 1.6K Resistor to Ground, SoC Ball J1.
- DSI_REXT Pin, on-board 6.04K Resistor to Ground, SoC Ball G4.
- PCIe_REXT Pin, on-board 200 Ohm Resistor to Ground, SoC Ball A2.
- CSI_REXT Pin, on-board 6.04K Resistor to Ground, SoC Ball D4.
- VDD_FA, left unconnected on NOVSOM, SoC Ball B5.

2.6 Power Scheme

All Power Rails of the SoC are routed to the B2B Connectors, the following power rails are being filtered on the NOVSOM™:

2.7 DDR

The NOVSOM™ has eight DDR3 memory chips, 16-bit width each, to provide a maximum of 4Gbyte. The DDR3 can be run up to a maximum specified clock speed of 528MHZ (tested up to 675MHZ).

2.8 On SoM Booting Options

2.8.1 SD Card

The NOVSOM™ SD supports board booting via the i.MX6x SD1 interface. The carrier board pin-strapping needs to be set for this boot option (unless fuses had been programmed for this option and boot mode for set to '00'). Please note that the SD1 interface pins are routed to the B2B connector and can be used in the PINMUXING scheme if this boot option is not selected. The SD is powered by the NVCC_SD1 power rail and it needs to be set to 3.3V if this option to be used.

2.8.2 NAND FLASH

The NOVSOM™ NAND FLASH supports board booting via the i.MX6x NAND/EIM interface. The carrier board pin-strapping needs to be set for this boot option (unless fuses had been programmed for this option and boot mode for set to '00'). Please note that the NAND/EIM interface pins are routed to the B2B connector and can be used in the PINMUXING scheme if this boot option is not selected. The NAND FLASH is powered by the NVCC_SD4 and NVCC_NANDF power rails and it needs to be set to 3.3V if this option is used. A custom option of using a 1.8V NAND is available, please consult with NovTech for this option.

2.8.3 SPI FLASH

The NOVSOM™ SPI FLASH supports board booting via the i.MX6x SPI interface that is MUXED with EIM BUS pins (eCSPI1 MISO <- EIM_D17, eCSPI1 MOSI <- EIM_D18, eCSPI1_SCLK <- EIM_D16 & eCSPI1 SS0 <- EIM_D19). The carrier board pin-strapping needs to be set for this boot option (unless fuses had been programmed for this option and boot mode for set to '00'). Please note that the EIM interface pins are routed to the B2B connector and can be used in the PINMUXING scheme if this boot option is not selected. The SPI FLASH is powered by the NVCC_EIM_SEC and NVCC_EIM2 power rails and it needs to be set to 3.3V or 2.8V if this option is used.

2.8.4 EEPROM

The NOVSOM™ EEPROM supports board booting via the i.MX6x I2C interface that is MUXED with EIM BUS pins (I2C SCL <- EIM_D17, I2C SDA <- EIM_D18). The carrier board pin-strapping needs to be set for this boot option (unless fuses had been programmed for this option and boot mode for set to '00'). Please note that the EIM interface pins are routed to the B2B connector and can be used in the PINMUXING scheme if this boot option is not selected.

The EEPROM is powered by the NVCC_EIM_SEC and NVCC_EIM2 power rails and it needs to be set to 3.3V or 2.8V if this option is used.

2.9 Additional Booting Options

The following are additional booting options that can be used with the NOVSOM™, please note that these need to be implemented on the carrier board.

- NOR FLASH
- OnNAND FLASH
- SD CARD on SD2, SD3 or SD4
- SATA

2.10 Minimal Requirement to Boot the NOVSOM™

In order to boot the NOVSOM™, the carrier board, at minimum, needs to drive the following signals:

- All Power Rails of the SoC with the correct sequencing.
- Reset signal, nPOR and ONOFF.
- Boot strapping options set correctly.
- Optional: UART1 for terminal messages.

3. Mechanical

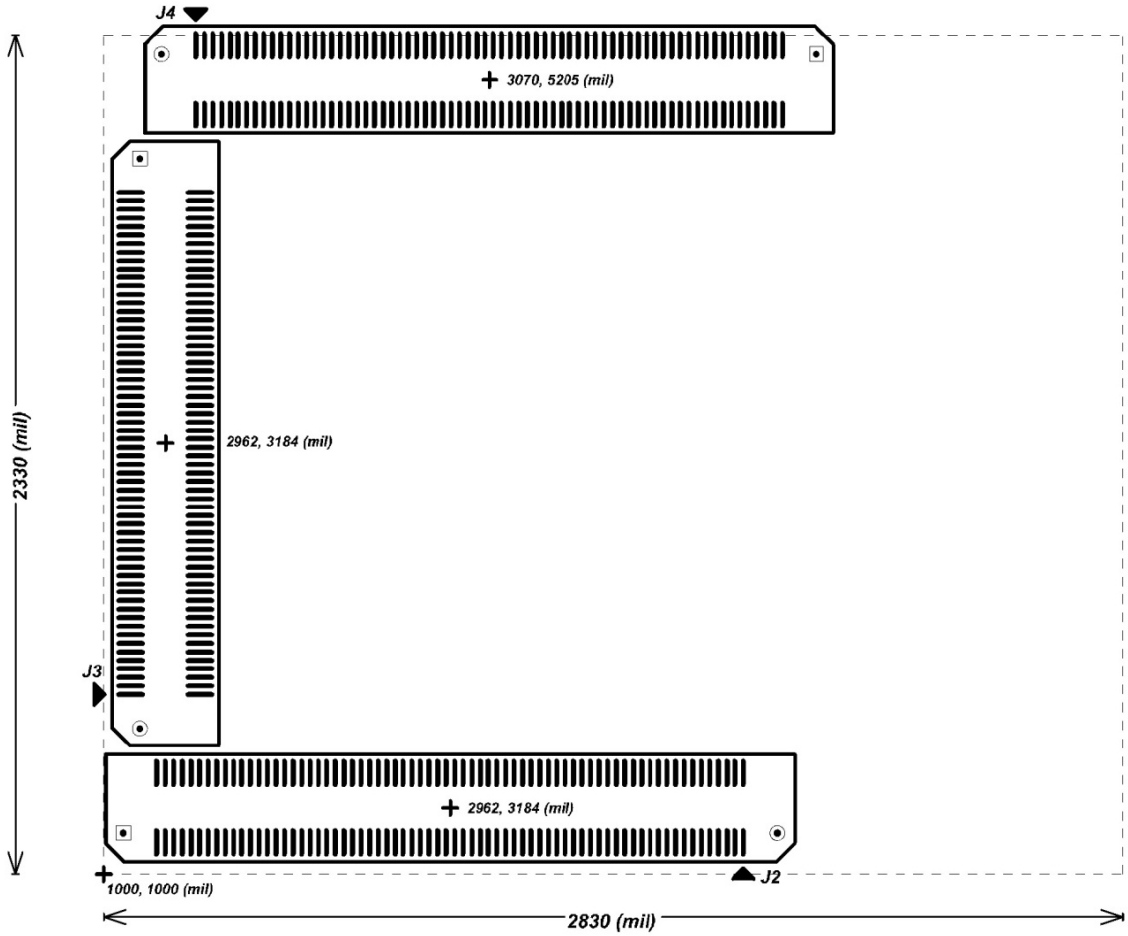


Figure 2 - Top view of the NOVSOM™ i.MX6x ***(note that J2, J3 and J4 are mounted on the bottom side of the module)***

3.1 B2B Part Numbers:

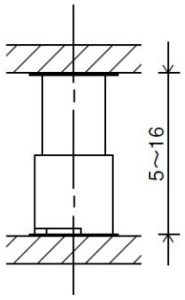
	SoM	Carrier Board
J2	FX8C-140P-SV(yy)	FX8C-140S-SVx(yy)
J3	FX8C-120P-SV(yy)	FX8C-120S-SVx(yy)
J4	FX8C-140P-SV(yy)	FX8C-140S-SVx(yy)

Please retrieve the FX8C connector series from **www.hiroseusa.com**

Table 2 - FX8C stacking options

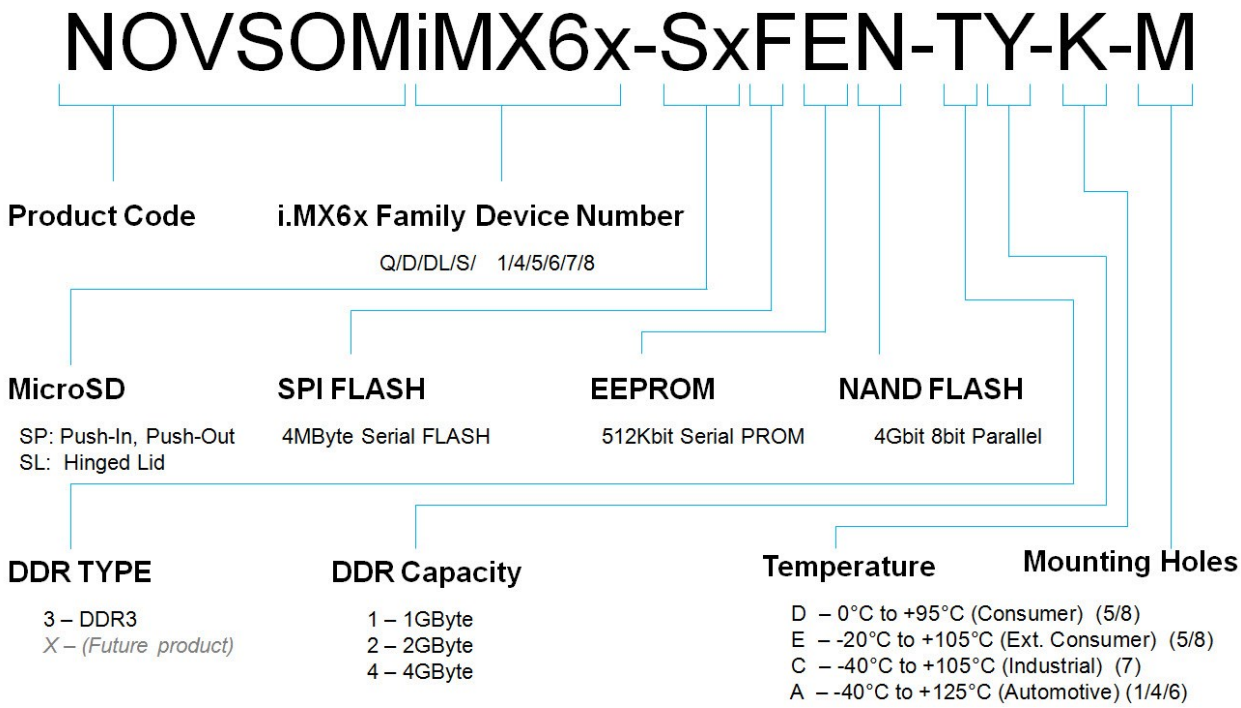
■Stacking height variations (5mm~16mm)

Header \ Receptacle	FX8C-**S-SV FX8C-** / **S11-SVJ	FX8C-**S-SV5 FX8C-** / **S11-SV5J
FX8C-**P-SV FX8C-** / **P11-SVJ	5mm	10mm
FX8C-**P-SV1 FX8C-** / **P11-SV1J	6mm	11mm
FX8C-**P-SV2 FX8C-**/**P11-SV2J	7mm	12mm
FX8C-**P-SV4 FX8C-** / **P11-SV4J	9mm	14mm
FX8C-**P-SV6 FX8C-** / **P11-SV6J	11mm	16mm



The standard NOVSOM™ comes with FX8C-**P-SV allowing a stacking height of 5mm or 10mm. Please take into consideration a 1mm clearance for the components on the bottom side of the NOVSOM™ resulting in a 4mm or 9mm stacking height.

4. Ordering Information



The above options are considered standard options, the following are additional custom options:

- B2B connector height
- Removal of 32.786Kz crystal and supporting external clock
- Changing the boot mode default value of '00'.

Please consult with NovTech regarding the above custom options.

5. Pin-Out Tables

Table 3 - J2 Odd Pin-Out 1 to 69

PIN	SIGNAL	i.MX6x Ball	Note
J2-1	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX2_N	AB1	
J2-3	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX2_P	AB2	
J2-5	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX1_P	AA1	
J2-7	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX1_N	AA2	
J2-9	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX0_N	Y1	
J2-11	i.MX6X_NVCC_LVDS_IPU_LVDS1_TX0_P	Y2	
J2-13	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX3_P	W1	
J2-15	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX3_N	W2	
J2-17	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX2_P	V1	
J2-19	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX2_N	V2	
J2-21	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX0_P	U1	
J2-23	i.MX6X_NVCC_LVDS_IPU_LVDS0_TX0_N	U2	
J2-25	i.MX6X_NVCC_GPIO_GPIO_2	T1	
J2-27	i.MX6X_NVCC_GPIO_GPIO_9	T2	
J2-29	i.MX6X_NVCC_GPIO_GPIO_17	R1	
J2-31	i.MX6X_NVCC_GPIO_GPIO_16	R2	
J2-33	i.MX6X_NVCC_CSI_IPU_CSI_PIXCLK	P1	
J2-35	i.MX6X_NVCC_CSI_IPU_CSI_DAT5	P2	
J2-37	i.MX6X_NVCC_GPIO_KEY_COL2	W6	
J2-39	i.MX6X_NVCC_GPIO_KEY_ROW0	V6	
J2-41	i.MX6X_NVCC_GPIO_KEY_ROW1	U6	
J2-43	i.MX6X_NVCC_GPIO_GPIO_0	T5	
J2-45	i.MX6X_NVCC_GPIO_KEY_ROW3	T7	
J2-47	i.MX6X_NVCC_GPIO_GPIO_4	R6	
J2-49	i.MX6X_NVCC_GPIO_GPIO_19	P5	
J2-51	i.MX6X_NVCC_GPIO_GPIO_18	P6	
J2-53	i.MX6X_NVCC_CSI_IPU_CSI_DAT8	N6	
J2-55	i.MX6X_NVCC_CSI_IPU_CSI_DAT7	N3	
J2-57	i.MX6X_NVCC_CSI_IPU_CSI_DAT6	N4	
J2-59	i.MX6X_NVCC_CSI_IPU_CSI_DAT11	M3	
J2-61	i.MX6X_NVCC_CSI_IPU_CSI_DAT14	M4	
J2-63	i.MX6X_NVCC_CSI_IPU_CSI_DAT17	L3	
J2-65	i.MX6X_NVCC_CSI_IPU_CSI_DAT16	L4	
J2-67	i.MX6X_NVCC_CSI_IPU_CSI_DAT18	M6	
J2-69	i.MX6X_NVCC_HDMI_IPU_DSI_D1_P	H1	

Table 4 – J2 Odd Pin-Out 71 to 139

PIN	SIGNAL	i.MX6x Ball	Note
J2-71	I.MX6X_NVCC_HDMI_IPU_DSI_D1_N	H2	
J2-73	I.MX6X_NVCC_HDMI_IPU_DSI_D0_P	G1	
J2-75	I.MX6X_NVCC_HDMI_IPU_DSI_D0_N	G2	
J2-77	I.MX6X_NVCC_MIPI_CSI_D3_P	F1	
J2-79	I.MX6X_NVCC_MIPI_CSI_D3_N	F2	
J2-81	I.MX6X_NVCC_MIPI_CSI_D2_N	E1	
J2-83	I.MX6X_NVCC_MIPI_CSI_D2_P	E2	
J2-85	I.MX6X_NVCC_MIPI_CSI_D1_N	D1	
J2-87	I.MX6X_NVCC_MIPI_CSI_D1_P	D2	
J2-89	I.MX6X_NVCC_PCIE_PCIE_RX_N	B1	
J2-91	I.MX6X_NVCC_PCIE_PCIE_RX_P	B2	
J2-93	I.MX6X_NVCC_PCIE_PCIE_TX_P	B3	
J2-95	I.MX6X_NVCC_PCIE_PCIE_TX_N	A3	
J2-97	I.MX6X_USBOTG_D_N	B6	
J2-99	I.MX6X_USBOTG_D_P	A6	
J2-101	I.MX6X_NVCC_CSI_IPU_CSI_DAT9	N5	
J2-103	I.MX6X_NVCC_CSI_IPU_CSI_DAT15	M5	
J2-105	I.MX6X_NVCC_CSI_IPU_CSI_DAT19	L6	
J2-107	I.MX6X_USBOTG_VBUS	E9	
J2-109	I.MX6X_USBOTG_CHD_B	B8	
J2-111	I.MX6X_USBH1_VBUS	D10	
J2-113	I.MX6X_NVCC_SD3_SD3_DATA7	F13	
J2-115	I.MX6X_NVCC_SD3_SD3_DATA1	F14	
J2-117	I.MX6X_NVCC_SD3_SD3_DATA6	E13	
J2-119	I.MX6X_NVCC_SD3_SD3_DATA4	D13	
J2-121	I.MX6X_NVCC_SD3_SD3_CLK	D14	
J2-123	I.MX6X_NVCC_SD3_SD3_RST	D15	
J2-125	I.MX6X_NVCC_NANDF_NAND_RB0	B16	
J2-127	I.MX6X_NVCC_SD3_SD3_CMD	B13	
J2-129	I.MX6X_NVCC_NANDF_NAND_CS2	A17	
J2-131	I.MX6X_NVCC_NANDF_NAND_CS3	D16	
J2-133	I.MX6X_NVCC_NANDF_NAND_CLE	C15	
J2-135	I.MX6X_NVCC_NANDF_NAND_CS1	C16	
J2-137	I.MX6X_NVCC_NANDF_NAND_CS0	F15	
J2-139	I.MX6X_NVCC_NANDF_NAND_WP_B	E15	

Table 5 – J2 Even Pin-Out 2 to 70

PIN	SIGNAL	i.MX6x Ball	Note
J2-2	I.MX6X_NVCC_LVDS_IPU_LVDS1_TX3_P	AA4	
J2-4	I.MX6X_NVCC_LVDS_IPU_LVDS1_TX3_N	AA3	
J2-6	I.MX6X_NVCC_LVDS_IPU_LVDS1_CLK_P	Y4	
J2-8	I.MX6X_NVCC_LVDS_IPU_LVDS1_CLK_N	Y3	
J2-10	I.MX6X_NVCC_LVDS_IPU_LVDS0_CLK_N	V4	
J2-12	I.MX6X_NVCC_LVDS_IPU_LVDS0_CLK_P	V3	
J2-14	I.MX6X_NVCC_LVDS_IPU_LVDS0_TX1_N	U4	
J2-16	I.MX6X_NVCC_LVDS_IPU_LVDS0_TX1_P	U3	
J2-18	I.MX6X_NVCC_GPIO_KEY_COL0	W5	
J2-20	I.MX6X_NVCC_GPIO_KEY_ROW2	W4	
J2-22	I.MX6X_NVCC_GPIO_KEY_ROW4	V5	
J2-24	I.MX6X_NVCC_GPIO_KEY_COL3	U5	
J2-26	I.MX6X_NVCC_GPIO_GPIO_6	T3	
J2-28	I.MX6X_NVCC_GPIO_GPIO_1	T4	
J2-30	I.MX6X_NVCC_GPIO_GPIO_7	R3	
J2-32	I.MX6X_NVCC_GPIO_GPIO_5	R4	
J2-34	I.MX6X_NVCC_CSI_IPU_CSI_DATA_EN	P3	
J2-36	I.MX6X_NVCC_CSI_IPU_CSI_MCLK	P4	
J2-38	I.MX6X_NVCC_GPIO_KEY_COL1	U7	
J2-40	I.MX6X_NVCC_GPIO_KEY_COL4	T6	
J2-42	I.MX6X_NVCC_GPIO_GPIO_8	R5	
J2-44	I.MX6X_NVCC_GPIO_GPIO_3	R7	
J2-46	I.MX6X_NVCC_CSI_IPU_CSI_DAT4	N1	
J2-48	I.MX6X_NVCC_CSI_IPU_CSI_VYSNC	N2	
J2-50	I.MX6X_NVCC_CSI_IPU_CSI_DAT10	M1	
J2-52	I.MX6X_NVCC_CSI_IPU_CSI_DAT12	M2	
J2-54	I.MX6X_NVCC_CSI_IPU_CSI_DAT13	L1	
J2-56	I.MX6X_NVCC_HDMI_IPU_HDMI_HPD	K1	
J2-58	I.MX6X_NVCC_HDMI_IPU_HDMI_DDCCEC	K2	
J2-60	I.MX6X_NVCC_HDMI_IPU_HDMI_D0_P	K6	
J2-62	I.MX6X_NVCC_HDMI_IPU_HDMI_D0_N	K5	
J2-64	I.MX6X_NVCC_HDMI_IPU_HDMI_D2_P	K4	
J2-66	I.MX6X_NVCC_HDMI_IPU_HDMI_D2_N	K3	
J2-68	I.MX6X_NVCC_HDMI_IPU_HDMI_D1_P	J4	
J2-70	I.MX6X_NVCC_HDMI_IPU_HDMI_D1_N	J3	

Table 6 – J2 Even Pin-Out 72 to 140

PIN	SIGNAL	i.MX6x Ball	Note
J2-72	I.MX6X_NVCC_HDMI_IPU_DSI_CLK0_P	H4	
J2-74	I.MX6X_NVCC_HDMI_IPU_DSI_CLK0_N	H3	
J2-76	I.MX6X_NVCC_HDMI_IPU_HDMI_CLK_N	J5	
J2-78	I.MX6X_NVCC_HDMI_IPU_HDMI_CLK_P	J6	
J2-80	I.MX6X_NVCC_MIPI_CSI_CLK0_P	F3	
J2-82	I.MX6X_NVCC_MIPI_CSI_CLK0_N	F4	
J2-84	I.MX6X_NVCC_MIPI_CSI_D0_P	E3	
J2-86	I.MX6X_NVCC_MIPI_CSI_D0_N	E4	
J2-88	I.MX6X_ANATOP_CLK2_P	D5	
J2-90	I.MX6X_ANATOP_CLK2_N	C5	
J2-92	I.MX6X_ANATOP_CLK1_P	D7	
J2-94	I.MX6X_ANATOP_CLK1_N	C7	
J2-96	I.MX6X_USBH1_D_N	F10	
J2-98	I.MX6X_USBH1_D_P	E10	
J2-100	I.MX6X_NVCC_MLB_IPU_MLB_S_N	A9	
J2-102	I.MX6X_NVCC_MLB_IPU_MLB_S_P	B9	
J2-104	I.MX6X_NVCC_MLB_IPU_MLB_D_P	A10	
J2-106	I.MX6X_NVCC_MLB_IPU_MLB_D_N	B10	
J2-108	I.MX6X_NVCC_MLB_IPU_MLB_C_N	A11	
J2-110	I.MX6X_NVCC_MLB_IPU_MLB_C_P	B11	
J2-112	I.MX6X_NVCC_SATA_SATA_TX_P	A12	
J2-114	I.MX6X_NVCC_SATA_SATA_TX_N	B12	
J2-116	I.MX6X_NVCC_SATA_SATA_RX_N	A14	
J2-118	I.MX6X_NVCC_SATA_SATA_RX_P	B14	
J2-120	I.MX6X_NVCC_SD3_SD3_DATA5	C13	
J2-122	I.MX6X_NVCC_SD3_SD3_DATA2	A15	
J2-124	I.MX6X_NVCC_SD3_SD3_DATA3	B15	
J2-126	I.MX6X_NVCC_NANDF_NAND_DATA2	F16	
J2-128	I.MX6X_NVCC_NANDF_NAND_DATA3	D17	
J2-130	I.MX6X_NVCC_NANDF_NAND_DATA4	A19	
J2-132	I.MX6X_NVCC_NANDF_NAND_DATA5	B18	
J2-134	I.MX6X_NVCC_NANDF_NAND_DATA6	E17	
J2-136	I.MX6X_NVCC_NANDF_NAND_DATA7	C18	
J2-138	I.MX6X_NVCC_NANDF_NAND_ALE	A16	
J2-140	I.MX6X_NVCC_SD3_SD3_DATA0	E14	

Table 7 - J3 Odd Pin-Out 1 to 69

PIN	SIGNAL	i.MX6x Ball	Note
J3-1	i.MX6x_SATA_VPH	G12	
J3-3	i.MX6x_NVCC_LVDS	V7	
J3-5	i.MX6x_HDMI_VP	L7	
J3-7	i.MX6x_NVCC_MIPI	K7	
J3-9	i.MX6x_HDMI_VPH	M7	
J3-11	i.MX6x_VDDUSB	F9	
J3-13	GND		
J3-15	i.MX6x_PCIE_VP	H7	
J3-17	i.MX6x_PCIE_VPH	G7	
J3-19	i.MX6x_VDD_CACHE	N12	
J3-21	GND		
J3-23	i.MX6x_NVCC_RGMII	G18	
J3-25	i.MX6x_VDDSOC		
J3-27	i.MX6x_VDDSOC		
J3-29	i.MX6x_VDDSOC		
J3-31	GND		
J3-33	GND		
J3-35	GND		
J3-37	i.MX6x_VDDHIGH	H10	
J3-39	i.MX6x_VDDHIGH	J10	
J3-41	i.MX6x_VDD_SNVS_IN	G11	
J3-43	i.MX6x_VDD_SNVS	G9	
J3-45	i.MX6x_VDDARM23		
J3-47	i.MX6x_VDDARM23		
J3-49	i.MX6x_VDDARM23		
J3-51	i.MX6x_NVCC_CSI	N7	
J3-53	i.MX6x_NVCC_JTAG	J7	
J3-55	i.MX6x_NVCC_GPIO	P7	
J3-57	i.MX6x_VDDHIGH_IN	H9	
J3-59	i.MX6x_VDDHIGH_IN	J9	
J3-61	i.MX6x_SATA_VP	G13	
J3-63	i.MX6x_NVCC_SD3	G14	
J3-65	i.MX6x_NVCC_NANDF	G15	
J3-67	i.MX6x_NVCC_SD2	G17	
J3-69	i.MX6x_NVCC_SD1	G16	

Table 8 – J3 Odd Pin-Out 71 to 119

PIN	SIGNAL	i.MX6x Ball	Note
J3-71	i.MX6x_VDDAPU		
J3-73	i.MX6x_VDDAPU		
J3-75	i.MX6x_VDDAPU		
J3-77	i.MX6x_VDDARM		
J3-79	i.MX6x_VDDARM		
J3-81	i.MX6x_VDDARM		
J3-83	i.MX6x_VDDARM_IN		
J3-85	i.MX6x_VDDARM_IN		
J3-87	i.MX6x_VDDARM_IN		
J3-89	i.MX6x_VDDARM_IN		
J3-91	i.MX6x_VDDARM_IN		
J3-93	i.MX6x_VDDARM_IN		
J3-95	i.MX6x_VDDARM_IN		
J3-97	i.MX6x_VDDARM_IN		
J3-99	i.MX6x_VDDARM_IN		
J3-101	i.MX6x_VDDARM_IN		
J3-103	i.MX6x_NVCC_LCD	P19	
J3-105	i.MX6x_NVCC_ENET	R19	
J3-107	i.MX6x_VDDSOC_IN		
J3-109	i.MX6x_VDDSOC_IN		
J3-111	i.MX6x_VDDSOC_IN		
J3-113	i.MX6x_VDDSOC_IN		
J3-115	i.MX6x_VDDSOC_IN		
J3-117	i.MX6x_VDDSOC_IN		
J3-119	i.MX6x_VDDSOC_IN		

Table 9 – J3 Even Pin-Out 2 to 70

PIN	SIGNAL	i.MX6x Ball	Note
J3-2	I.MX6X_NVCC_NANDF_NAND_DATA1	C17	
J3-4	I.MX6X_NVCC_NANDF_NAND_DATA0	A18	
J3-6	CON_KEEP_1		
J3-8	i.MX6x_PCIE_VPTX	G8	
J3-10	CON_KEEP_2		
J3-12	CON_KEEP_3		
J3-14	CON_KEEP_4		
J3-16	CON_KEEP_5		
J3-18	CON_KEEP_6		
J3-20	CON_KEEP_7		
J3-22	CON_KEEP_8		
J3-24	GND		
J3-26	GND		
J3-28	GND		
J3-30	GND		
J3-32	GND		
J3-34	GND		
J3-36	i.MX6x_NVCC_PLL	E8	
J3-38	I.MX6X_NVCC_JTAG_JTAG_TRSTB	C2	
J3-40	I.MX6X_NVCC_JTAG_JTAG_TMS	C3	
J3-42	I.MX6X_NVCC_JTAG_JTAG_TCK	H5	
J3-44	I.MX6X_NVCC_JTAG_JTAG_TDI	G5	
J3-46	I.MX6X_ANATOP_RTC_CLK		
J3-48	I.MX6X_NVCC_JTAG_JTAG_TDO	G6	
J3-50	I.MX6X_NVCC_RESET_PMIC_STBY_REQ	F11	
J3-52	I.MX6X_NVCC_RESET_TAMPER	E11	
J3-54	PM_MCU_NVCC_RESET_I.MX6X_NPOR	C11	
J3-56	I.MX6X_NVCC_RESET_PMIC_ON_REQ	D11	
J3-58	I.MX6X_NVCC_RESET_ONOFF	D12	
J3-60	I.MX6X_NVCC_RESET_BOOT_MODE0	C12	
J3-62	I.MX6X_NVCC_RESET_BOOT_MODE1	F12	
J3-64	GND		
J3-66	GND		
J3-68	GND		
J3-70	GND		

Table 10 – J3 Even Pin-Out 72 to 120

PIN	SIGNAL	i.MX6x Ball	Note
J3-72	GND		
J3-74	GND		
J3-76	GND		
J3-78	GND		
J3-80	GND		
J3-82	GND		
J3-84	GND		
J3-86	GND		
J3-88	GND		
J3-90	i.MX6x_NVCC_EIM0	K19	
J3-92	GND		
J3-94	i.MX6x_NVCC_EIM1	L19	
J3-96	GND		
J3-98	GND		
J3-100	GND		
J3-102	i.MX6x_NVCC_EIM2	M19	
J3-104	GND		
J3-106	GND		
J3-108	GND		
J3-110	GND		
J3-112	GND		
J3-114	GND		
J3-116	GND		
J3-118	GND		
J3-120	GND		

Table 11 – J4 Odd Pin-Out 1 to 69

PIN	SIGNAL	i.MX6x Ball	Note
J4-1	DDR_+1.5V		
J4-3	DDR_+1.5V		
J4-5	DDR_+1.5V		
J4-7	DDR_+1.5V		
J4-9	DDR_+1.5V		
J4-11	DDR_+1.5V		
J4-13	DDR_+1.5V		
J4-15	DDR_+1.5V		
J4-17	DDR_+1.5V		
J4-19	DDR_VTT		
J4-21	DDR_VTT		
J4-23	DDR_VTT		
J4-25	DDR_VTT		
J4-27	DDR_VREF	AC2	
J4-29	I.MX6X_NVCC_SD4_SD4_DATA2	F17	
J4-31	I.MX6X_NVCC_SD2_SD2_DATA2	A23	
J4-33	I.MX6X_NVCC_RGMII_RGMII_RD1	B23	
J4-35	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D23	D25	
J4-37	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D26	E24	
J4-39	I.MX6X_NVCC_SD4_SD4_DATA7	D19	
J4-41	I.MX6X_NVCC_SD2_SD2_CMD	F19	
J4-43	I.MX6X_NVCC_SD2_SD2_DATA1	E20	
J4-45	I.MX6X_NVCC_RGMII_RGMII_TD1	F20	
J4-47	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D20	G20	
J4-49	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D21	H20	
J4-51	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D30	J20	
J4-53	I.MX6X_NVCC_EIM_MAIN0_EIM_OE	K20	
J4-55	I.MX6X_NVCC_EIM_MAIN1_EIM_DA0	L20	
J4-57	I.MX6X_NVCC_EIM_MAIN1_EIM_DA11	M20	
J4-59	I.MX6X_NVCC_RGMII_RGMII_TX_CTL	C23	
J4-61	I.MX6X_NVCC_RGMII_RGMII_TD0	C22	
J4-63	I.MX6X_NVCC_RGMII_RGMII_RD3	D23	
J4-65	I.MX6X_NVCC_RGMII_RGMII_RX_CTL	D22	
J4-67	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D22	E23	
J4-69	I.MX6X_NVCC_EIM_MAIN_SEC_EIM_EB2	E22	

Table 12 – J4 Odd Pin-Out 71 to 139

PIN	SIGNAL	i.MX6x Ball	Note
J4-71	I.MX6X_NVCC_EIM_MAIN_SEC_EIM_EB3	F23	
J4-73	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D24	F22	
J4-75	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D28	G23	
J4-77	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D25	G22	
J4-79	I.MX6X_NVCC_EIM_MAIN0_EIM_A21	H23	
J4-81	I.MX6X_NVCC_EIM_MAIN0_EIM_A20	H22	
J4-83	I.MX6X_NVCC_EIM_MAIN0_EIM_CS1	J23	
J4-85	I.MX6X_NVCC_EIM_MAIN0_EIM_A18	J22	
J4-87	I.MX6X_NVCC_EIM_MAIN1_EIM_EB1	K23	
J4-89	I.MX6X_NVCC_EIM_MAIN0_EIM_LBA	K22	
J4-91	I.MX6X_NVCC_EIM_MAIN1_EIM_DA5	L23	
J4-93	I.MX6X_NVCC_EIM_MAIN1_EIM_DA4	L22	
J4-95	I.MX6X_NVCC_EIM_MAIN1_EIM_DA13	M23	
J4-97	I.MX6X_NVCC_EIM_MAIN1_EIM_DA10	M22	
J4-99	I.MX6X_NVCC_LCD_IPU_DI0_PIN3	N20	
J4-101	I.MX6X_NVCC_LCD_IPU_DISP0_DAT4	P20	
J4-103	I.MX6X_NVCC_LCD_IPU_DISP0_DAT13	R20	
J4-105	I.MX6X_NVCC_EIM_MAIN1_EIM_DA14	N23	
J4-107	I.MX6X_NVCC_EIM_MAIN1_EIM_BCLK	N22	
J4-109	I.MX6X_NVCC_LCD_IPU_DISP0_DAT2	P23	
J4-111	I.MX6X_NVCC_LCD_IPU_DISP0_DAT1	P22	
J4-113	I.MX6X_NVCC_LCD_IPU_DISP0_DAT6	R23	
J4-115	I.MX6X_NVCC_LCD_IPU_DISP0_DAT8	R22	
J4-117	I.MX6X_NVCC_LCD_IPU_DISP0_DAT11	T23	
J4-119	I.MX6X_NVCC_LCD_IPU_DISP0_DAT15	T22	
J4-121	I.MX6X_NVCC_LCD_IPU_DISP0_DAT20	U22	
J4-123	I.MX6X_NVCC_ENET_ENET_MDIO	V23	
J4-125	I.MX6X_NVCC_ENET_ENET_RX_ER	W23	
J4-127	I.MX6X_NVCC_ENET_ENET_RXD1	W22	
J4-129	I.MX6X_NVCC_LCD_IPU_DISP0_DAT0	P24	
J4-131	I.MX6X_NVCC_LCD_IPU_DI0_PIN4	P25	
J4-133	I.MX6X_NVCC_LCD_IPU_DISP0_DAT5	R25	
J4-135	I.MX6X_NVCC_LCD_IPU_DISP0_DAT12	T24	
J4-137	I.MX6X_NVCC_LCD_IPU_DISP0_DAT17	U24	
J4-139	I.MX6X_NVCC_LCD_IPU_DISP0_DAT14	U25	

Table 13 – J4 Even Pin-Out 2 to 70

PIN	SIGNAL	i.MX6x Ball	Note
J4-2	I.MX6X_NVCC_SD1_SD1_DATA0	A21	
J4-4	I.MX6X_NVCC_SD1_SD1_CLK	D20	
J4-6	I.MX6X_NVCC_SD1_SD1_CMD	B21	
J4-8	I.MX6X_NVCC_SD1_SD1_DATA3	F18	
J4-10	I.MX6X_NVCC_SD1_SD1_DATA1	C20	
J4-12	I.MX6X_NVCC_SD1_SD1_DATA2	E19	
J4-14	I.MX6X_NVCC_SD4_SD4_CMD	B17	
J4-16	I.MX6X_NVCC_SD4_SD4_DATA0	D18	
J4-18	I.MX6X_NVCC_SD4_SD4_DATA5	C19	
J4-20	I.MX6X_NVCC_SD4_SD4_DATA4	E18	
J4-22	I.MX6X_NVCC_SD4_SD4_CLK	E16	
J4-24	I.MX6X_NVCC_SD4_SD4_DATA1	B19	
J4-26	I.MX6X_NVCC_SD4_SD4_DATA3	A20	
J4-28	I.MX6X_NVCC_SD4_SD4_DATA6	B20	
J4-30	I.MX6X_NVCC_SD2_SD2_DATA0	A22	
J4-32	I.MX6X_NVCC_SD2_SD2_DATA3	B22	
J4-34	I.MX6X_NVCC_RGMII_RGMII_TD3	A24	
J4-36	I.MX6X_NVCC_RGMII_RGMII_RD2	B24	
J4-38	I.MX6X_NVCC_RGMII_RGMII_RXC	B25	
J4-40	I.MX6X_NVCC_RGMII_RGMII_RD0	C24	
J4-42	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D16	C25	
J4-44	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D18	D24	
J4-46	I.MX6X_NVCC_SD2_SD2_CLK	C21	
J4-48	I.MX6X_NVCC_RGMII_RGMII_TXC	D21	
J4-50	I.MX6X_NVCC_RGMII_RGMII_TD2	E21	
J4-52	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D17	F21	
J4-54	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D19	G21	
J4-56	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D31	H21	
J4-58	I.MX6X_NVCC_EIM_MAIN0_EIM_A23	J21	
J4-60	I.MX6X_NVCC_EIM_MAIN1_EIM_EB0	K21	
J4-62	I.MX6X_NVCC_EIM_MAIN1_EIM_DA2	L21	
J4-64	I.MX6X_NVCC_EIM_MAIN1_EIM_DA9	M21	
J4-66	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D27	E25	
J4-68	I.MX6X_NVCC_EIM_MAIN0_EIM_A22	F24	
J4-70	I.MX6X_NVCC_EIM_MAIN0_EIM_A24	F25	

Table 14 – J4 Even Pin-Out 72 to 140

PIN	SIGNAL	i.MX6x Ball	Note
J4-72	I.MX6X_NVCC_EIM_MAIN0_EIM_A17	G24	
J4-74	I.MX6X_NVCC_EIM_MAIN0_EIM_A19	G25	
J4-76	I.MX6X_NVCC_EIM_MAIN0_EIM_CS0	H24	
J4-78	I.MX6X_NVCC_EIM_MAIN0_EIM_A16	H25	
J4-80	I.MX6X_NVCC_EIM_MAIN0_EIM_RW	J24	
J4-82	I.MX6X_NVCC_EIM_MAIN1_EIM_DA1	J25	
J4-84	I.MX6X_NVCC_EIM_MAIN1_EIM_DA3	K24	
J4-86	I.MX6X_NVCC_EIM_MAIN1_EIM_DA6	K25	
J4-88	I.MX6X_NVCC_EIM_MAIN1_EIM_DA8	L24	
J4-90	I.MX6X_NVCC_EIM_MAIN1_EIM_DA7	L25	
J4-92	I.MX6X_NVCC_EIM_MAIN1_EIM_DA12	M24	
J4-94	I.MX6X_NVCC_EIM_MAIN1_EIM_WAIT	M25	
J4-96	I.MX6X_NVCC_EIM_MAIN1_EIM_DA15	N24	
J4-98	I.MX6X_NVCC_LCD_IPU_DI0_PIN2	N25	
J4-100	I.MX6X_NVCC_EIM_MAIN0_EIM_A25	H19	
J4-102	I.MX6X_NVCC_EIM_MAIN_SEC_WEIM_D29	J19	
J4-104	I.MX6X_NVCC_LCD_IPU_DI0_DISP_CLK	N19	
J4-106	I.MX6X_NVCC_LCD_IPU_DISP0_DAT21	T20	
J4-108	I.MX6X_NVCC_ENET_ENET_TXD0	U20	
J4-110	I.MX6X_NVCC_ENET_ENET_MDC	V20	
J4-112	I.MX6X_NVCC_ENET_ENET_TXD1	W20	
J4-114	I.MX6X_NVCC_LCD_IPU_DI0_PIN15	N21	
J4-116	I.MX6X_NVCC_LCD_IPU_DISP0_DAT3	P21	
J4-118	I.MX6X_NVCC_LCD_IPU_DISP0_DAT10	R21	
J4-120	I.MX6X_NVCC_LCD_IPU_DISP0_DAT16	T21	
J4-122	I.MX6X_NVCC_LCD_IPU_DISP0_DAT19	U23	
J4-124	I.MX6X_NVCC_ENET_ENET_CRS_DV	U21	
J4-126	I.MX6X_NVCC_ENET_ENET_REF_CLK	V22	
J4-128	I.MX6X_NVCC_ENET_ENET_TX_EN	V21	
J4-130	I.MX6X_NVCC_LCD_IPU_DISP0_DAT7	R24	
J4-132	I.MX6X_NVCC_ENET_ENET_RXD0	W21	
J4-134	I.MX6X_NVCC_LCD_IPU_DISP0_DAT9	T25	
J4-136	I.MX6X_NVCC_LCD_IPU_DISP0_DAT18	V25	
J4-138	I.MX6X_NVCC_LCD_IPU_DISP0_DAT22	V24	
J4-140	I.MX6X_NVCC_LCD_IPU_DISP0_DAT23	W24	

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