

# Bridgetek Pte Ltd

## FT905/6/7/8

### (Datasheet)



The FT905/6/7/8 series includes the FT905, FT906, FT907 and FT908 which are complete System-On-Chip 32-bit RISC microcontrollers for embedded applications featuring a high level of integration and low power consumption. They have the following features:

- High performance, low power 32-bit FT32core processor, running at a frequency of 100MHz.
- 256kB on-chip Flash memory.
- 256kB on-chip shadow program memory.
- True Zero Wait States (OWS) up to 3.1 DMIPS per MHz performance.
- 64kB on-chip data memory.
- Flash OTP memory for security configuration.
- Integrated Phase-Locked Loop (PLL) supports external 12MHz crystal and direct external clock source input.
- 32.768 kHz Real Time Clock (RTC) support.
- One USB 2.0 EHCI compatible host controller supports high-speed (480Mbit/s), full-speed (12Mbit/s), and low-speed (1.5Mbit/s).
- One USB 2.0 device controller supports high-speed (480Mbit/s) and full-speed (12Mbit/s).
- USB 2.0 host and device controllers support the Isochronous, Interrupt, Control, and Bulk transfers.
- Supports USB Battery Charging Specification Rev 1.2. Downstream port can be configured as SDP, CDP or DCP. Upstream port can perform BCD mode detection.
- 10/100Mbps Ethernet that is compliant with the IEEE 802.3/802.3u standards. (FT905 and FT906 only).
- Supports One-Wire debugger for downloading firmware to Flash memory or shadow program memory, and supports a software debugger.
- Two CAN controllers support CAN protocol 2.0 parts A&B, data rate is up to 1Mbit/s. (FT905 and FT907 only).
- One SPI master supports single / dual / quad modes of data transfer. Clock rate is up to 25 MHz.
- One SPI slave supports single data transfer with a 25MHz clock.
- One I<sup>2</sup>C interface which can be configured as a master or a slave. It supports standard / fast / fast-plus / high speed mode data transfers of up to 3.4 Mbit/s. Clock stretching is supported.
- UART interface can be configured as one full programmable UART0 or two simple UART0 and UART1 with CTS / RTS control function only.
- Four user timers with pre-scaling and a watchdog function.
- Supports 7 independent PWM channels. Channel 0 and 1 can be configured as PCM 8-bit/16-bit stereo audio output.
- Supports two 10-bit DACs 0/1 channels output, sample rate at ~1 MS/s.
- Supports four 8-bit/10-bit ADC 1/4 channels input, sample rate is up to ~960 KS/s.
- Single 3.3 volt power supply and built-in 1.2 V regulators.
- 3.3 volt I/O power supply.
- Supports VBUS power switching and overcurrent control.
- Provides a Power-On Reset (POR) signal to indicate stable power regulator.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free -76-pin (QFN) and 80-pin (LQFP) packages (all RoHS compliant).

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# 1 Typical Applications

- Home security system
- Home Automation
- Embedded audio application
- Motor drive and application control
- E-meter
- CCTV monitor
- Industrial automation
- Medical appliances
- Instrumentation
- DAQ System

## 1.1 Part Numbers

| Part Number | Package   |
|-------------|---|
| FT905Q-C-X  | 76 Pin QFN, pitch 0.4mm, body 9mm x 9mm x 0.9mm, support both CAN Bus and Ethernet features.              |
| FT905L-C-X  | 80 Pin LQFP, pitch 0.4mm, body 10mm x 10mm x 1.40mm, support both CAN Bus and Ethernet features.          |
| FT906Q-C-X  | 76 Pin QFN, pitch 0.4mm, body 9mm x 9mm x 0.9mm, support Ethernet, doesn't support CAN Bus.               |
| FT906L-C-X  | 80 Pin LQFP, pitch 0.4mm, body 10mm x 10mm x 1.40mm, support Ethernet, doesn't support CAN Bus.           |
| FT907Q-C-X  | 76 Pin QFN, pitch 0.4mm, body 9mm x 9mm x 0.9mm, support CAN Bus, doesn't support Ethernet.               |
| FT907L-C-X  | 80 Pin LQFP, pitch 0.4mm, body 10mm x 10mm x 1.40mm, support CAN Bus, doesn't support Ethernet.           |
| FT908Q-C-X  | 76 Pin QFN, pitch 0.4mm, body 9mm x 9mm x 0.9mm, doesn't support either CAN Bus or Ethernet features.     |
| FT908L-C-X  | 80 Pin LQFP, pitch 0.4mm, body 10mm x 10mm x 1.40mm, doesn't support either CAN Bus or Ethernet features. |

**Table 1-1 - FT905/6/7/8 Series Part Numbers**

**Note:** Packaging codes for x is:

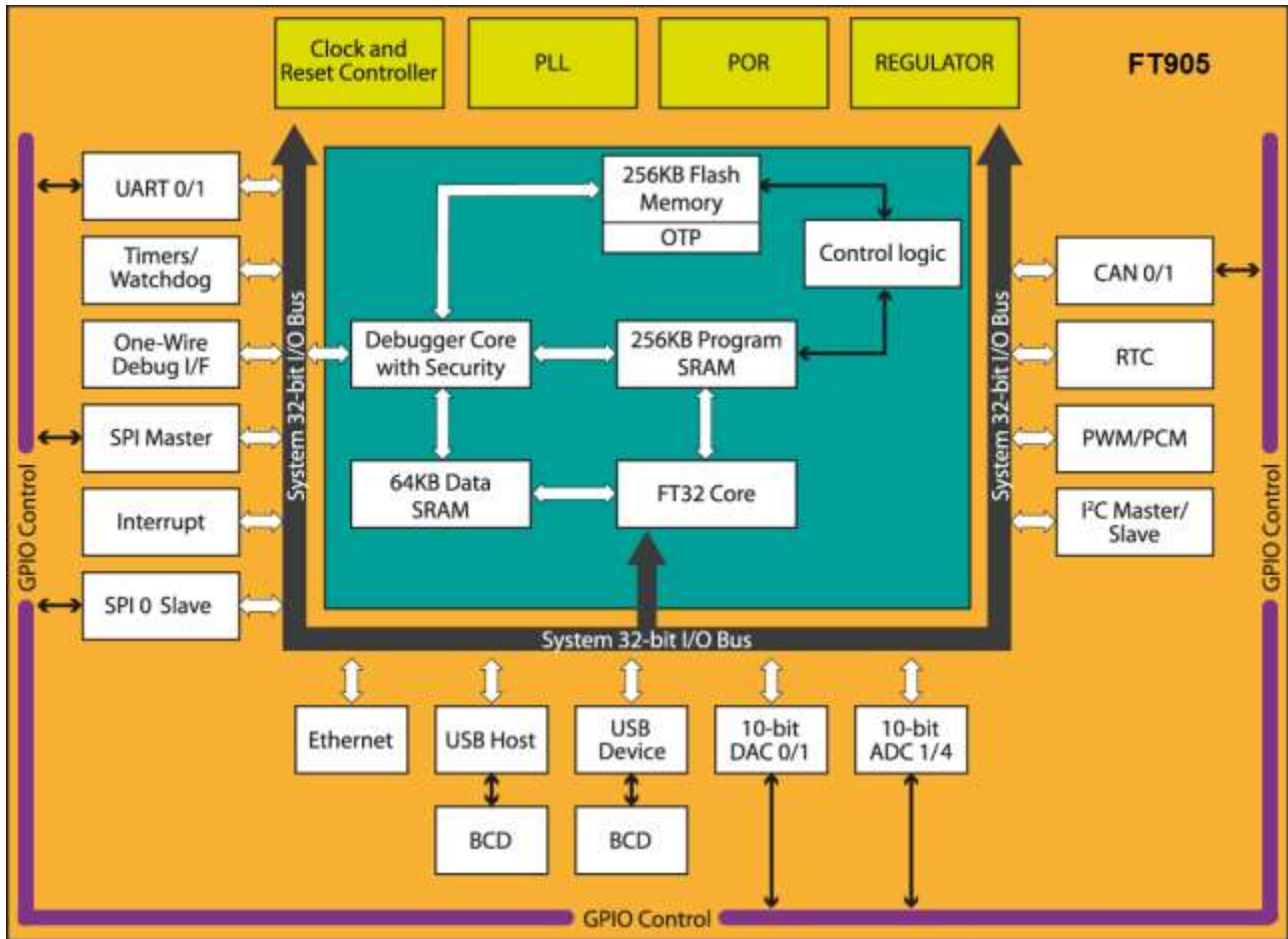
-R: Taped and Reel (qty per reel for LQFP is 1000; qty per reel for QFN is 3000)

-T: Tray packing (qty per tray for LQFP is 160; qty per tray for QFN is 260)

## 1.2 USB 2.0 Compliant

The FT905/6/7/8 series contains a USB 2.0 host controller and device controller that are both compliant with USB 2.0 specification.

## 2 FT905 Block Diagram



**Figure 2-1 - FT905 Block Diagram**

For a description of each function please refer to [Chapter 4](#).

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## 3 Device Pin Out and Signal Description

### 3.1 Pin Out – FT905 QFN-76

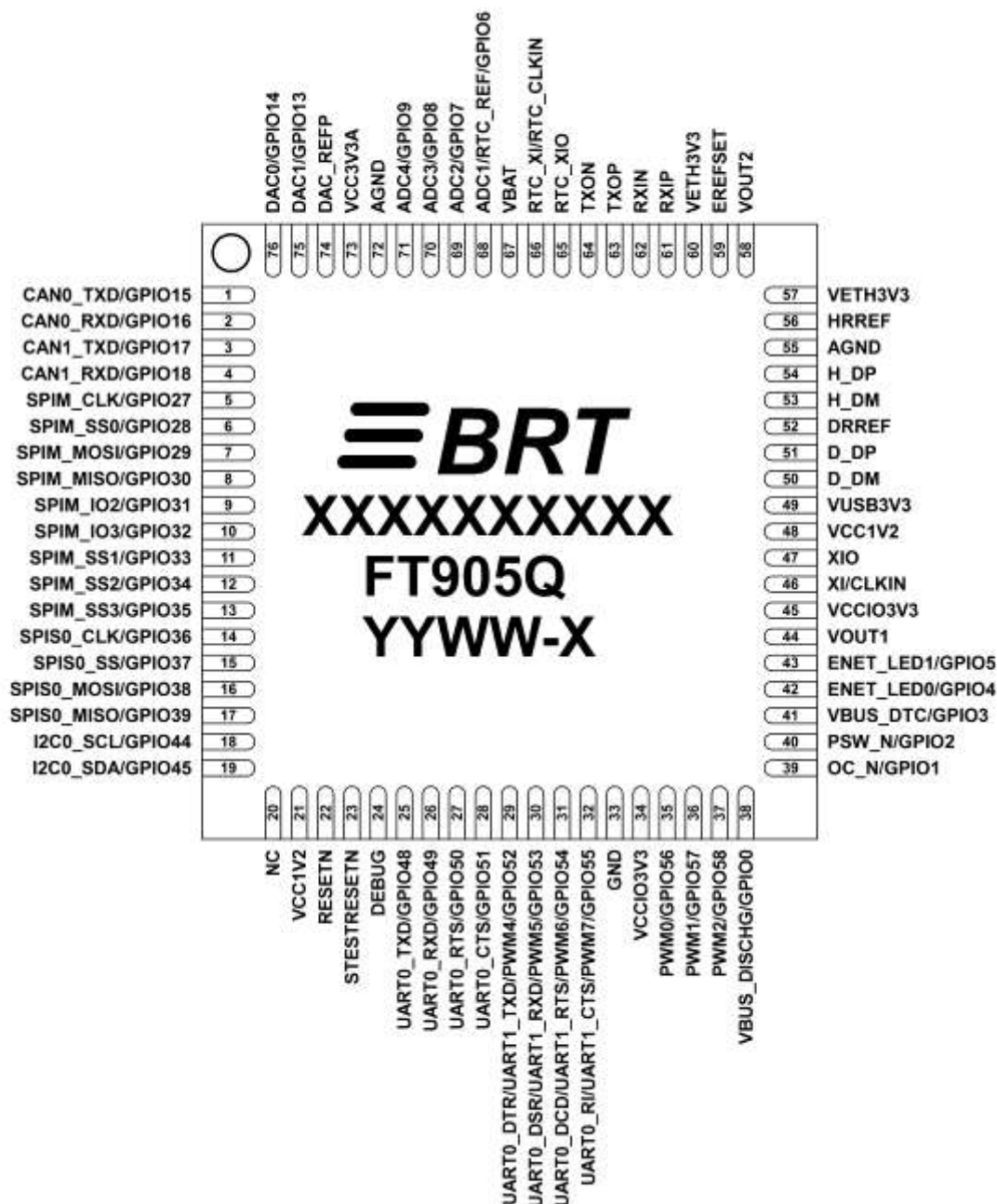
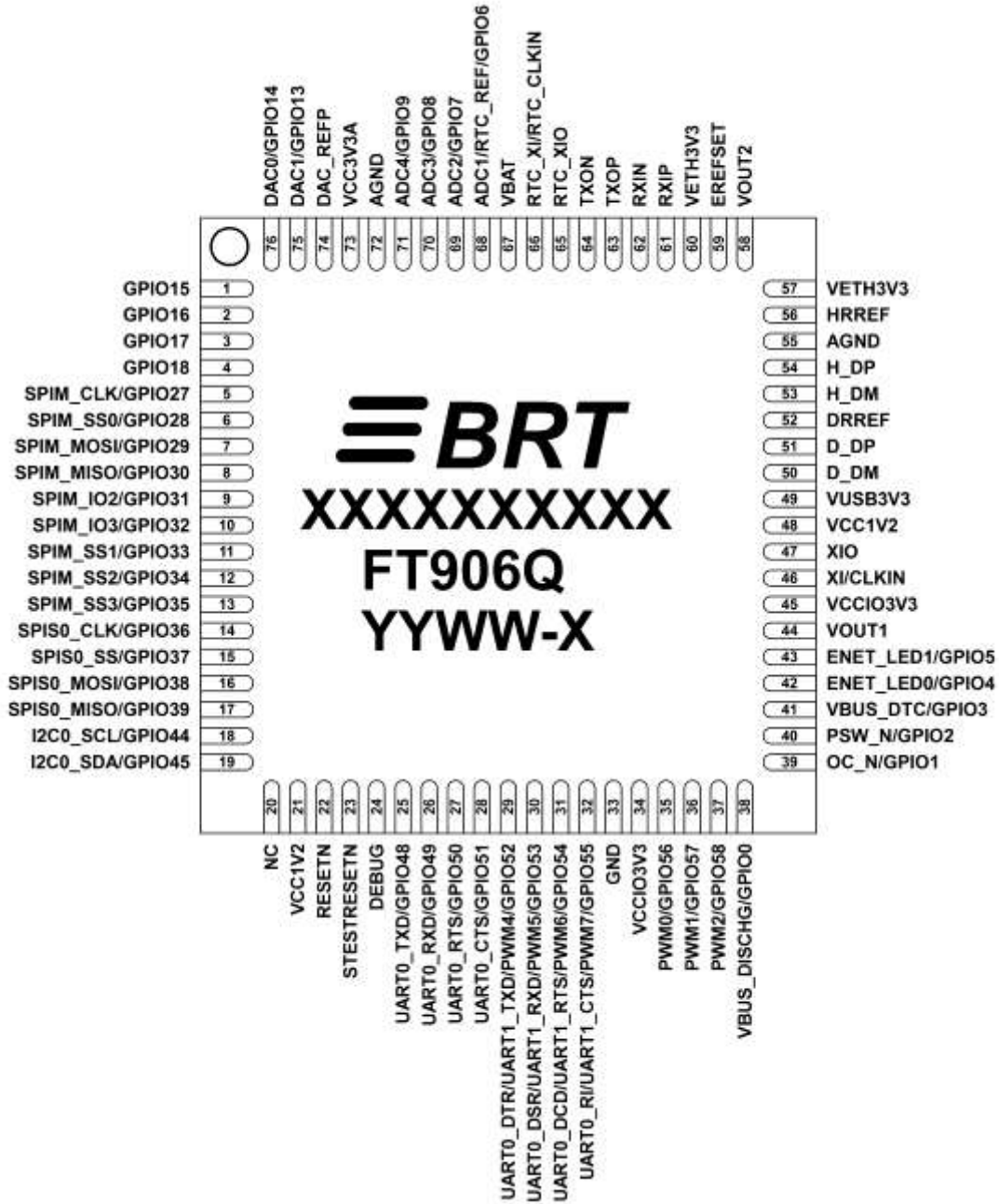
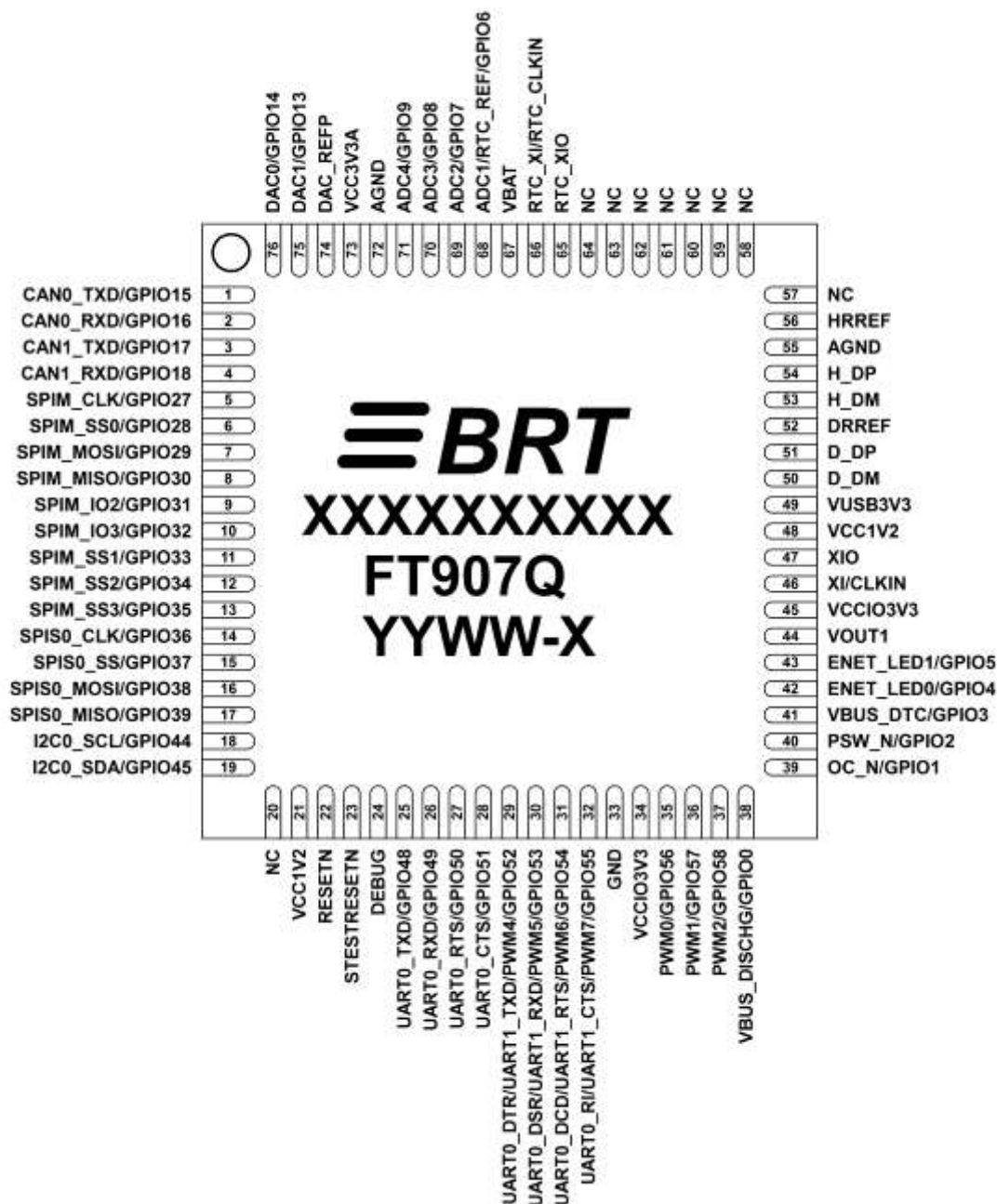


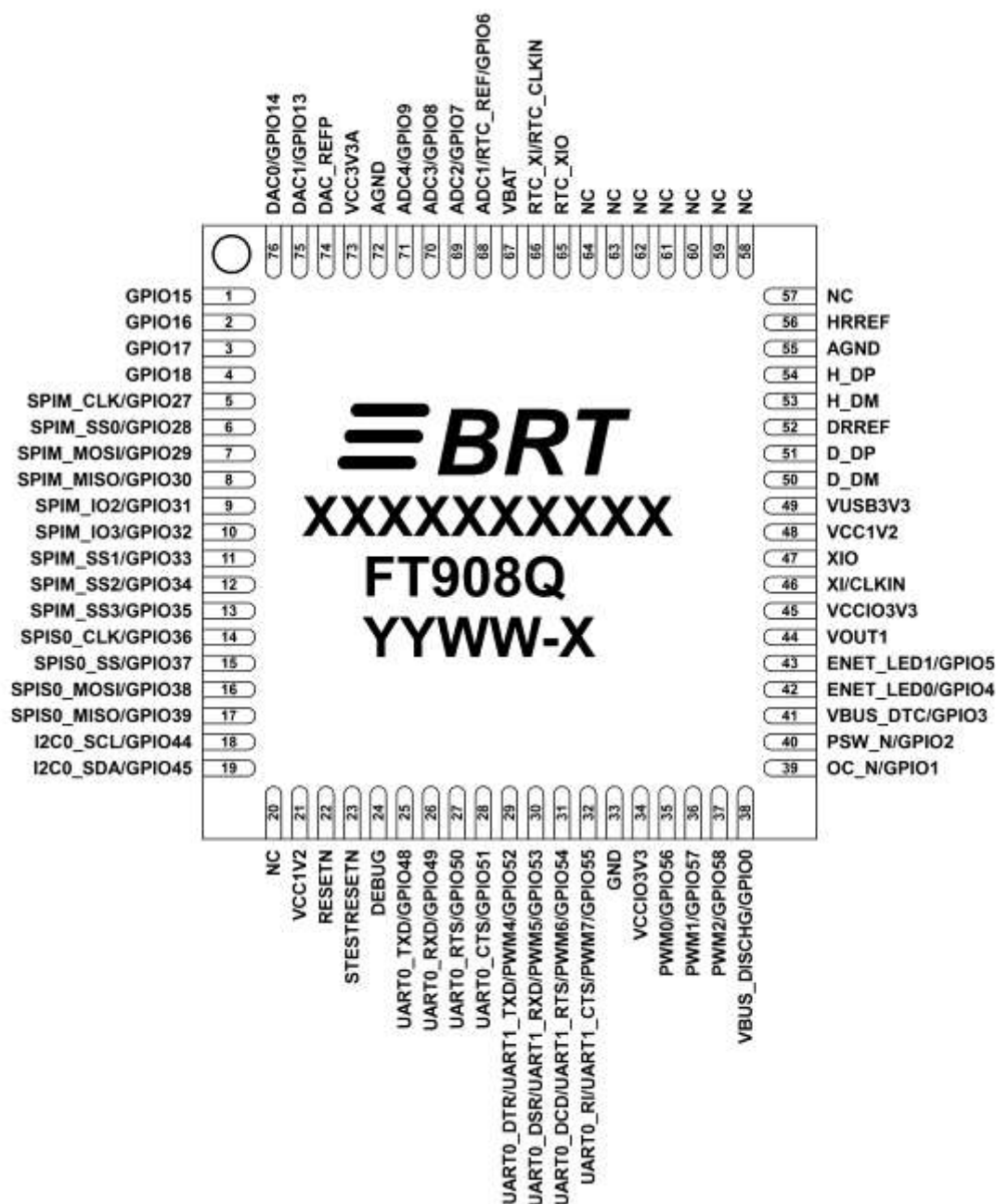
Figure 3-1 - Pin Configuration FT905Q (top-down view)



**Figure 3-2 - Pin Configuration FT906Q (top-down view)**



**Figure 3-3 - Pin Configuration FT907Q (top-down view)**



### Figure 3-4 - Pin Configuration FT908Q (top-down view)

### 3.2 Pin Out – FT905 LQFP-80

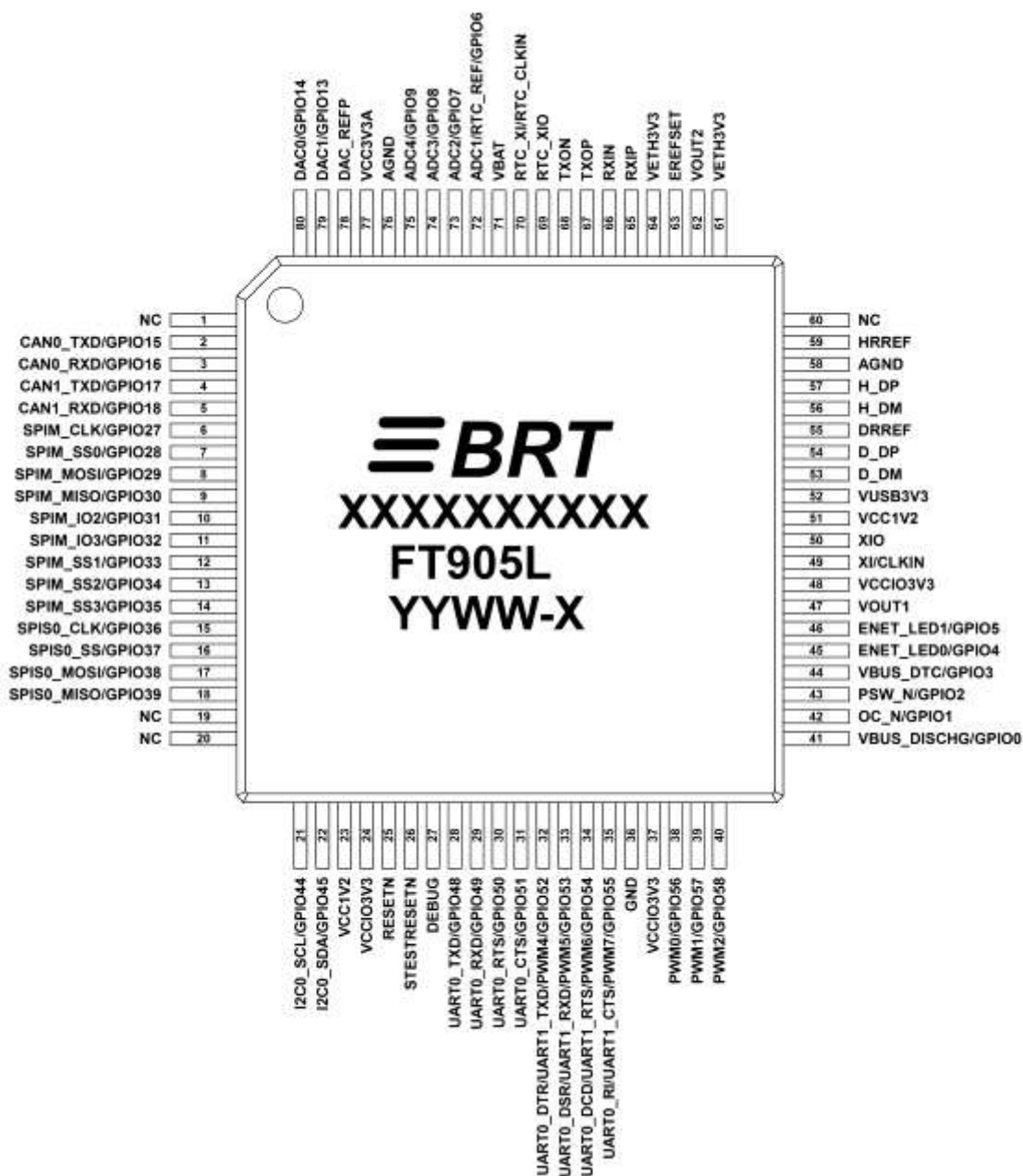
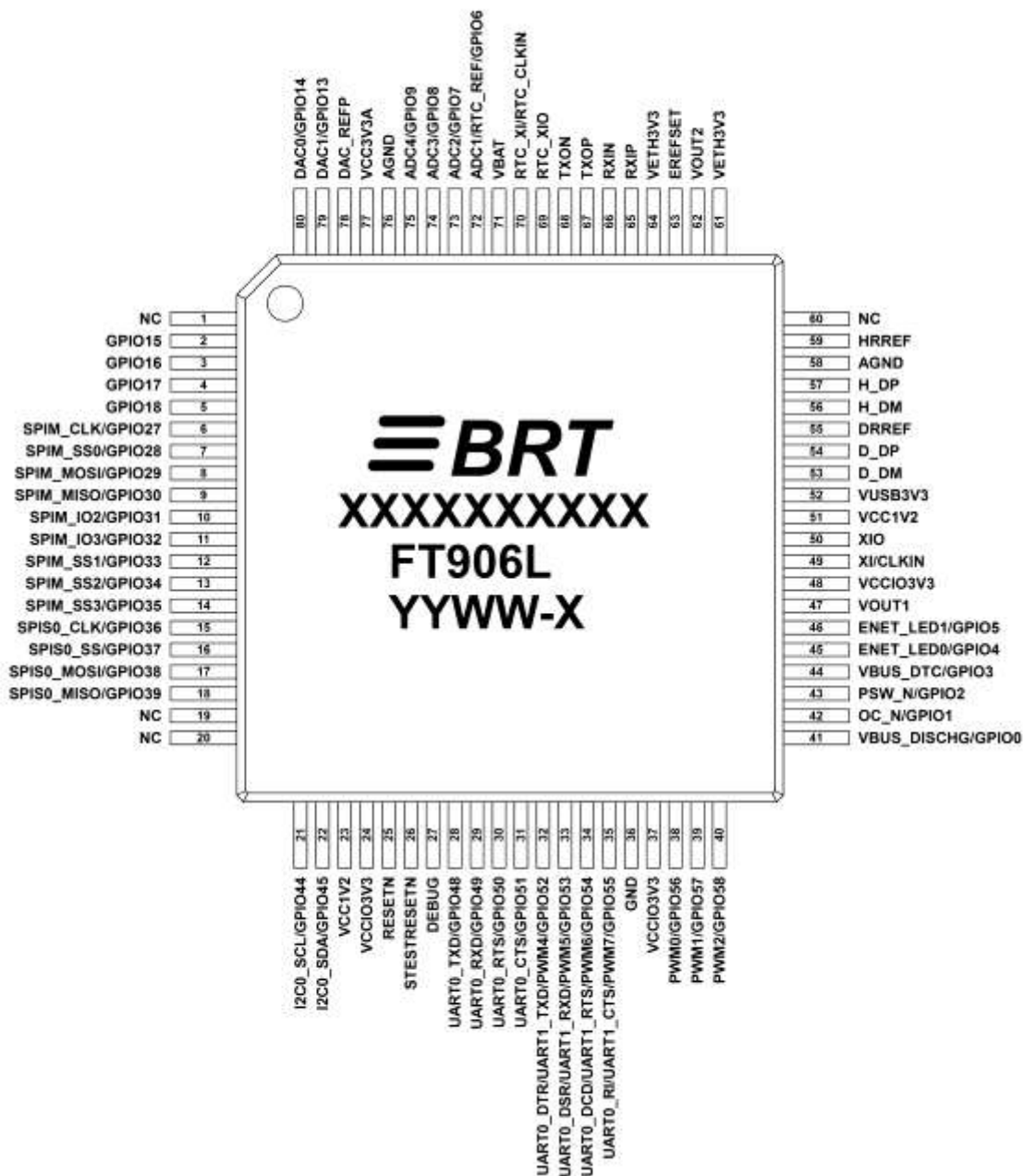
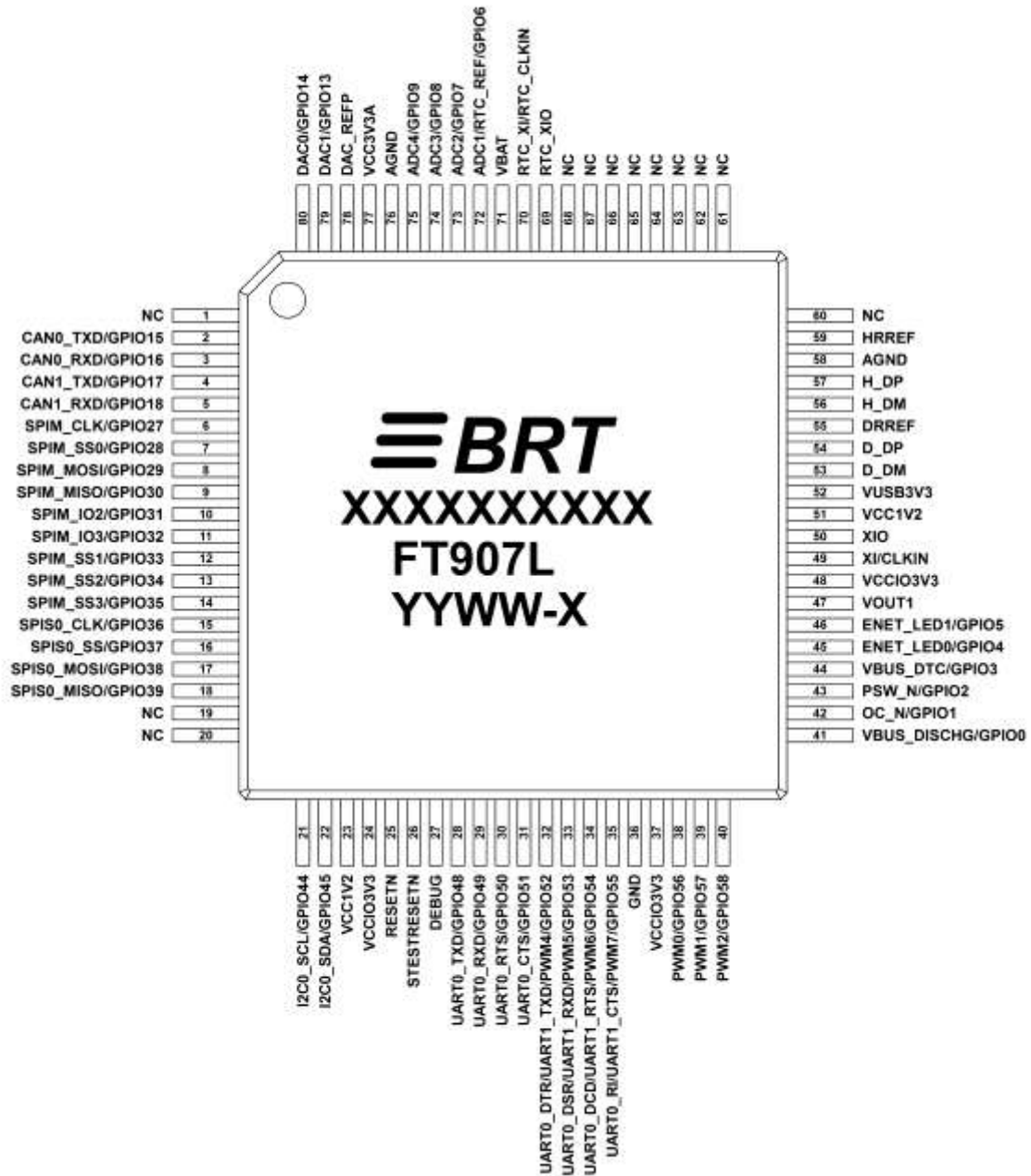


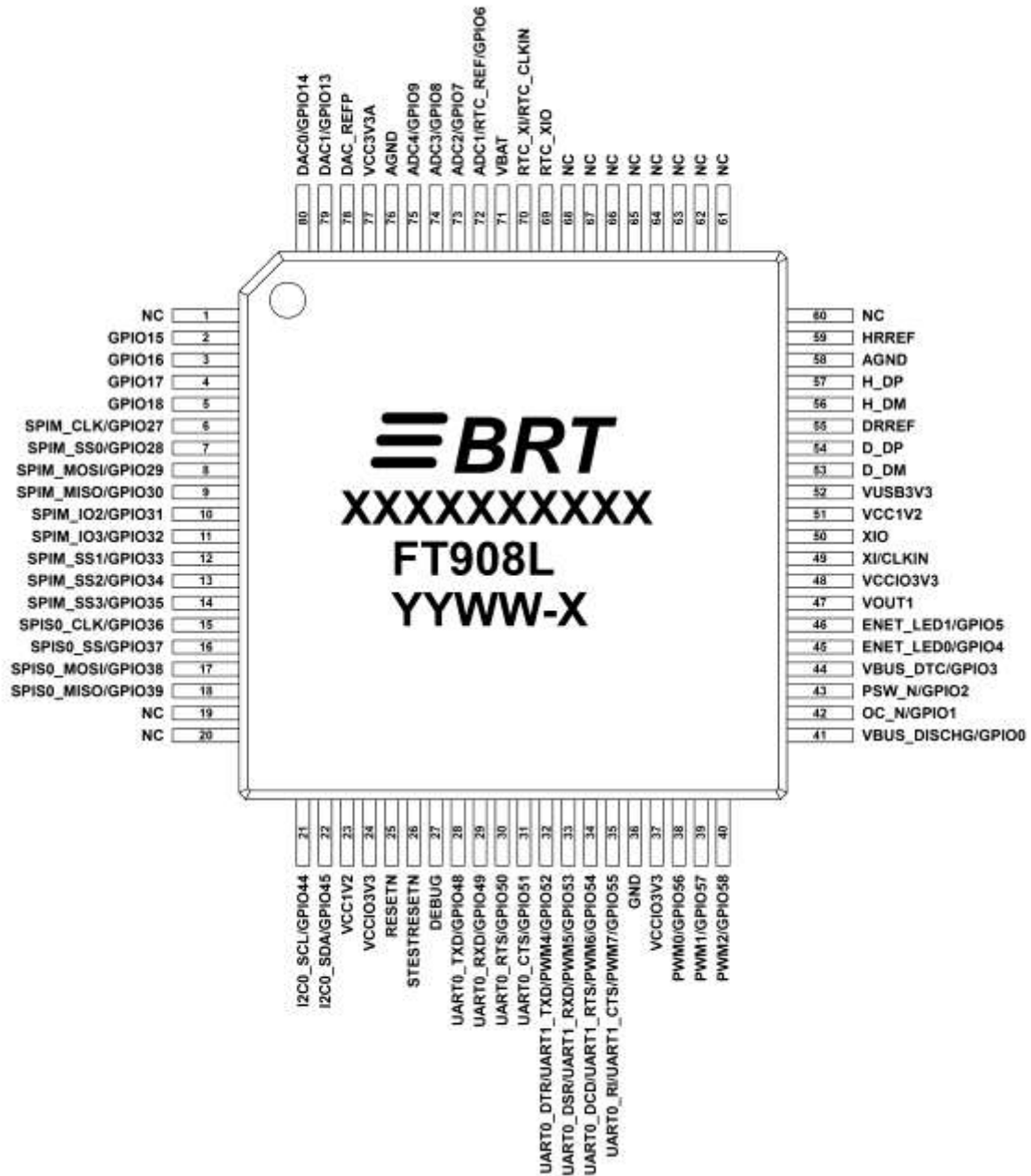
Figure 3-5 - Pin Configuration FT905L (top-down view)



**Figure 3-6 - Pin Configuration FT906L (top-down view)**



**Figure 3-7 - Pin Configuration FT907L (top-down view)**



**Figure 3-8 - Pin Configuration FT908L (top-down view)**

### 3.3 Pin Description

| QFN Pin No. | LQFP Pin No. | Name             | Type | Description  |
|-------------|--------------|------------------|------|--|
| -           | 1            | NC               | -    | Not connected.   |
| 1           | 2            | CAN0_TXD/GPIO15  | I/O  | GPIO15 input/output. (By default is GPIO input, internal pull-low)<br>CAN0 transmitter output. <a href="#">[1]</a>   |
| 2           | 3            | CAN0_RXD/GPIO16  | I/O  | GPIO16 input/output. (By default is GPIO input, internal pull-low)<br>CAN0 receiver input. <a href="#">[1]</a>   |
| 3           | 4            | CAN1_TXD/GPIO17  | I/O  | GPIO17 input/output. (By default is GPIO input, internal pull-low)<br>CAN1 transmitter output. <a href="#">[1]</a>   |
| 4           | 5            | CAN1_RXD/GPIO18  | I/O  | GPIO18 input/output. (By default is GPIO input, internal pull-low)<br>CAN1 receiver input. <a href="#">[1]</a>   |
| 5           | 6            | SPIM_CLK/GPIO27  | I/O  | GPIO27 input/output. (By default is GPIO input, internal pull-low)<br>Serial clock output for SPI master.  |
| 6           | 7            | SPIM_SS0/GPIO28  | I/O  | GPIO28 input/output. (By default is GPIO input, internal pull-low)<br>Slave select 0 output for SPI master.  |
| 7           | 8            | SPIM_MOSI/GPIO29 | I/O  | GPIO29 input/output. (By default is GPIO input, internal pull-low)<br>Master out slave in for SPI master.<br>Data line 0 input/output for SPI master dual & quad mode. |
| 8           | 9            | SPIM_MISO/GPIO30 | I/O  | GPIO30 input/output. (By default is GPIO input, internal pull-low)<br>Master in slave out for SPI master.<br>Data line 1 input/output for SPI master dual & quad mode. |
| 9           | 10           | SPIM_IO2/GPIO31  | I/O  | GPIO31 input/output. (By default is GPIO input, internal pull-low)<br>Data line 2 input/output for SPI master quad mode.   |
| 10          | 11           | SPIM_IO3/GPIO32  | I/O  | GPIO32 input/output. (By default is GPIO input, internal pull-low)<br>Data line 3 input/output for SPI master quad mode.   |
| 11          | 12           | SPIM_SS1/GPIO33  | I/O  | GPIO33 input/output. (By default is GPIO input, internal pull-low)<br>Slave select 1 output for SPI master.  |
| 12          | 13           | SPIM_SS2/GPIO34  | I/O  | GPIO34 input/output. (By default is GPIO input, internal pull-low)<br>Slave select 2 output for SPI master.  |
| 13          | 14           | SPIM_SS3/GPIO35  | I/O  | GPIO35 input/output. (By default is GPIO input, internal pull-low)   |

| QFN Pin No. | LQFP Pin No. | Name               | Type | Description  |
|-------------|--------------|--------------------|------|--|
|             |              |                    |      | Slave select 3 output for SPI master.  |
| 14          | 15           | SPIS0_CLK/GPIO36   | I/O  | GPIO36 input/output. (By default is GPIO input, internal pull-low)<br>Serial clock input for SPI slave 0.  |
| 15          | 16           | SPIS0_SS/GPIO37    | I/O  | GPIO37 input/output. (By default is GPIO input, internal pull-low)<br>Slave select input for SPI slave 0.  |
| 16          | 17           | SPIS0_MOSI /GPIO38 | I/O  | GPIO38 input/output. (By default is GPIO input, internal pull-low)<br>Master out slave in for SPI slave 0.   |
| 17          | 18           | SPIS0_MISO /GPIO39 | I/O  | GPIO39 input/output. (By default is GPIO input, internal pull-low)<br>Master in slave out for SPI slave 0.   |
| -           | 19           | NC                 | -    | Not connected.   |
| -           | 20           | NC                 | -    | Not connected.   |
| 18          | 21           | I2C0_SCL/GPIO44    | I/O  | GPIO44 input/output. (By default is GPIO input, internal pull-low)<br>I2C 0 serial clock input/output. (By default is I2C 0 master)  |
| 19          | 22           | I2C0_SDA/GPIO45    | I/O  | GPIO45 input/output. (By default is GPIO input, internal pull-low)<br>I2C 0 data line input/output. (By default is I2C 0 master)   |
| 20          | -            | NC                 | -    | Not connected.   |
| 21          | 23           | VCC1V2             | P    | +1.2V supply voltage for PLL.<br>Connect +1.2V output from the internal regulator to this pin. Specifically, this pin must be connected to pin 44 of QFN package or pin 47 of LQFP package. Connect a 0.1uF decoupling capacitor to GND. |
| -           | 24           | VCCIO3V3           | P    | +3.3V supply voltage.<br>This is the supply voltage for all the I/O ports. Connect a 0.1uF decoupling capacitor to GND. This pin must be connected to pin 37.  |
| 22          | 25           | RESETN             | I    | Chip reset input for normal operation. Active low. Connect external 10kΩ pull-up to VCC3V3 for safe operation.   |
| 23          | 26           | STESTRESETN        | I    | Chip reset input for test mode.<br>Connect this pin to Ground via a 10kΩ resistor for normal operation.  |
| 24          | 27           | DEBUG              | I/O  | One-wire debugger interface input/output.  |
| 25          | 28           | UART0_TXD/GPIO48   | I/O  | GPIO48 input/output. (By default is GPIO input, internal pull-low)<br>Transmitter output for UART0.  |
| 26          | 29           | UART0_RXD/GPIO49   | I/O  | GPIO49 input/output. (By default is GPIO input, internal pull-low)   |

| QFN Pin No. | LQFP Pin No. | Name                             | Type | Description  |
|-------------|--------------|----------------------------------|------|--|
|             |              |                                  |      | Receiver input for UART0.  |
| 27          | 30           | UART0_RTS/GPIO50                 | I/O  | GPIO50 input/output. (By default is GPIO input, internal pull-low)<br>Request to send output for UART0.  |
| 28          | 31           | UART0_CTS/GPIO51                 | I/O  | GPIO51 input/output. (By default is GPIO input, internal pull-low)<br>Clear to send input for UART0.   |
| 29          | 32           | UART0_DTR/UART1_TX D/PWM4/GPIO52 | I/O  | GPIO52 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 4, output.<br>Transmitter output for UART1.<br>Data terminal ready output for UART0.       |
| 30          | 33           | UART0_DSR/UART1_RXD/PWM5/GPIO53  | I/O  | GPIO53 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 5, output.<br>Receiver input for UART1.<br>Data set ready input for UART0.                 |
| 31          | 34           | UART0_DCD/UART1_RTS/PWM6/GPIO54  | I/O  | GPIO54 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 6, output.<br>Request to send output for UART1.<br>Data carrier detection input for UART0. |
| 32          | 35           | UART0_RI/UART1_CTS/PWM7/GPIO55   | I/O  | GPIO55 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 7, output.<br>Clear to send input for UART1.<br>Ring indicator input for UART0.            |
| 33          | 36           | GND                              | P    | Ground   |
| 34          | 37           | VCCIO3V3                         | P    | +3.3V supply voltage.<br>This is the supply voltage for all the I/O ports. Connect 10uF and 0.1uF decoupling capacitors.   |
| 35          | 38           | PWM0/GPIO56                      | I/O  | GPIO56 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 0, output.<br>A stereo 16/8-bit PCM audio data channel output.                             |
| 36          | 39           | PWM1/GPIO57                      | I/O  | GPIO57 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 1, output.<br>A stereo 16/8-bit PCM audio data channel output.                             |
| 37          | 40           | PWM2/GPIO58                      | I/O  | GPIO58 input/output. (By default is GPIO input, internal pull-low)<br>PWM channel 2, output.   |

| QFN Pin No. | LQFP Pin No. | Name               | Type | Description   |
|-------------|--------------|--------------------|------|---|
| 38          | 41           | VBUS_DISCHG /GPIO0 | I/O  | GPIO0 input/output. (By default is GPIO input, internal pull-high)<br>USB host VBUS discharge.  |
| 39          | 42           | OC_N/GPIO1         | I/O  | GPIO1 input/output. (By default is GPIO input, internal pull-high)<br>USB host port over current status output. Active low.   |
| 40          | 43           | PSW_N/GPIO2        | I/O  | GPIO2 input/output. (By default is GPIO input, internal pull-high)<br>USB host port external VBUS power switcher. Active low.   |
| 41          | 44           | VBUS_DTC/GPIO3     | I/O  | GPIO3 input/output. (By default is GPIO input, internal pull-low)<br>USB device VBUS detection.   |
| 42          | 45           | ENET_LED0/GPIO4    | I/O  | GPIO4 input/output. (By default is GPIO input, internal pull-low)<br>Ethernet activity indicator LED 0. <a href="#">[2]</a>   |
| 43          | 46           | ENET_LED1/GPIO5    | I/O  | GPIO5 input/output. (By default is GPIO input, internal pull-low)<br>Ethernet activity indicator LED 1. <a href="#">[2]</a>   |
| 44          | 47           | VOUT1              | P    | +1.2V Regulator power supply.<br>This is internal regulator output. Connect 4.7uF and 0.1uF decoupling capacitors.  |
| 45          | 48           | VCCIO3V3           | P    | +3.3V supply voltage.<br>This is the supply voltage for all the I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 34 of QFN package or pin 37 LQFP package.                            |
| 46          | 49           | XI/CLKIN           | AI   | 12MHz clock frequency input to the Oscillator circuit or to internal clock generator circuit.   |
| 47          | 50           | XIO                | AO   | Output from the Oscillator amplifier.   |
| 48          | 51           | VCC1V2             | P    | +1.2V Regulator power supply for USB.<br>Provide +1.2V power to this pin. This pin must be connected to pin 44 of QFN package or pin 47 of LQFP package. Connect 0.1uF decoupling capacitor.                            |
| 49          | 52           | VUSB3V3            | P    | +3.3V supply voltage.<br>This is the supply voltage for USB device and host I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor. |
| 50          | 53           | D_DM               | AI/O | USB device bidirectional DM line.   |
| 51          | 54           | D_DP               | AI/O | USB device bidirectional DP line.   |
| 52          | 55           | DRREF              | AI   | USB device reference voltage input.<br>Connect 12Kohm +/- 1% resistor to GND.   |
| 53          | 56           | H_DM               | AI/O | USB host bidirectional DM line.   |

| QFN Pin No. | LQFP Pin No. | Name               | Type | Description  |
|-------------|--------------|--------------------|------|--|
| 54          | 57           | H_DP               | AI/O | USB host bidirectional DP line.  |
| 55          | 58           | AGND               | P    | Analog Ground  |
| 56          | 59           | HRREF              | AI   | USB host reference voltage input.<br>Connect 12Kohm +/- 1% resistor to GND.  |
| -           | 60           | NC                 | -    | Not connected.   |
| 57          | 61           | VETH3V3            | P    | +3.3V supply voltage.<br>This is the supply voltage for Ethernet I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor. |
| 58          | 62           | VOUT2              | P    | +1.2V Regulator power supply. <sup>[2]</sup><br>This is internal regulator output for Ethernet transceiver. Connect 0.1uF decoupling capacitor.  |
| 59          | 63           | EREFSET            | AI   | Ethernet reference voltage input. <sup>[2]</sup><br>Connect 12.3Kohm +/- 1% resistor to GND.   |
| 60          | 64           | VETH3V3            | P    | +3.3V supply voltage.<br>This is the supply voltage for Ethernet I/O ports. Connect a 0.1uF decoupling capacitor. This pin must be connected to pin 57 of QFN package or pin 61 of LQFP package.             |
| 61          | 65           | RXIP               | I    | Ethernet receive data positive input. <sup>[2]</sup><br>Differential receive signal pair.  |
| 62          | 66           | RXIN               | I    | Ethernet receive data negative input. <sup>[2]</sup><br>Differential receive signal pair.  |
| 63          | 67           | TXOP               | O    | Ethernet transmit data positive output. <sup>[2]</sup><br>Differential transmit signal pair.   |
| 64          | 68           | TXON               | O    | Ethernet transmit data negative output. <sup>[2]</sup><br>Differential transmit signal pair.   |
| 65          | 69           | RTC_XIO            | AO   | Output from the RTC Oscillator amplifier.  |
| 66          | 70           | RTC_XI/RTC_CLKIN   | AI   | 32.768KHz clock frequency input to the RTC Oscillator circuit or to internal RTC clock generator circuit.  |
| 67          | 71           | VBAT               | P    | +1.5V RTC supply voltage.  |
| 68          | 72           | ADC1/RTC_REF/GPIO6 | I/O  | GPIO6 input/output. (By default is GPIO input, internal pull-low)<br>Reference clock for RTC calibration.<br>10-bit A/D converter 1, input.  |
| 69          | 73           | ADC2/GPIO7         | I/O  | GPIO7 input/output. (By default is GPIO input, internal pull-low)<br>10-bit A/D converter 2, input.  |

| QFN Pin No. | LQFP Pin No. | Name        | Type | Description  |
|-------------|--------------|-------------|------|--|
| 70          | 74           | ADC3/GPIO8  | I/O  | GPIO8 input/output. (By default is GPIO input, internal pull-low)<br>10-bit A/D converter 3, input.  |
| 71          | 75           | ADC4/GPIO9  | I/O  | GPIO9 input/output. (By default is GPIO input, internal pull-low)<br>10-bit A/D converter 4, input.  |
| 72          | 76           | AGND        | P    | Analog Ground  |
| 73          | 77           | VCC3V3A     | P    | +3.3V supply voltage.<br>This is the supply voltage for Analog I/O ports. Connect 10uF and 0.1uF decoupling capacitors. This pin could be connected to all +3.3V power supply pins without 10uF capacitor. |
| 74          | 78           | DAC_REFP    | P    | 10-bit DAC positive reference voltage.   |
| 75          | 79           | DAC1/GPIO13 | I/O  | GPIO13 input/output. (By default is GPIO input, internal pull-low)<br>10-bit D/A converter 1, output.  |
| 76          | 80           | DAC0/GPIO14 | I/O  | GPIO14 input/output. (By default is GPIO input, internal pull-low)<br>10-bit D/A converter 0, output.  |

**Table 3-1 - FT905 pin description**

- [1] CAN Bus 0/1 only are featured on both FT905 and FT907 packages.
- [2] Ethernet pins are available on FT905 and FT906 only. For FT907 and FT908, shall leave all Ethernet pins as NC pin floating except for ENET\_LED0/GPIO4 and ENET\_LED1/GPIO5 as GPIO by default.

**Notes:**

|    |                     |      |                                 |
|----|---------------------|------|---------------------------------|
| P  | : Power or ground   | I/O  | : Bi-direction Input and Output |
| I  | : Input             | AI   | : Analog Input                  |
| O  | : Output            | AO   | : Analog Output                 |
| OD | : Open drain output | AI/O | : Analog Input / Output         |

## 4 Function Description

### 4.1 Architectural Overview

The FT905/6/7/8 series embedded microcontrollers include a high performance 32-bit FT32 RISC core processor and 256kB hi-speed Flash memory for software program downloading with a One-Wire debugger interface. The core processor uses a 32-bit I/O system bus to connect to all of the peripherals.

- 32-bit MCU Processor Core
- 256kB Flash Memory
- 256kB Shadow Program Memory
- 64kB Data Memory
- USB2.0 host controller with battery charging capability
- USB2.0 device controller with battery charging detection capability
- 10/100Mbps Ethernet controller (*FT905 and FT906 only*)
- Two CAN bus interfaces (*FT905 and FT907 only*)
- Real Time Clock
- One-Wire debugger interface
- One SPI master interface and one SPI slave interface
- One I<sup>2</sup>C bus interface, which can be configured as a master or a slave
- Programmable 8 Mb/s UART interface, which can be configured as one fully-functional UART or two simple UARTs with CTS/RTS flow control function only
- Four 16-bit timers and one 32-bit watchdog timer
- 8-Channel PWM with optional 2-Channel Audio PCM
- 10-bit DAC0/1 channel
- Configurable 8-bit/10-bit four channel 480/960 kS/s ADC
- General purpose I/O interface

The functions for each controller / interface are briefly described in the following subsections.

### 4.2 FT32 Core Processor

The FT32 core processor is running at frequencies of up to 100MHz. The processor contains the CPU itself with control logic and its 256kB program memory and 64kB data memory. The outside connections for the core processor are the memory-mapped I/O interface, the interrupt interface, asynchronous reset and the system clock.

### 4.3 256kB Flash Memory

The internal 256kB Flash memory is used to store a boot loader or user application of the FT905/6/7/8 series. It is a high performance and low power consumption memory that supports up to 80MHz serial clock. The system will perform memory copy from Flash memory to CPU program memory automatically after system power on.

### 4.4 Boot Sequence

After the initial memory copy completes, the CPU jumps to program memory location zero. This may be the start of the user application which is stored in advance in Flash memory, or a boot loader only which allows program memory to perform modifications via (e.g.) UART or USB.

The option of a boot loader is a special purpose routine in the FT905/6/7/8 series embedded microcontrollers. It is small routine stored in the Flash memory. Typically the boot loader is 1-4kbytes in size, and is loaded at the top of the available memory.

## 4.5 Interrupt

The FT905/6/7/8 series interrupt controller handles 32 interrupt inputs. When an interrupt occurs, the Interrupt Service Route (ISR) will process this event via the CPU. The ISR vector range is from 0 to 31, which corresponds to interrupts 0 to 31. See Table 4-1 for more information.

Each interrupt shall be assigned the interrupt vector number and priority before use. By default, the highest priority interrupt is interrupt 0, and the lowest is interrupt 31. However, the interrupt priority can be rearranged by register settings and also allows multiple interrupts at the same priority.

To prevent the loss and delay of high priority interrupts, the FT905/6/7/8 series uses nested interrupts if enabled. Nested interrupts allow interrupt requests of a high priority to pre-empt interrupt requests of a low priority. The FT905/6/7/8 series supports up to 16-levels deep, nested interrupts.

The interrupt controller has a global interrupt mask bit to temporarily block all interrupts. If this bit is set to "1", then with the exception of an interrupt assigned priority as "0", which is a non-maskable interrupt (NMI) input, all interrupts are masked.

See Table 4-1 for FT905/6/7/8 series default interrupt priority.

| Peripherals of Interrupt | Interrupt Vector Index | Default Priority |
|--------------------------|------------------------|------------------|
| Power Management         | 0                      | 0 (NMI)          |
| USB2.0 Host Controller   | 1                      | 1                |
| USB2.0 Device Controller | 2                      | 2                |
| Ethernet Controller      | 3                      | 3                |
| <b>UNUSED</b>            | <b>4</b>               | <b>4</b>         |
| CAN Bus 0                | 5                      | 5                |
| CAN Bus 1                | 6                      | 6                |
| <b>UNUSED</b>            | <b>7</b>               | <b>7</b>         |
| SPI Master               | 8                      | 8                |
| SPI Slave 0              | 9                      | 9                |
| <b>UNUSED</b>            | <b>10</b>              | <b>10</b>        |
| I <sup>2</sup> C Master  | 11                     | 11               |
| I <sup>2</sup> C Slave   | 12                     | 12               |
| UART 0                   | 13                     | 13               |
| UART 1                   | 14                     | 14               |
| <b>UNUSED</b>            | <b>15</b>              | <b>15</b>        |
| PWM                      | 16                     | 16               |
| Timers                   | 17                     | 17               |
| GPIO                     | 18                     | 18               |
| RTC                      | 19                     | 19               |

| Peripherals of Interrupt | Interrupt Vector Index | Default Priority |
|--------------------------|------------------------|------------------|
| ADC                      | 20                     | 20               |
| DAC                      | 21                     | 21               |
| Slow Clock Timer         | 22                     | 22               |
| <b>UNUSED</b>            | <b>23-31</b>           | <b>23-31</b>     |

**Table 4-1 - Default interrupt priority in FT905/6/7/8 series**

## 4.6 Memory Mapping

A list of the I/O memory mapping for registers and memory in the FT905/6/7/8 series is given below in table 4-2. Refer to the [FT9xx User Manual](#) for a detailed description of registers.

| Function   | Address Memory Range |         | Comment                       |
|--|----------------------|---------|-------------------------------|
| General setup registers                                | 0x10000              | 0x100BF | DW/W/B                        |
| Interrupt controller registers                         | 0x100C0              | 0x100FF | DW/W/B                        |
| USB2.0 host controller registers                       | 0x10100              | 0x1017F | DW/W/B                        |
| USB2.0 host controller RAM memory                      | 0x11000              | 0x12FFF | DW/W/B                        |
| USB2.0 device controller registers                     | 0x10180              | 0x1021F | DW/W/B                        |
| USB2.0 device registers for high-bandwidth isochronous | 0x10A1C              | 0x10A33 | DW/W/B                        |
| Ethernet controller registers                          | 0x10220              | 0x1023F | Registers: DW/W/B<br>FIFO: DW |
| CAN BUS 0 registers                                    | 0x10240              | 0x1025F | B                             |
| CAN BUS 1 registers                                    | 0x10260              | 0x1027F | B                             |
| RTC registers  | 0x10900              | 0x1093F | DW                            |
| SPI master registers                                   | 0x102A0              | 0x102BF | DW                            |
| SPI master registers (extended)                        | 0x10940              | 0x1095F | DW                            |
| SPI slave 0 registers                                  | 0x102C0              | 0x102DF | DW                            |
| SPI slave 0 registers (extended)                       | 0x10960              | 0x1097F | DW                            |
| I <sup>2</sup> C master registers                      | 0x10300              | 0x1030F | B                             |
| I <sup>2</sup> C slave registers                       | 0x10310              | 0x1031F | B                             |
| UART 0 register  | 0x10320              | 0x1032F | B                             |
| UART 1 registers                                       | 0x10330              | 0x1033F | B                             |

| Function                    | Address Memory Range |         | Comment                 |
|-----------------------------|----------------------|---------|-------------------------|
| Timers & Watchdog registers | 0x10340              | 0x1034F | B                       |
| PWM registers               | 0x103C0              | 0x103FF | Registers: B<br>FIFO: W |
| Flash controller registers  | 0x10800              | 0x108BF | B                       |

**Table 4-2 - I/O memory mapping in FT905/6/7/8 series**

**Notes:** DW / W / B are length of register operation

DW: Double Word (32-bit)      W: Word (16-bit)      B: Byte (8-bit)

## 4.7 USB 2.0 Host Controller

The Hi-Speed USB 2.0 single-port host controller is compliant with the USB 2.0 specification and the Enhanced Host Controller Interface (EHCI) specification. There is an option to enable a downstream port with a Battery Charging (BC) feature, which can be configured as a Standard Downstream Port (SDP), or Charging Downstream Port (CDP), or Dedicated Charging Port (DCP). The battery charging feature is compatible with the [Battery Charging Specification Revision 1.2 \(BC 1.2\)](#) by USB-IF.

### Features

- Compliant with the USB specification revision 2.0.
- Compliant with EHCI specification revision 1.0.
- The USB1.1 host is integrated into the USB2.0 EHCI compatible host controller.
- Supports data transfer at hi-speed (480 Mb/s), full-speed (12 Mb/s) and low-speed (1.5 Mb/s).
- Supports the split transaction for hi-speed hubs and the preamble transaction of full-speed hubs.
- Supports the Isochronous/Interrupt/Control/Bulk data transfers.
- 8 kB high speed RAM memory integrated.
- Supports Battery Charging specification revision 1.2.
- Supports VBUS power switching and over current control.

## 4.8 USB2.0 Device Controller

The USB 2.0 device controller is fully compliant with the USB2.0 specification. There is also an option to enable a battery charger detection (BCD) feature on an upstream port, which can identify whether the connected downstream port supports SDP, CDP or DCP charging function. Battery charge detection allows the USB device to determine if higher currents may be available from the USB connection for rapid battery charging.

### Features

- Supports data transfer at high-speed (480 Mb/s) and full-speed (12 Mb/s).
- Software configurable EP0 control endpoint size 8-64 bytes.
- Software configurable 7 IN/OUT endpoints.
- EP1-EP7 has double buffering which contains 2kB IN and 2kB OUT buffers.
- Supports the Isochronous/Interrupt/Control/Bulk data transfers.
- Supports high-bandwidth isochronous IN transaction.
- Max endpoint packet sizes upon 1024 bytes.
- Supports VBUS detection.
- Supports suspend and resume power management functions.
- Supports remote wakeup feature.
- Supports Battery Charging specification revision 1.2.

## 4.9 Ethernet Controller

The Ethernet controller contains an on-chip 10/100BASE-TX Ethernet transceiver and Media Access Control (MAC) designed to provide high performance of frame transmission and reception. The Ethernet transceiver is compliant with 10/100BASE-TX Ethernet standards, such as IEEE802.3/802.3u and ANSI X3.263-1995, and the MAC protocol refers to IEEE standard 802.3-2000.

### Features

- 10/100Mbps data transfer.
- Conforms to IEEE 802.3-2002 specification.
- Supports full-duplex and half-duplex modes.
  - Supports CSMA/CD protocol for half-duplex operation.
  - Supports IEEE802.3x flow control for full-duplex operation.
- Programmable MAC address.
- CRC-32 algorithm calculates the FCS a nibble at a time, with automatic FCS generation and checking, able to capture frames with CRC errors if required.
- Promiscuous mode support.
- Station Management (STA) entity included.
- Supports double buffering for 2kB TX and 4kB RX memory.
- Two LED indicators used by Ethernet multi-function.

## 4.10 CAN Bus Controller

The FT905/6/7/8 series contains two controllers, CAN0 and CAN1. Controller Area Network (CAN) is a high performance communication protocol for serial data communication. It is widely used in automotive and industrial applications; however this is expanding due to its reliability and feasibility. CAN bus use a multi-master bus scheme with one logic bus line and equal nodes. The number of nodes is not limited by the protocol. Nodes do not have specific addresses. Instead, message identifiers are used, indicating the message content and priority of the message. The FT905/6/7/8 CAN controller supports multicasting and broadcasting with an external CAN transceiver.

### Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rates of up to 1 Mb/s.
- Supports standard (11-bit identifier) and extended (29-bit identifier) frames.
- Support hardware message filtering with dual/single filters.
- 64 Bytes receiver and 16 Bytes transmitter FIFO.
- No overload frames are generated.
- Supports normal and listen-only modes.
- Supports single shot transmission.
- Supports an abort transmission feature.
- Readable error counters and last error code capture supported.

## 4.11 Real Time Clock

The Real Time Clock (RTC) runs off a dedicated 32.768 kHz oscillator with its own power rail which can be connected to a separate battery via the VBAT pin.

### Features

- Built-in Clock Stabilizer for the 32.768 kHz input.
- Records systems sleep time.
- Supports Date and Time format in BCD.
- Counts Second, Minute, Hour, Day, Date of the Month, Month and Year with Leap-Year Compensation Valid up to 2199.
- Supports two configurable Time-of-Day Alarms.
- Supports interrupt for two configurable alarm events.
- Supports On-Chip Digital Trimming with Auto Calibration.

## 4.12 One-Wire Debugger Interface

The Debugger interface provides the capability, over a One-Wire half duplex serial link, to access memory mapped address space, such as the Flash memory, program memory, data memory and I/O memory. However, there is no transfer capability from any of the internal memory to the debugger interface.

**Features**

- Single wire half duplex link that has one Start, eight Data and one Stop bits at a 1M bit/s rate.
- Supports debugger command read / write operation with variable data transfer.
- Supports CHIP ID read out.
- Supports checksum checking by Flash memory operation.
- Supports CPU software debugging to execute Run, Stop, Step, Halt, Set software breakpoint, etc. operations.
- Use semaphore flag to control resource allocated by CPU or Debugger.

**4.13 SPI Interface**

The FT905/6/7/8 series contains one SPI master and one SPI slave controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus.

**Features**

- Maximum SPI data bit rate 50 MHz in master and 25 MHz in slave mode.
- Full duplex synchronous serial data transfer.
- Compliant with SPI specification, support four transfer formats.
- The SPI master controller supports Single, Dual and Quad SPI transfer.
- The SPI slave controller supports Single transfer only.
- Supports SPI mode and FIFO mode operations.
- Multi-master system supported.
- Supports bus error detection.
- The SPI master controller can address up to 4 SPI slave devices.
- Support 16 / 64 Bytes receiver and 16 / 64 Bytes transmitter FIFO respectively.

**4.14 I<sup>2</sup>C Interface**

The FT905/6/7/8 series supports an I<sup>2</sup>C bus controller which is a bidirectional, two wires (Serial Clock line (SCL) and a Serial Data line (SDA)) interface. The interface can be programmed to operate with arbitration and clock synchronization allowing it to operate in multi-master systems. It supports transmission speed up to 3.4 Mb/s.

**Features**

- Conforms to v2.1 and v3.0 of the I<sup>2</sup>C specification.
  - UM10204 I<sup>2</sup>C-bus specification and user manual Rev. 6 – 4 April 2014
- Supports flexible transmission speed modes.
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast-plus (up to 1 Mb/s)
  - High-speed (up to 3.4 Mb/s)
- Can be configured as Master mode or Slave mode.
- Perform arbitration and clock synchronization.
- Multi-master systems supported.
- Supports both 7-bit and 10-bit addressing modes on the I<sup>2</sup>C bus.
- Supports clock stretching.

**4.15 UART Interface**

The FT905/6/7/8 series contains two UART controllers, namely UART0 and UART1, with standard transmit and receive data lines.

UART0 provides a full modem control handshake interface and support for 9-bit data, allowing automatic address detection while 9-bit data mode is enabled.

UART1 is a simplified programmable serial interface with CTS and RTS flow control logic. The signals are multiplexed with UART0 and can only be used if UART0 is used in simple mode (CTS/RTS only).

### Features

- Maximum UART data bit rate of 8Mbit/s.
- Supports UART mode and FIFO mode operation.
- 16 / 128 bytes FIFO for TX and RX in FIFO mode to reduce the interrupt frequency.
- Software compatible with 16450, 16550, 16750 and 16950 industry standard.
- Modem control function (CTS, RTS, DSR, DTR, RI, and DCD) support for UART0.
- Programmable automatic out-of-band flow control logic through Auto-RTS and Auto-CTS.
- Programmable automatic flow control logic using DTR and DSR.
- Programmable automatic in-band flow control logic using XON/XOFF characters.
- Supports external RS-485 buffer enable.
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7-, 8-, or 9-bit characters
  - Even, Odd, or No-parity bit generation and detection
  - 1-, 1.5- (for 5 data bits only) or 2- (for 6/7/8 data bits) stop bit generation
  - Baud rate generation
  - Detection of bad data in Receive FIFO
- Supports Transmitter and Receiver disable capability.

## 4.16 Timers and Watchdog Timer

The FT905/6/7/8 series has four 16-bit user timers with individual pre-scaler and a 32-bit watchdog feature.

The watchdog timer is controlled from the main clock. The watchdog can be initialized with a 5-bit register. The value of this register points to a bit of the 32-bit counter which will be set by the application firmware. As the timer decrements, an interrupt occurs when the timer rolls over. Once started and initialized the watchdog can't be stopped. It can only be cleared by writing into a register.

The four user timers can be controlled from the main clock, each timer has its own 16-bit pre-scaler. These timers can be started, stopped and cleared / initialized. The pre-scalers can be cleared or initialised the same way.

The current value of all timers/pre-scalers can be read from a common register one-at-a-time (multiplexed access).

All timers can count up/down and signal an interrupt when the timer rolls over. The timers can also be configured to be one-shot or in continuous mode. They are initialised from a common register one-at-a-time (multiplexed access).

If the user timer has already started using its pre-scaler, it cannot be cleared and the command is ignored. Each of the pre-scalers automatically stops after it is cleared individually. It also starts automatically when the corresponding user timer starts using it.

### Features

- Four user timers with individual pre-scaler.
- Supports 16-bit pre-scaler with system clock reference.
- Supports individual timer interrupt.
- Supports one-shot and continuous count for timer.
- Supports 32-bit counter watchdog.
- Supports watchdog interrupt.

## 4.17 PWM

The FT905/6/7/8 series supports 7 separate independent PWM output channels. All channels share an 8-bit pre-scaler to scale the system clock frequency to the desired channels.

Each channel has its own 16-bit comparator value. This is the value that would be matched to a preset 16-bit counter. When a channel's 16-bit comparator value matches that of the 16-bit counter, the corresponding PWM channel output will toggle. This 16-bit comparator value will continue to count until it reaches its preset value, and the counter will just roll over.

A special feature allows the 7 channels each to also toggle its own output based on the comparison results of other channels. Hence each channel potentially can have up to 8 toggle edges. The PWM signal generated can be output as a single-shot or continuous output.

The PWM counter also supports an external trigger. There are 6 GPIOs selectable for an external trigger. PWM channel 0 and channel 1 can double as a stereo 11.025 kHz or 22.050 kHz PCM audio channel. Once this feature is setup, the 16-bit or 8-bit PCM audio data can be downloaded to the PWM local FIFO which can hold up to 64 bytes stereo or 128 bytes mono audio data. The data is played back based on the pre-scaler and 16-bit counter, and is automatically scaled to fit in the playback period if necessary.

The PWM FIFO can generate a number of interrupts to support PCM playback. They are FIFO empty, full, half-full, overflow, and underflow. Each of these interrupts can be individually masked if required.

### Features

- Supports 7 PWM output channels.
- Supports single-shot or continuous PWM data output.
- Supports external GPIO trigger.
- Supports 16-bit / 8-bit stereo PCM audio data output.
- Controls PCM FIFO full, empty, half-empty, and over-flow / under-flow buffer management.
- Supports PCM volume control for audio playback.

## 4.18 Analog to Digital Converter (ADC)

The FT905/6/7/8 series has a low-power, high-speed, successive approximation Analog-to-Digital Converter (ADC) that supports a configurable 8-bit/10-bit resolution and superior maximum sampling frequencies of up to approximately 960 Kilo Samples Per-second (kS/s). This ADC accepts analog inputs ranging from the ground supplies to the power supplies. This ADC can be used in various low-power and medium-resolution applications.

### Features

- Configurable 8-bit/10-bit successive approximation ADC.
- Supports 7 channel input.
- Individual channels can be selected for conversion.
- Power-down mode support.
- Max conversion rate up to approximately 960 kS/s.
- Measurement range 0 to VCC3V3A, by default the range voltage is 10% off of VCC3V3A. See Table 5-7.
- INL: +/-2 LSB (max).
- DNL: +/-1 LSB (max).

## 4.19 Digital to Analog Converter (DAC)

The FT905/6/7/8 series has two 10-bit, 1 Mega Samples Per-second (MS/S) Digital-Analog converter (DAC). It includes digital logic for registering the DAC value and a unity-gain buffer capable of driving off-chip. The module can also be switched to a power-down state where it consumes a minimum amount of current. The maximum output value of the DAC is decided by the reference voltage at pin DAC\_REFP.

### Features

- Two 10-bit DACs.
- 10-bit R-2R DAC ladder structure.
- Buffered output.
- Power-down mode support.
- Programmable conversion rate, the maximum rate is 1MHz.
- Selectable output drive.
- INL: +/-2 LSB (max).
- DNL: +/-1 LSB (max).

## 4.20 General Purpose Input Output

The FT905/6/7/8 provides up to 42 configurable Input / Output pins controlled by GPIO registers. All pins have multiple functions with special peripheral connection. Separate registers allow setting or clearing any number of outputs simultaneously. All GPIO pins default to inputs with pull-down resistors enabled on reset except GPIO0/1/2 inputs with pull-up resistors enabled.

All GPIOs can function as an interrupt. The polarity can be either positive edge or negative edge if its interrupt capability is enabled. In the meantime, the GPIO pin must be configured as a GPIO input.

### Features

- All GPIOs default to inputs after reset (except GPIO0/1/2).
- Multi-function selection on GPIO pins.
- Pull-up/Pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.
- Direction control of individual bits.
- Supports GPIO input Schmitt trigger.
- Supports GPIO interrupt, where each enabled GPIO interrupt can be used to wake-up the system from power-down mode.

## 4.21 System Clocks

### 4.21.1 12MHz Oscillator

The oscillator generates a 12MHz reference frequency output to the clock multiplier PLL. The oscillator clock source comes from either an external 12MHz crystal or a 12MHz square wave clock. The external crystal is connected across XI/CLKIN and XIO in the configuration shown in Session [6.1](#). The optional external clock input is connected to XI/CLKIN only.

### 4.21.2 Phase Locked Loop

The internal PLL takes a 12 MHz clock input from a crystal oscillator. The PLL outputs 100 MHz system clock frequency to the CPU processor and other peripheral circuits. Each peripheral has an individual enable control signal to gate the clock source.

### 4.21.3 32.768 KHz RTC Oscillator

The RTC oscillator provides a clock to the RTC time counter. Either an external 32.768 KHz crystal or a 32.768 KHz square wave clock can be used as clock source. The external crystal is connected across RTC\_XI/RTC\_CLKIN and RTC\_XIO in the configuration shown in Session [6.2](#). The optional external clock input is connected to the RTC\_XI/RTC\_CLKIN pin directly.

### 4.21.4 Internal Slow Clock Oscillator

The FT905/6/7/8 internal slow clock oscillator provides at least 5ms slow clock source to generate an interrupt for the USB 2.0 device remote wake-up feature. A USB 2.0 device with remote wake-up capability may not generate resume signalling unless the bus has been continuously in the idle state for 5ms. For a detailed description of USB 2.0 suspend/resume, please refer to [USB 2.0 specification](#) chapter 7.1.7.7.

## **4.22 Power Management**

### **4.22.1 Power Supply**

The FT905/6/7/8 series may be operated with a single supply of +3.3V applied to VCCIO3V3, VUSB3V3, VETH3V3 and VCC3V3A pins. The +1.2V internal regulator VOUT1 provides the power to the core circuit after VCCIO3V3 power on and the system will generate a Power on Reset (POR) pulse when the output voltage rises above the POR threshold.

The second +1.2V internal regulator VOUT2 will provide the power to the Ethernet transceiver when VETH3V3 gets the power supply.

### **4.22.2 Power down mode**

Power down mode applies to the entire system. In the power down mode, the system 12MHz oscillator and PLL both switch off and the system clock to the core and all peripherals stop except for the RTC oscillator and internal regulator. The internal regulator retains the power for the core and RTC running. An interrupt from GPIO or wake-up events from the USB 2.0 device controller and host controller can wake-up the system from power down mode independently.

If the USB 2.0 host controller was used and the respective interrupt bit enabled before the system entered into power down mode, then the following events can wake-up the system.

- Remote wake-up interrupt to USB 2.0 host controller.
- USB device connected interrupt to USB 2.0 host controller.
- USB device disconnected interrupt to USB 2.0 host controller.
- USB 2.0 host controller detected the over-current (OC) protection event.

If the USB 2.0 device controller was used and the respective interrupt bit also enabled before the system entered into power down mode, the following events can wake-up the system.

- USB 2.0 device controllers detects connect interrupt.
- USB 2.0 device controllers detects disconnect interrupt.
- USB host issue reset signal to USB 2.0 device controller.
- USB host issue resume signal to USB 2.0 device controller.

## 5 Devices Characteristics and Ratings

### 5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT905/6/7/8 series devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

| Parameter   | Value   | Unit  |
|---|---|-------|
| Storage Temperature   | -65 to +150   | °C    |
| Floor Life (Out of Bag) At Factory Ambient<br>(30°C / 60% Relative Humidity)          | 168 Hours<br>(IPC/JEDEC J-STD-033A MSL Level 3<br>Compliant)* | Hours |
| Ambient Temperature (Power Applied)   | -40 to +85  | °C    |
| VCC3V3 Supply Voltage   | -0.5 to +4.6  | V     |
| DC Input Voltage – USB Host H_DP and H_DM   | -0.5 to +5  | V     |
| DC Input Voltage – USB Device D_DP and D_DM   | -0.5 to +5  | V     |
| DC Input Voltage – Ethernet TXON, TXOP, RXIN<br>and RXIP                              | -0.5 to +5.6  | V     |
| DC Input Voltage – 5V tolerance I/O cells (GPIOs<br>that are not shared with ADC/DAC) | -0.5 to +5.8  | V     |
| Others – 3V I/O cells (GPIOs that are shared<br>with ADC/DAC)                         | -0.5 to VCC3V3+0.5  | V     |

**Table 5-1 - Absolute Maximum Ratings**

\* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

## 5.2 DC Characteristics

### Electrical Characteristics (Ambient Temperature = -40°C to +85°C)

The typical values are obtained at room temperature ( $T_j = 25^\circ\text{C}$ ),  $V_{CC3V3} = 3.3\text{V}$ , and  $V_{CC1V2} = 1.2\text{V}$ .

| Parameter | Description                  | Minimum | Typical | Maximum | Units         | Conditions   |
|-----------|------------------------------|---------|---------|---------|---------------|--|
| VCCIO3V3  | I/O operating supply voltage | 2.97    | 3.3     | 3.63    | V             | Normal Operation                                   |
| $I_{cc1}$ | Power down current           | -       | 700     | -       | $\mu\text{A}$ | Power Down Mode                                    |
| $I_{cc2}$ | Idle current                 | -       | 42      | -       | mA            | Idle   |
| $I_{cc3}$ | System operating current*    | -       | 75      | -       | mA            | USB 2.0 Host controller high speed data transfer   |
|           |                              | -       | 75      | -       | mA            | USB 2.0 Device controller high speed data transfer |
|           |                              | -       | 100     | -       | mA            | 10/100 Mbit/s Ethernet transfer data               |
|           |                              | -       | 50      | -       | mA            | ADC / DAC Operation                                |
| VOUT1     | Internal LDO voltage         | -       | 1.2     | -       | V             | Normal Operation                                   |

**Table 5-2 - Operating Voltage and Current**

**Note:** The typical system operating current measured, based on each function, implements normal operation with the FT32 core active, and other peripherals kept idle.

### DC characteristics of I/O cells

| Parameter   | Description                                  | Minimum        | Typical | Maximum | Units            | Conditions                               |
|-------------|--|----------------|---------|---------|------------------|--|
| $V_{oh}$    | Output Voltage High                          | 2.4            | -       | -       | V                | $ I_{oh}  = 2\text{mA} \sim 16\text{mA}$ |
| $V_{ol}$    | Output Voltage Low                           | -              | -       | 0.4     | V                | $ I_{ol}  = 2\text{mA} \sim 16\text{mA}$ |
| $V_{opu}^*$ | Output pull-up Voltage for 5V tolerance I/Os | VCCIO3V3 - 0.9 | -       | -       | V                | $ I_{pu}  = 1\mu\text{A}$                |
| $V_{ih}$    | Input High Voltage                           | 2.0            | -       | -       | V                | LVTTL                                    |
| $V_{il}$    | Input Low Voltage                            | -              | -       | 0.8     | V                | LVTTL                                    |
| $V_{th}$    | Schmitt trigger positive threshold Voltage   | -              | 1.6     | 2.0     | V                | LVTTL                                    |
| $V_{tl}$    | Schmitt-trigger negative threshold Voltage   | 0.8            | 1.1     | -       | V                | LVTTL                                    |
| $R_{pu}$    | Input pull-up resistance equivalent          | 40             | 75      | 190     | $\text{K}\Omega$ | $V_{in} = 0\text{V}$                     |
| $R_{pd}$    | Input pull-down resistance equivalent        | 40             | 75      | 190     | $\text{K}\Omega$ | $V_{in} = V_{CCIO3V3}$                   |

|            |                       |   |         |   |         |                                     |
|------------|-----------------------|---|---------|---|---------|-------------------------------------|
| $I_{in}$   | Input leakage current | - | $\pm 1$ | - | $\mu A$ | $V_{in} = V_{CCIO3V3}$ or 0         |
|            |                       | - | $\pm 1$ | - | $\mu A$ | $V_{in} = 5V$ or 0                  |
| $C_{in}^*$ | Input Capacitance     | - | 2.8     | - | pF      | $V_{CCIO3V3}$ with 5V tolerance I/O |

**Table 5-3 - Digital I/O Pin Characteristics ( $V_{CCIO3V3} = +3.3V$ , Standard Drive Level)**

**Note:** This parameter indicates that the pull-up resistor for the 5V tolerance I/O cells cannot reach  $V_{CCIO3V3}$  DC level even without DC loading current.

$C_{in}$  includes the cell layout capacitance and pad capacitance.

### DC characteristics of USB I/O cells

| Parameter                                | Description  | Minimum | Typical | Maximum | Units | Conditions                       |
|--|--|---------|---------|---------|-------|----------------------------------|
| General characteristics                  |  |         |         |         |       |                                  |
| VUSB3V3                                  | USB power supply voltage                             | 2.97    | 3.3     | 3.63    | V     | Normal operation                 |
| VCC1V2*                                  | USB core supply voltage                              | 1.08    | 1.2     | 1.32    | V     | Normal operation                 |
| Input level for high speed               |  |         |         |         |       |                                  |
| V <sub>hscm</sub>                        | Voltage of high speed data signal in the common mode | -50     | -       | 500     | mV    | -                                |
| V <sub>hssq</sub>                        | High speed squelch detection threshold               | -       | -       | 100     | mV    | Squelch is detected              |
|  |  | 150     | -       | -       | mV    | Squelch is not detected          |
| V <sub>hdsdc</sub>                       | High speed disconnection detection threshold         | 625     | -       | -       | mV    | Disconnection is detected        |
|  |  | -       | -       | 525     | mV    | Disconnection is not detected    |
| Output level for high speed              |  |         |         |         |       |                                  |
| V <sub>hsoi</sub>                        | High speed idle output voltage (Differential)        | -10     | -       | 10      | mV    | -                                |
| V <sub>hsol</sub>                        | High speed low level output voltage (Differential)   | -10     | -       | 10      | mV    | -                                |
| V <sub>hsoh</sub>                        | High speed high level output voltage (Differential)  | -360    | -       | 400     | mV    | -                                |
| V <sub>chirpj</sub>                      | Chirp-J output voltage (Differential)                | 700     | -       | 1100    | mV    | -                                |
| V <sub>chirpk</sub>                      | Chirp-K output voltage (Differential)                | -900    | -       | -500    | mV    | -                                |
| Input level for full speed and low speed |  |         |         |         |       |                                  |
| V <sub>di</sub>                          | Differential input voltage                           | 0.2     | -       | -       | V     | V <sub>dp</sub> -V <sub>dm</sub> |

| Parameter  | Description                      | Minimum | Typical | Maximum | Units | Conditions                                     |
|--|----------------------------------|---------|---------|---------|-------|--|
|  | sensitivity                      |         |         |         |       |  |
| $V_{cm}$   | Differential common mode voltage | 0.8     | -       | 2.5     | V     | -  |
| $V_{se}$   | Single ended receiver threshold  | 0.8     | -       | 2.0     | V     | -  |
| <b>Output level for full speed and low speed</b> |                                  |         |         |         |       |  |
| $V_{ol}$   | Low level output voltage         | 0       | -       | 0.3     | V     | -  |
| $V_{oh}$   | High level output voltage        | 2.8     | -       | 3.6     | V     | -  |
| <b>Resistance</b>                                |                                  |         |         |         |       |  |
| $R_{drv}$  | Driver output impedance          | 40.5    | 45      | 49.5    | ohm   | Equivalent resistance used as an internal chip |

**Table 5-4 - USB I/O Pin (D\_DP/D\_DM, H\_DP/H\_DM) Characteristics**

**Note:** The VCC1V2 is the USB Host or Peripheral transceiver core power supply input which needs connected to an external +1.2V voltage power while the USB Host or Peripheral controller is active.

#### DC characteristics of Ethernet I/O cells

| Parameter                      | Description                                  | Minimum | Typical | Maximum | Units | Conditions          |
|--------------------------------|--|---------|---------|---------|-------|---------------------|
| <b>General characteristics</b> |  |         |         |         |       |                     |
| VETH3V3                        | Ethernet power supply voltage                | 2.97    | 3.3     | 3.63    | V     | Normal operation    |
| VOUT2*                         | Ethernet LDO voltage                         | -       | 1.2     | -       | V     | Normal operation    |
| Total dissipative power        | 10Base-TX mode (Including TX current)        | -       | -       | 510     | mW    | 10Base-TX mode      |
|                                | 10Base-TX mode (Excluding TX current)        | -       | -       | 147     | mW    | 10Base-TX mode      |
|                                | 100Base-TX mode (Including TX current)       | -       | -       | 310     | mW    | 100Base-TX mode     |
|                                | 100Base-TX mode (Excluding TX current)       | -       | -       | 165     | mW    | 100Base-TX mode     |
|                                | Auto-negotiation mode (Including TX current) | -       | -       | 550     | mW    | 100Base-TX mode     |
|                                | Auto-negotiation mode (Excluding TX current) | -       | -       | 187     | mW    | 100Base-TX mode     |
|                                | Power down mode                              | -       | -       | 10      | mW    | Ethernet power down |

**Table 5-5 - Ethernet I/O pin (TXON/TXOP, RXIN/RXIP) characteristics**

**Note:** The VOUT2 is the internal Regulator +1.2V voltage output which provide a power supply for the Ethernet transceiver.

#### DC characteristics of DAC I/O cells

| Parameter         | Description                     | Minimum | Typical | Maximum | Units       | Conditions                   |
|-------------------|---------------------------------|---------|---------|---------|-------------|------------------------------|
| VCC3V3A           | DAC power supply voltage        | 2.97    | 3.3     | 3.63    | V           | Normal Operation             |
| VREFP             | Reference voltage               | 0       | -       | VCC3V3A | V           | DCAP_REFP positive reference |
| RES               | Resolution                      | 10      | -       | -       | Bits        | -                            |
| INL               | Integral nonlinearity error     | -2      | -       | 2       | LSB         | VREFP = VCC3V3A              |
| DNL               | Differential nonlinearity error | -1      | -       | 1       | LSB         | VREFP = VCC3V3A              |
| -                 | Conversion latency              | -       | -       | 1       | Clock cycle | -                            |
| -                 | DAC reference impedance         | 150     | -       | 200     | K $\Omega$  | -                            |
| C <sub>LOAD</sub> | Output load: rated capacitance  | -       | -       | 10      | pF          | -                            |
| R <sub>LOAD</sub> | Output load: rated resistance   | 6.7     | -       | -       | K $\Omega$  | -                            |

**Table 5-6 - DAC I/O pin (DAC\_REFP, DAC0/1) characteristics**

#### DC characteristics of ADC I/O cells

| Parameter  | Description                     | Minimum | Typical    | Maximum | Units | Conditions                     |
|------------|---------------------------------|---------|------------|---------|-------|--------------------------------|
| VCC3V3A    | Analog power supply voltage     | 2.97    | 3.3        | 3.63    | V     | Normal operation               |
| XAIN       | Analog input range              | 0       | -          | VCC3V3A | V     | -                              |
| RES        | Resolution                      | -       | 10         | -       | Bit   | -                              |
| INL        | Integral nonlinearity error     | -3      | 0.56/-1.05 | 2       | LSB   | 10%-90% of VCC3V3A Reference   |
|            |                                 | -4      | 0.56/-1.05 | 2       | LSB   | Rail-to-Rail VCC3V3A reference |
| DNL        | Differential nonlinearity error | -1      | 0.66/-0.58 | 1       | LSB   | -                              |
| Xsampleclk | Sample rate                     | -       | -          | 960     | KSPS  | -                              |

**Table 5-7 - ADC I/O Pin Characteristics**

## 5.3 AC Characteristics

AC Characteristics (Ambient Temperature = -40°C to +85°C)

### System clock dynamic characteristics

| Parameter                     | Value   |         |         | Unit |
|-------------------------------|---------|---------|---------|------|
|                               | Minimum | Typical | Maximum |      |
| Crystal oscillator            |         |         |         |      |
| Clock frequency               | -       | 12.00   | -       | MHz  |
| Clock accuracy                | -       | -       | 50      | ppm  |
| Period jitter                 | -       | -       | 120     | ps   |
| Cycle-to-cycle jitter         | -       | -       | 150     | ps   |
| Long-term jitter              | -       | -       | 200     | ps   |
| External clock input          |         |         |         |      |
| external clock jitter         | -       | -       | 500     | Ps   |
| clock duty cycle              | 45      | 50      | 55      | %    |
| Input voltage on pin XI/CLKIN | -       | 3.3     | -       | V    |

**Table 5-8 - System clock characteristics**

### RTC clock dynamic characteristics

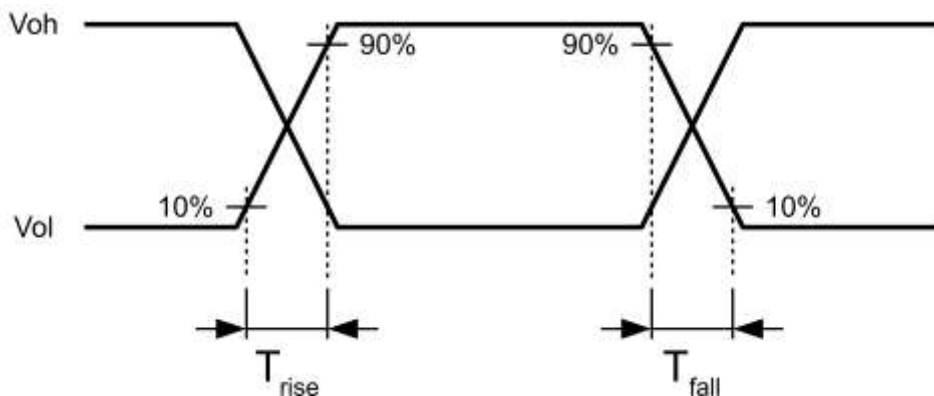
| Parameter                                | Value   |         |         | Unit |
|--|---------|---------|---------|------|
|  | Minimum | Typical | Maximum |      |
| Crystal oscillator                       |         |         |         |      |
| Clock frequency                          | -       | 32768   | -       | Hz   |
| External clock input                     |         |         |         |      |
| external clock jitter                    | -       | -       | 500     | Ps   |
| clock duty cycle                         | 45      | 50      | 55      | %    |
| Startup time                             | -       | 0.5     | 5       | S    |
| Input voltage on pin<br>RTC_XI/RTC_CLKIN | -       | 1.2     | -       | V    |

**Table 5-9 - RTC clock characteristics**

### Analog USB I/O pins dynamic characteristics

| Parameter                                   | Description                          | Minimum | Typical | Maximum | Units | Conditions                                      |
|---|--------------------------------------|---------|---------|---------|-------|---|
| <b>Driver characteristic for high speed</b> |                                      |         |         |         |       |   |
| $T_{hsr}$                                   | High speed differential rise time    | 500     | -       | -       | ps    | -   |
| $T_{hsf}$                                   | High speed differential fall time    | 500     | -       | -       | ps    | -   |
| <b>Driver characteristic for full speed</b> |                                      |         |         |         |       |   |
| $T_{fr}$                                    | Rise time of DP/DM                   | 4       | -       | 20      | ns    | CI=50pF<br>10%~90% of  Voh-Vol                  |
| $T_{ff}$                                    | Fall time of DP/DM                   | 4       | -       | 20      | ns    | CI=50pF<br>10%~90% of  Voh-Vol                  |
| $T_{frma}$                                  | Differential rise/fall time matching | 90      | -       | 110     | %     | The first transition exclude from the idle mode |
| <b>Driver characteristic for low speed</b>  |                                      |         |         |         |       |   |
| $T_{lr}$                                    | Rise time of DP/DM                   | 75      | -       | 300     | ns    | CI=200pF~600pF<br>10%~90% of  Voh-Vol           |
| $T_{lf}$                                    | Fall time of DP/DM                   | 75      | -       | 300     | ns    | CI=200pF~600pF<br>10%~90% of  Voh-Vol           |
| $T_{lrma}$                                  | Differential rise/fall time matching | 80      | -       | 125     | %     | The first transition exclude from the idle mode |

**Table 5-10 - Analog I/O pins (D\_DP/D\_DM, H\_DP/H\_DM) characteristics**

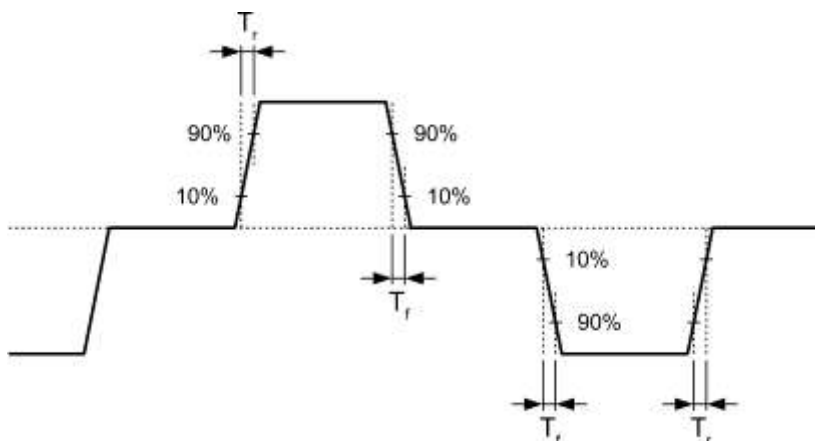


**Figure 5-1 - USB Rise and Fall Times for DP/DM**

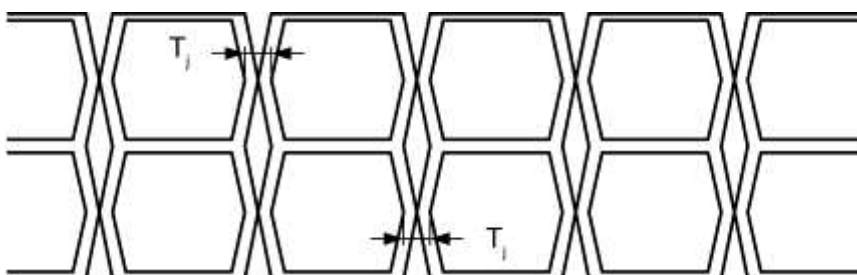
### Analog Ethernet I/O pins dynamic characteristics

| Parameter                          | Description                              | Minimum | Typical | Maximum | Units | Conditions                             |
|------------------------------------|--|---------|---------|---------|-------|--|
| <b>Transmitter characteristics</b> |  |         |         |         |       |  |
| $2 \times V_{txa}$                 | Peak-to-peak differential output voltage | 1.9     | 2.0     | 2.1     | V     | 100Base-TX mode                        |
| $T_r / T_f$                        | Signal rise/fall time                    | 3.0     | 4.0     | 5.0     | ns    | 100Base-TX mode                        |
| -                                  | Output jitter                            | -       | -       | 1.4     | ns    | 100Base-TX mode, scrambled idle signal |
| $V_{txov}$                         | Overshoot                                | -       | -       | 5.0     | %     | 100Base-TX mode                        |
| <b>Receiver characteristics</b>    |  |         |         |         |       |  |
| -                                  | Common-mode input voltage                | 2.97    | 3.3     | 3.63    | V     | -                                      |
| -                                  | Error-free cable length                  | 100     | -       | -       | meter | -                                      |

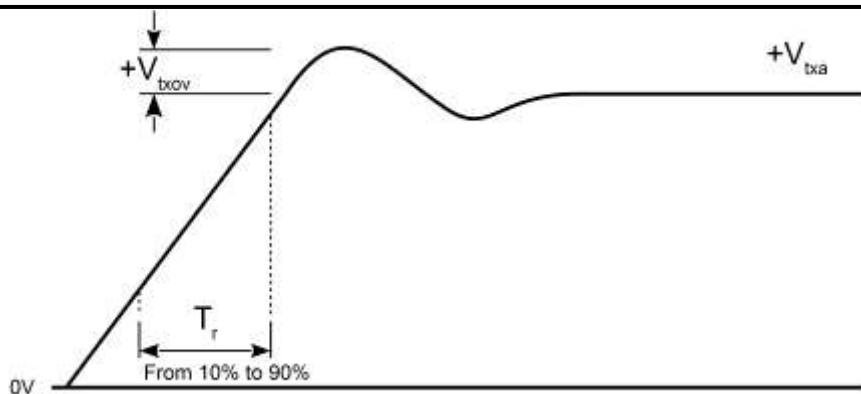
**Table 5-11 - Analog I/O pins (TXON/TXOP, RXIN/RXIP) characteristics**



**Figure 5-2 - 100Base-TX  $T_{r/f}$  Timing**

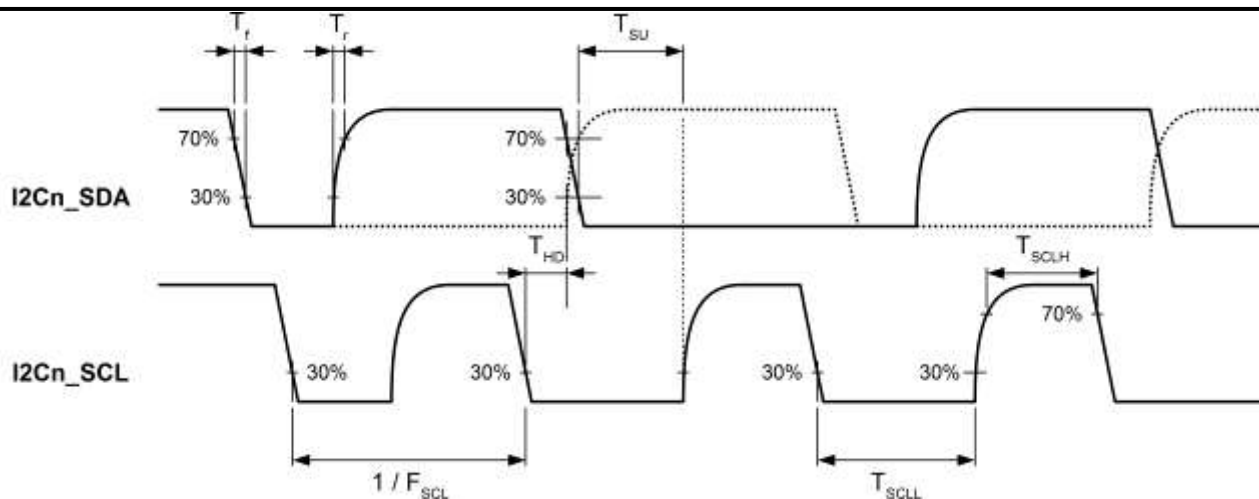
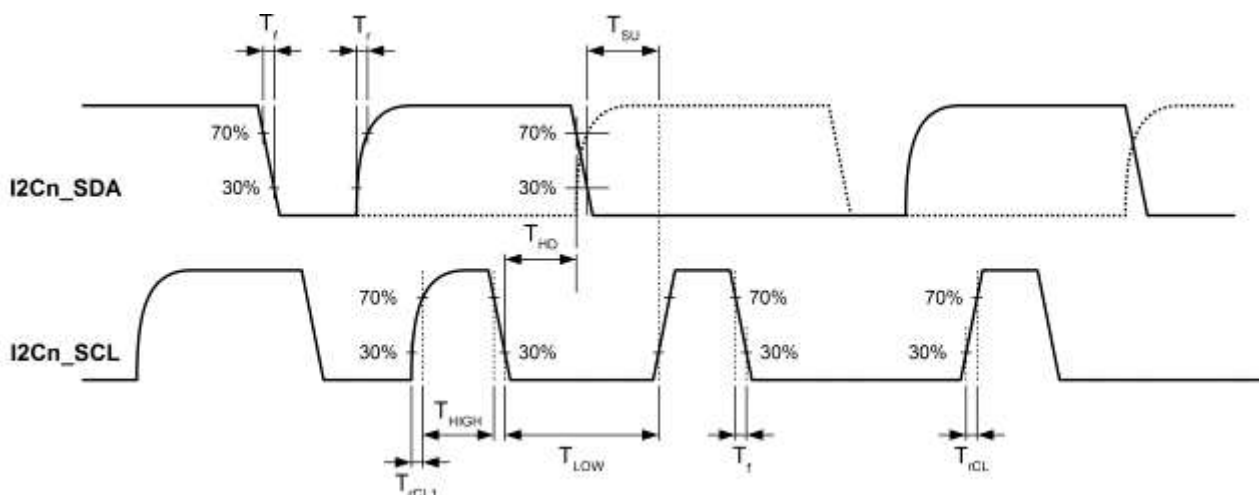


**Figure 5-3 - 100Base-TX Jitter Timing**


**Figure 5-4 - 100Base-TX Transmission Waveform**
**I<sup>2</sup>C Bus I/O pins dynamic characteristics ( $V_{cc}$  (I/O) = 3.3V)**

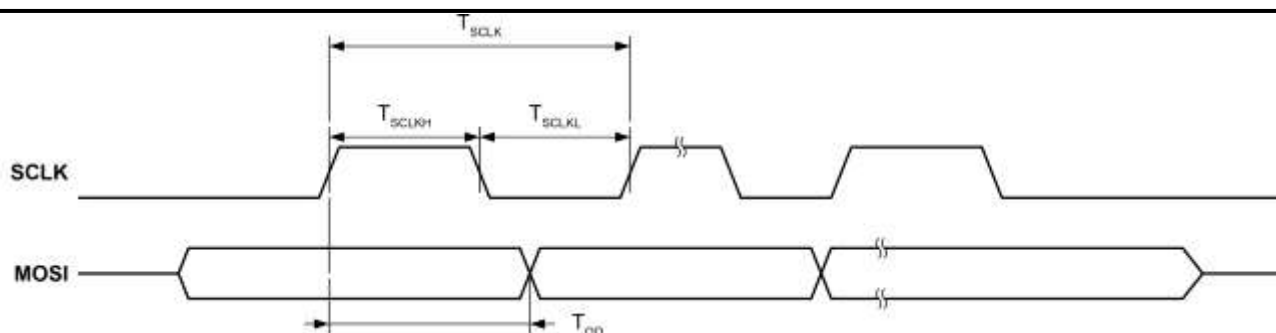
| Parameter  | Description                                      | Standard mode (SM) |      | Fast mode (FM) |     | Fast mode Plus (FM+) |      | High Speed mode (HS) |                       | Unit    |
|------------|--|--------------------|------|----------------|-----|----------------------|------|----------------------|-----------------------|---------|
|            |  | Min                | Max  | Min            | Max | Min                  | Max  | Min                  | Max                   |         |
| $F_{SCL}$  | SCL clock frequency                              | 0                  | 100  | 0              | 400 | 0                    | 1000 | 0                    | 3400                  | kHz     |
| $T_{SCLL}$ | SCL clock low period                             | 4.7                | -    | 1.3            | -   | 0.5                  | -    | 0.320                | -                     | $\mu$ s |
| $T_{SCLH}$ | SCL clock high period                            | 4.0                | -    | 0.6            | -   | 0.26                 | -    | 0.120                | -                     | $\mu$ s |
| $T_{SU}$   | data setup time                                  | 250                | -    | 100            | -   | 50                   | -    | 10                   | -                     | ns      |
| $T_{HD}$   | data hold time                                   | 0                  | -    | 0              | -   | 0                    | -    | 0                    | 150                   | ns      |
| $T_r$      | rise time  | -                  | 1000 | -              | 300 | -                    | 120  | 20                   | 160                   | ns      |
| $T_{rCL1}$ | rise time 1 <sup>st</sup> clock after $S_r$ (HS) |                    |      |                |     |                      |      | 20                   | 160                   | ns      |
| $T_{rCL}$  | rise time clock (HS)                             |                    |      |                |     |                      |      | 20                   | 80                    | ns      |
| $T_f$      | fall time  | -                  | 300  | -              | 300 | -                    | 300  | 20                   | 80 (SCL)<br>160 (SDA) | ns      |

**Table 5-12 - I<sup>2</sup>C I/O pins (I2C0\_SCL/SDA, I2C1\_SCL/SDA) characteristics**

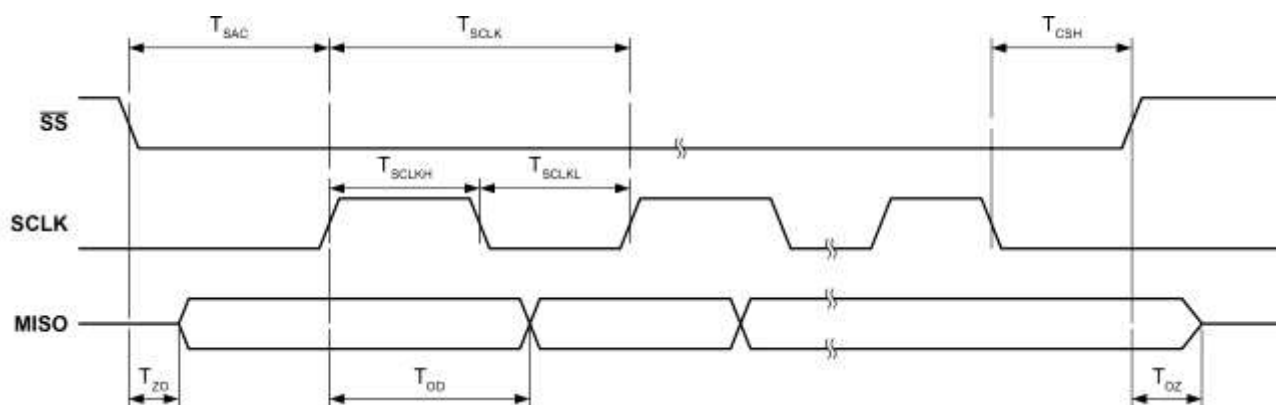

**Figure 5-5 - Definition of I<sup>2</sup>C Timing F/S mode**

**Figure 5-6 - Definition of I<sup>2</sup>C Timing HS mode**
**SPI Master I/O pins dynamic characteristics ( $V_{cc}$  (I/O) = 3.3V)**

| Parameter   | Description             | Min | Typ | Max | Unit |
|-------------|-------------------------|-----|-----|-----|------|
| $T_{SCLK}$  | SPI clock period        | 20  |     |     | ns   |
| $T_{SCLKL}$ | SPI clock low duration  | 19  |     |     | ns   |
| $T_{SCLKH}$ | SPI clock high duration | 19  |     |     | ns   |
| $T_{OD}$    | output data delay       | 19  |     | 20  | ns   |

**Table 5-13 - SPI I/O pins (SPIM\_CLK/MOSI/MISO/SS0/SS1/SS2/SS3) characteristics**


**Figure 5-7 - Definition of SPI Master Timing Mode 0**
**SPI Slave I/O pins dynamic characteristics ( $V_{CC} (I/O) = 3.3V$ )**

| Parameter   | Description             | Min | Typ | Max | Unit |
|-------------|-------------------------|-----|-----|-----|------|
| $T_{SCLK}$  | SPI clock period        | 40  |     |     | ns   |
| $T_{SCLKL}$ | SPI clock low duration  | 16  |     |     | ns   |
| $T_{SCLKH}$ | SPI clock high duration | 16  |     |     | ns   |
| $T_{SAC}$   | SPI access time         | 20  |     |     | ns   |
| $T_{OD}$    | output data delay       | 7   |     | 27  | ns   |
| $T_{ZO}$    | output enable delay     | 10  |     |     | ns   |
| $T_{OZ}$    | output disable delay    | 10  |     |     | ns   |
| $T_{CSH}$   | CS hold time            | 0   |     |     | ns   |

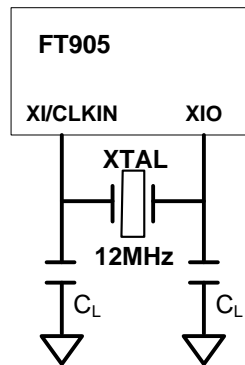
**Table 5-14 - SPI I/O pins (SPIS0\_CLK/MOSI/MISO/SS, SPIS1\_CLK/MOSI/MISO/SS) characteristics**

**Figure 5-8 - Definition of SPI Slave Timing Mode 0**

## 6 Application Information

### 6.1 Crystal Oscillator

The crystal oscillator operates at a frequency of 12MHz. The oscillator can operate in one of two following configuration.

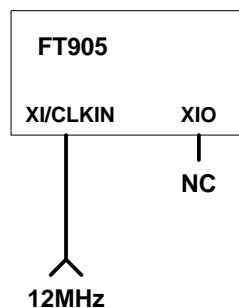
#### 6.1.1 Crystal Oscillator Application Circuit



**Figure 6-1 - Crystal oscillator connection**

Feedback resistance is integrated on chip; only a crystal and capacitors C<sub>L</sub> need to be connected externally. With the proper selection of crystal, the oscillator circuit can generate better quality signals for the FT905/6/7/8. Parameter C<sub>L</sub> is typically 27pF but should be checked with the crystal manufacturer.

#### 6.1.2 External Clock Input



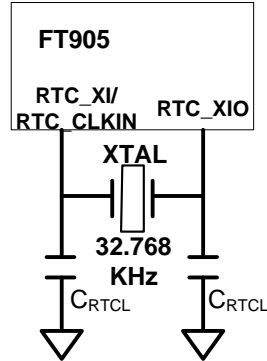
**Figure 6-2 - External clock input**

The 12MHz input clock signal connects XI/CLKIN to the internal oscillator directly. The XIO pin can be left unterminated.

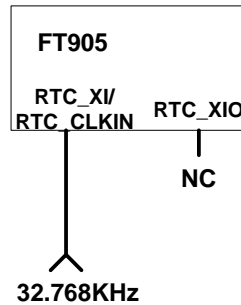
## 6.2 RTC Oscillator

In the RTC oscillator circuit Figure 6-3, only a 32.768 kHz crystal and capacitors  $C_{RTCL}$  need to be connected externally. The parameter  $C_{RTCL}$  should be checked with the crystal manufacturer.

An external input clock Figure 6-4 can be connected to RTC\_XI/RTC\_CLKIN if RTC\_XIO is left open.



**Figure 6-3 - RTC 32.768 KHz oscillator connection**



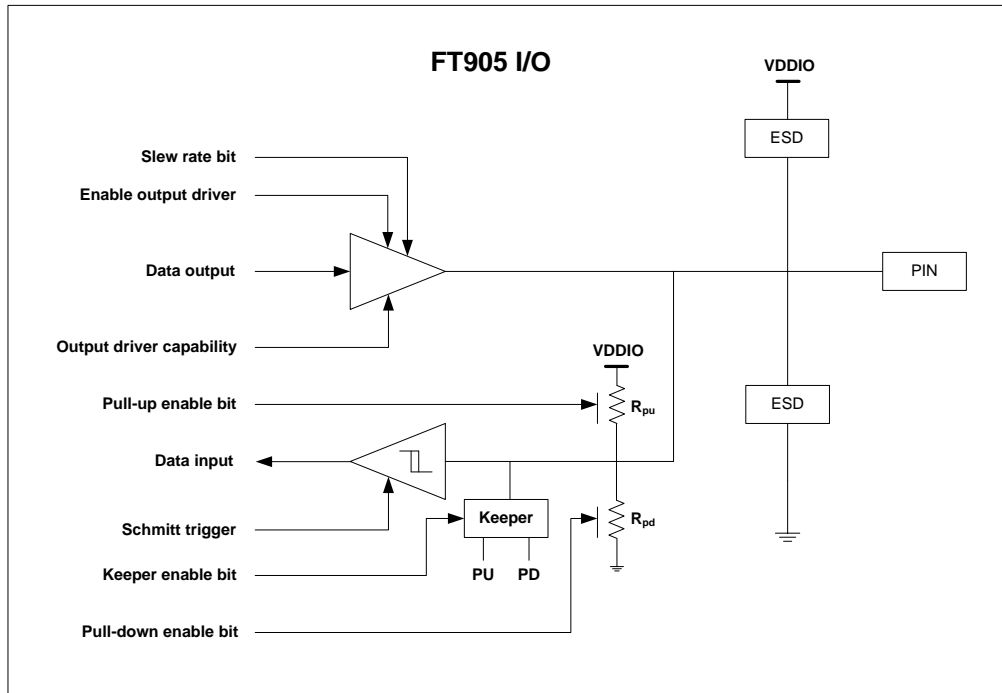
**Figure 6-4 - External 32.768 KHz clock input**

## 6.3 Standard I/O Pin Configuration

Figure 6-5 shows the possible pin modes for standard I/O pins with multiplex functions:

- Output driver enabled
- Output driver capability control
- Output slew rate control
- Open drain output
- Input with pull-up enabled
- Input with pull-down enabled
- Input with keeper enabled
- Input with Schmitt trigger

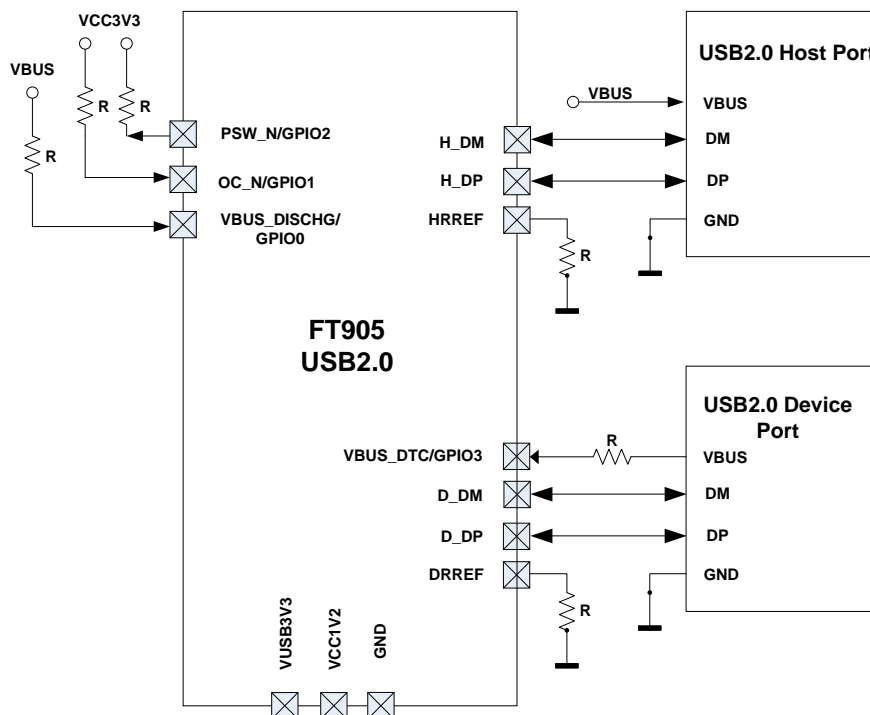
The default configuration for standard I/O pins is input with pull-down enabled except GPIO 0/1/2. All I/O pins have ESD protection.



**Figure 6-5 - Standard I/O pin configuration**

## 6.4 USB 2.0 Device and Host Interface

The example diagram in Figure 6-6 shows the FT905/6/7/8 series supporting one USB 2.0 host port and one USB 2.0 device port, which makes the FT905/6/7/8 system data transfer possible via USB.



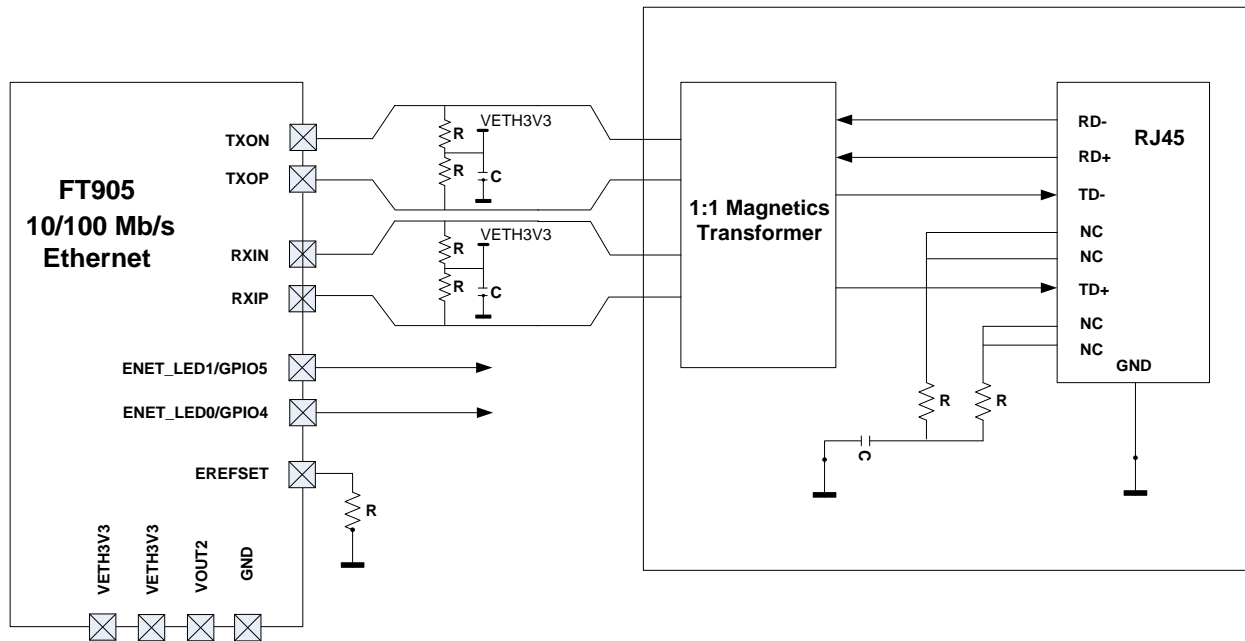
**Figure 6-6 – USB 2.0 ports connection**

The FT905/6/7/8 System shall provide I/O power (+3.3V supply) on VUSB3V3 and core power (+1.2V supply) on VCC1V2 for the USB 2.0 device/host controller. The internal band-gap gets reference voltage from DRREF or HRREF with an external reference resistor R (12 K $\Omega$   $\pm$ 1%) respective connected to GND.

The USB 2.0 host controller will provide +5V power voltage output for VBUS and go through PSW\_N signal to control power switching on/off.

## 6.5 10/100 Mb/s Ethernet Interface

Figure 6-7 shows the 10/100 Mb/s Ethernet port configuration via the transmit (TXON & TXOP) and receive (RXIN & RXIP) differential pair pins.



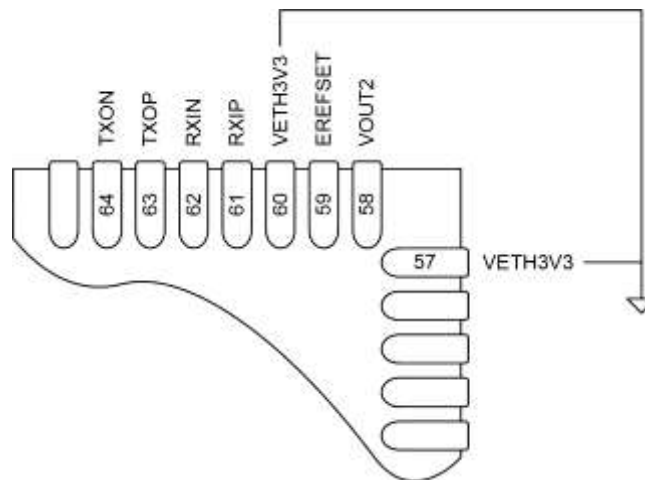
**Figure 6-7 - 10/100 Mb/s Ethernet interface**

The FT905/6/7/8 Ethernet connection to a termination network should go through a 1:1 magnetics transformer and an RJ-45. For space saving, the magnetics and RJ-45 may be a single integrated component. The system shall provide +3.3V power supply for VETH3V3. The internal Regulator will generate +1.2V output on VOUT2. The EREFSET connects an external resistor R (12.3 K $\Omega$   $\pm$ 1%) to GND to provide a reference voltage for the Ethernet transceiver.

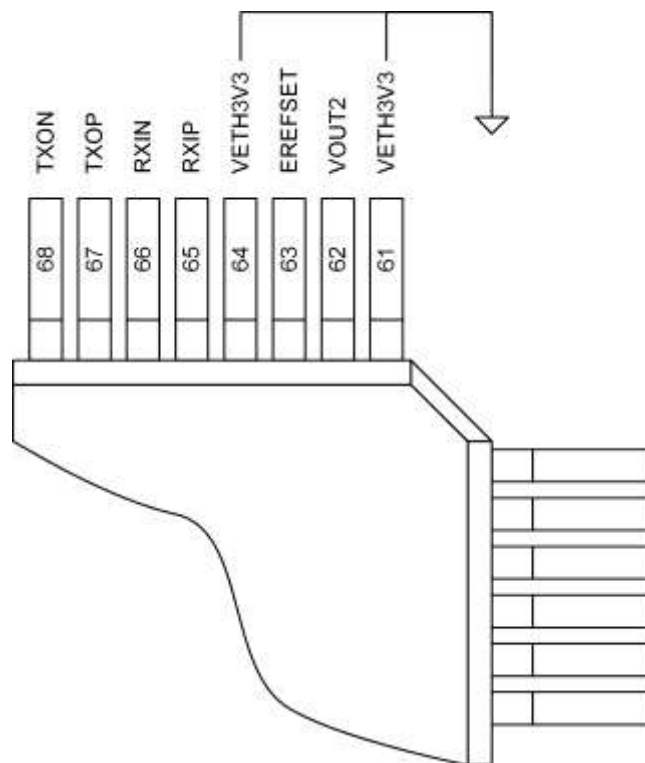
There are two Ethernet LEDs output for TX/RX transmission, Full-duplex/Half-duplex, Collision, Link or 10/100 Mb/s Speed indication. The required function should be set in the chip registers before using the LED indicator.

## 6.6 Ethernet Connection when Unused (FT905 & FT906)

If the Ethernet peripheral is not used in the end application, connect VETH3V3 to ground, see Figure 6-8 and Figure 6-9.



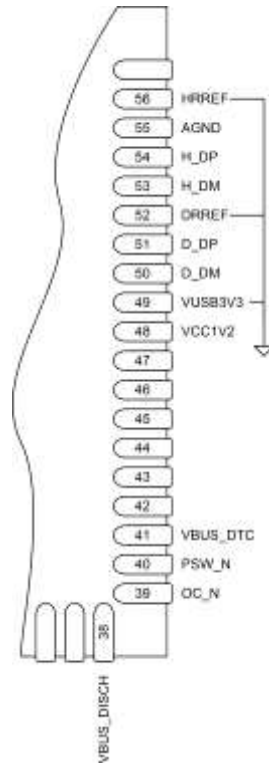
**Figure 6-8 - Unused Ethernet Connection (QFN)**



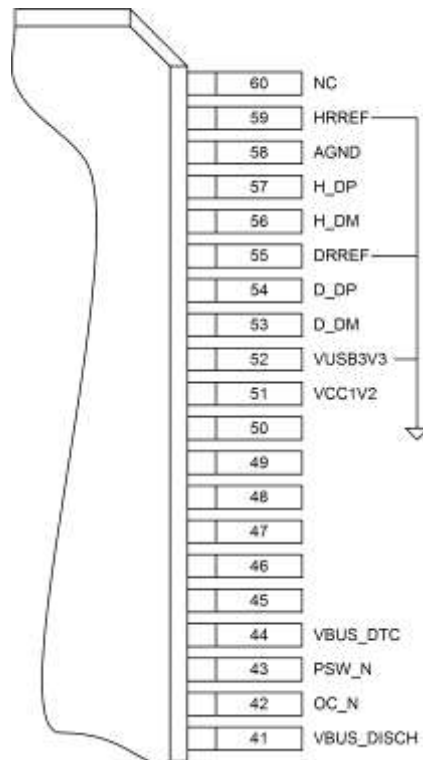
**Figure 6-9 - Unused Ethernet Connection (LQFP)**

## 6.7 USB Connection when Unused (FT905/6/7/8)

If the USB peripheral (Host and Device) is not used in the end application, connect VUSB3V3, HRREF, and DRREF to ground, see Figure 6-10 and Figure 6-11.



**Figure 6-10 - Unused USB Connection (QFN)**

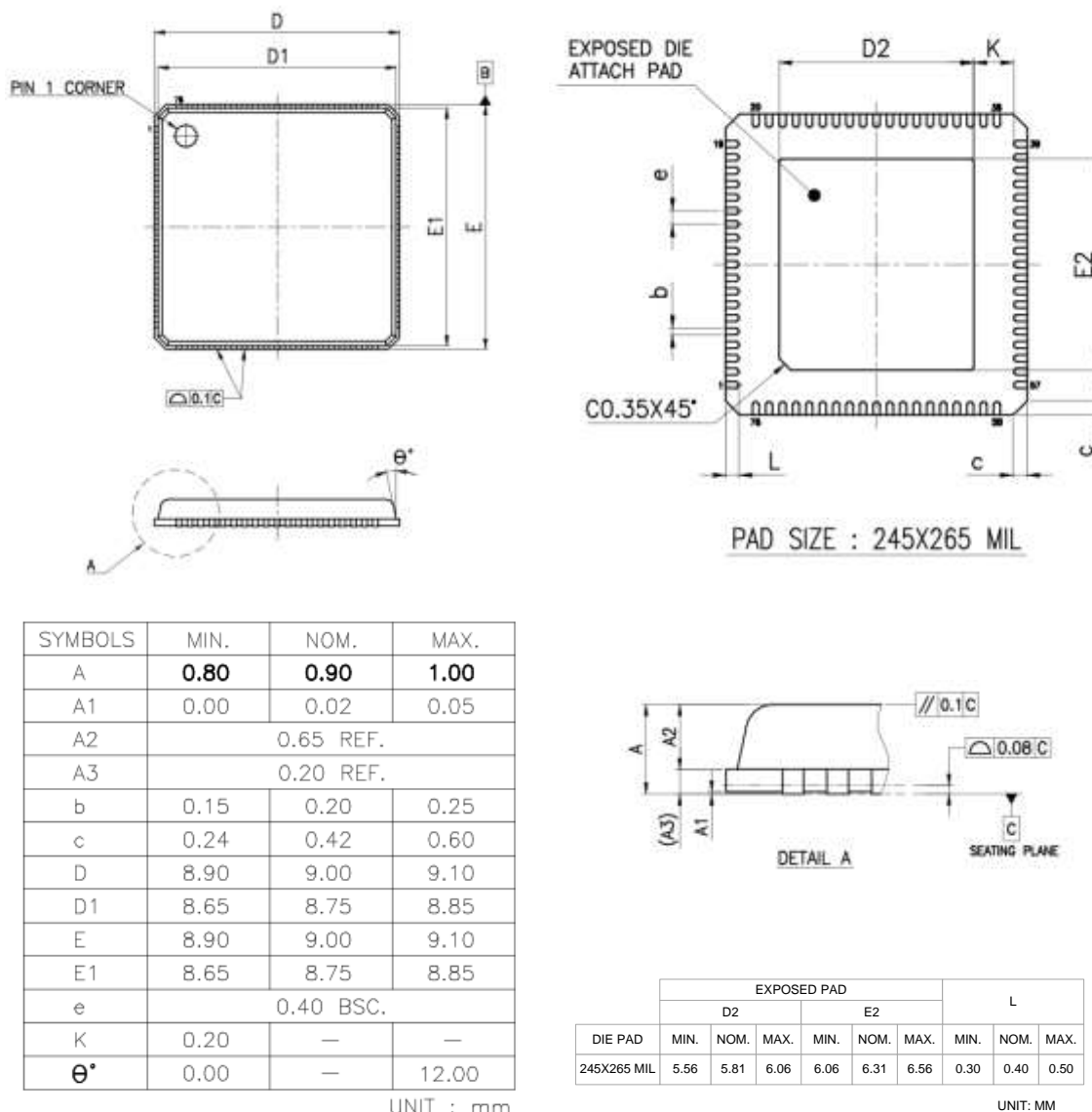


**Figure 6-11 - Unused USB Connection (LQFP)**

## 7 Package Parameters

The FT905/6/7/8 series is available in two different packages. The FT905Q/FT906Q/FT907Q/FT908Q is the QFN-76 package and the FT905L/FT906L/FT907L/FT908L is LQFP-80 package. The dimensions, markings and solder reflow profile for all packages are described in the following sections.

### 7.1 QFN-76 Package Dimensions



**Figure 7-1 - QFN-76 Package Dimensions**

**Note:** On the underside of the package, the exposed thermal pad should be connected to GND.

## 7.2 QFN-76 Device Marking

### FT90XQ Top Side

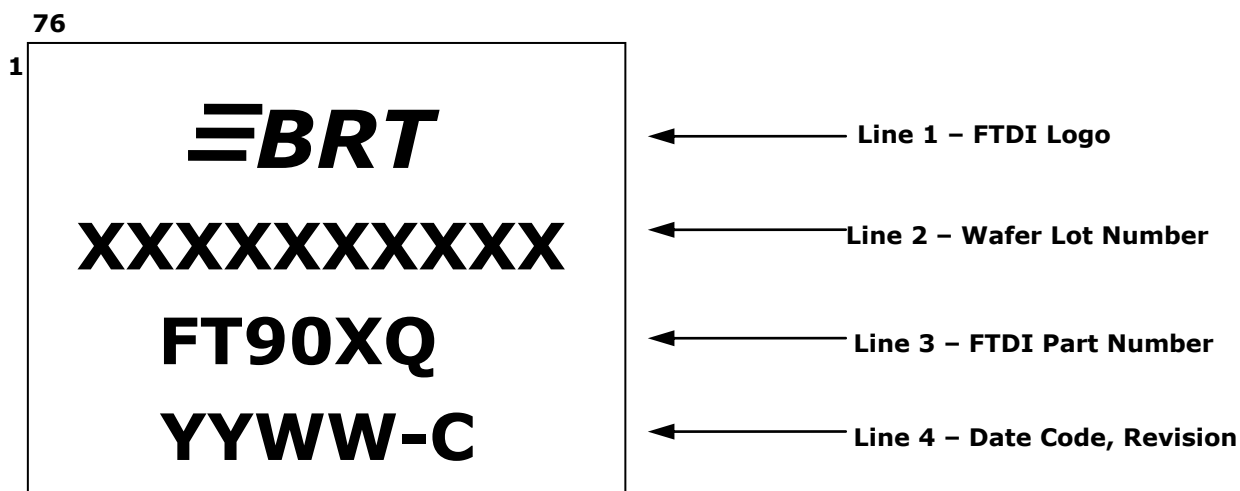


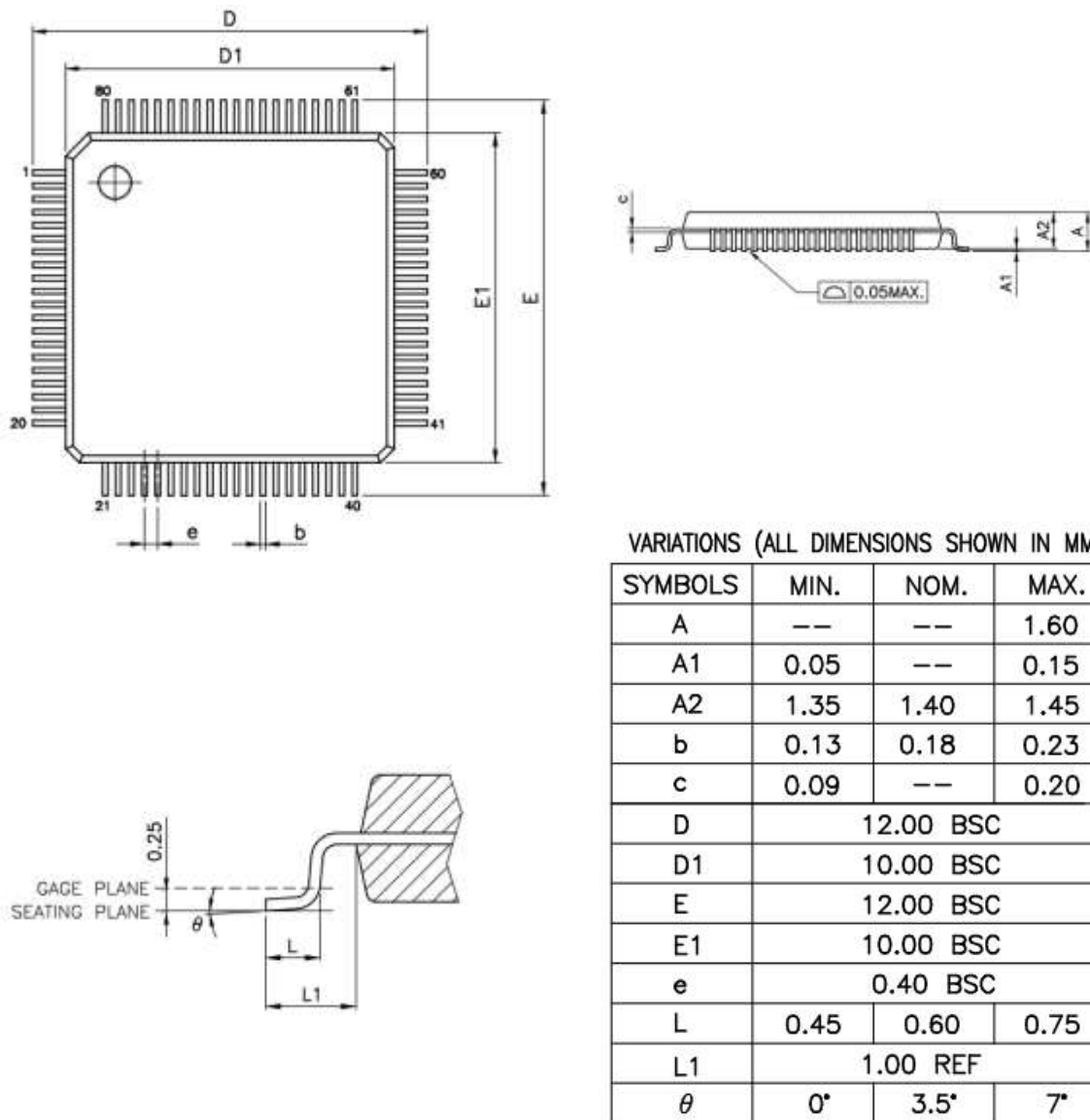
Figure 7-2 - FT90XQ Top side

#### Notes:

1. FT90XQ symbol stands for FT905Q, FT906Q, FT907Q and FT908Q.
2. YYWW = Date Code, where YY is year and WW is week number and following character B indicates the silicon revision B.
3. Marking alignment should be centre justified.
4. Laser marking should be used.

All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex).

## 7.3 LQFP-80 Package Dimensions



**Figure 7-3 - LQFP-80 Package Dimensions**

## 7.4 LQFP-80 Device Marking

### FT90XL Top Side

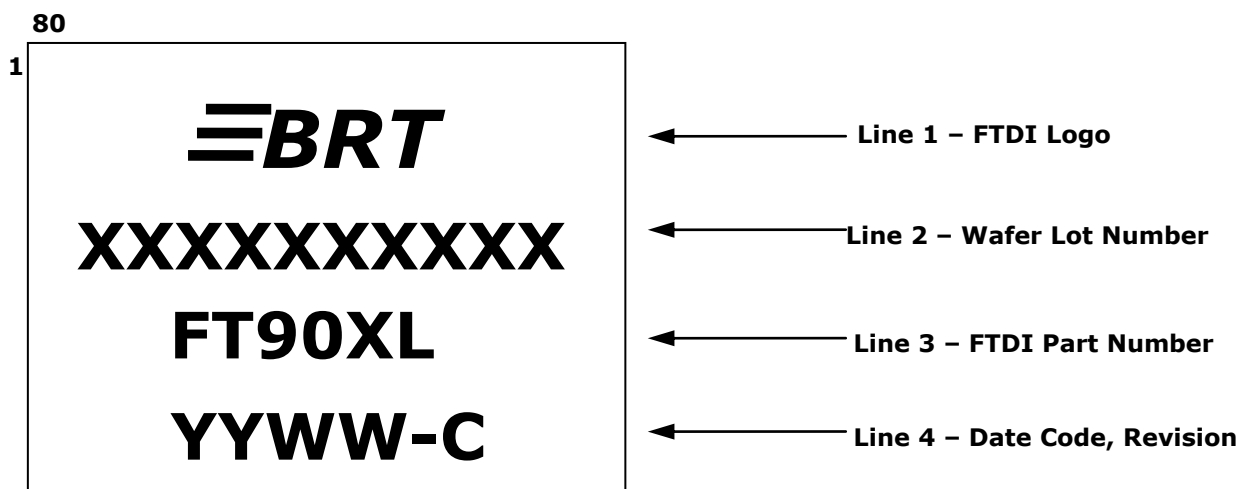


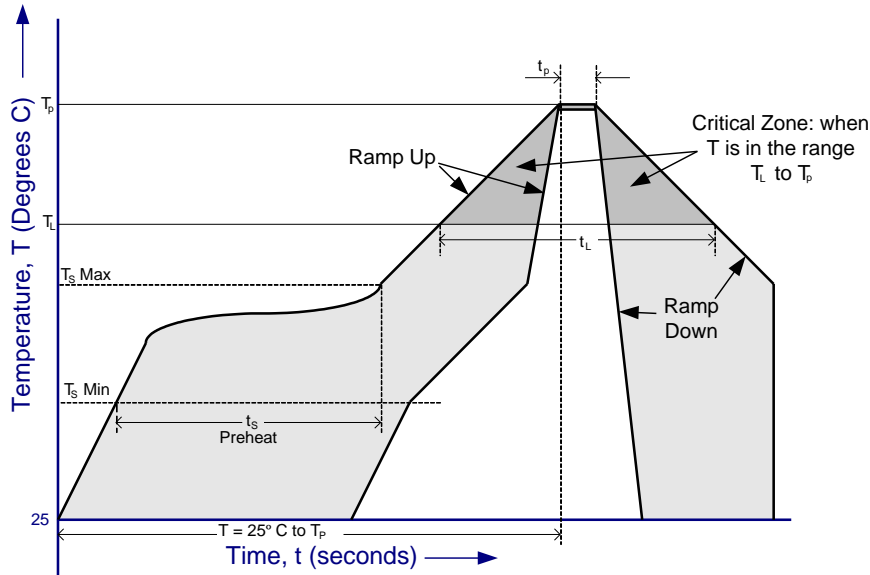
Figure 7-4 - FT90XL Top side

#### Notes:

1. FT90XL symbol stands for FT905L, FT906L, FT907L and FT908L.
2. YYWW = Date Code, where YY is year and WW is week number and following character B indicates the silicon revision B.
3. Marking alignment should be centre justified.
4. Laser marking should be used.
5. All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex).

## 7.5 Solder Reflow Profile

The FT905/6/7/8 series is supplied in Pb free QFN-76 package and LQFP-80 package. The recommended solder reflow profile for all packages options is shown in Figure 7-5.



**Figure 7-5 - FT905 Solder Reflow Profile**

The recommended values for the solder reflow profile are detailed in Table 7-1. Values are shown for both a completely Pb free solder process (i.e. the FT905 is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT905 is used with non-Pb free solder).

| Profile Feature  | Pb Free Solder Process              | Non-Pb Free Solder Process          |
|--|-------------------------------------|-------------------------------------|
| Average Ramp Up Rate (T <sub>s</sub> to T <sub>p</sub> )   | 3°C / second Max.                   | 3°C / Second Max.                   |
| Preheat<br>- Temperature Min (T <sub>s</sub> Min.)<br>- Temperature Max (T <sub>s</sub> Max.)<br>- Time (t <sub>s</sub> Min to t <sub>s</sub> Max) | 150°C<br>200°C<br>60 to 120 seconds | 100°C<br>150°C<br>60 to 120 seconds |
| Time Maintained Above Critical Temperature<br>T <sub>L</sub> :<br>- Temperature (T <sub>L</sub> )<br>- Time (t <sub>L</sub> )                      | 217°C<br>60 to 150 seconds          | 183°C 60 to 150 seconds             |
| Peak Temperature (T <sub>p</sub> )   | 260°C                               | 240°C                               |
| Time within 5°C of actual Peak Temperature<br>(t <sub>p</sub> )  | 20 to 40 seconds                    | 20 to 40 seconds                    |
| Ramp Down Rate   | 6°C / second Max.                   | 6°C / second Max.                   |
| Time for T= 25°C to Peak Temperature, T <sub>p</sub>   | 8 minutes Max.                      | 6 minutes Max.                      |

**Table 7-1 - Reflow Profile Parameter Values**

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## Appendix A – References

### Document References

[FT90x Product Page](#)

[AN\\_324 FT9xx User Manual](#)

[BRT AN\\_020 FT90x Revision C User Manual](#)

[BRT AN\\_019 Migration Guide Moving from FT90x Revision B to FT90x Revision C](#)

AN\_341 FT32 Technical Manual (available under NDA. Contact Bridgetek for more information)

[USB2.0 Specification](#)

[Battery Charging Specification Revision 1.2 \(BC 1.2\)](#)

### Acronyms and Abbreviations

| Terms | Description                    |
|-------|--------------------------------|
| ADC   | Analog-to-Digital Converter    |
| BCD   | Battery Charge Device          |
| CAN   | Controller Area Network        |
| CDP   | Charging Downstream Port       |
| DAC   | Digital-to-Analog Converter    |
| DAQ   | Data Acquisition               |
| DCP   | Dedicated Charging Port        |
| DNL   | Differential Nonlinearity      |
| FCS   | Ethernet Frame Check Sequence  |
| FIFO  | First In First Out             |
| GPIO  | General Purpose Input / Output |
| INL   | Integral Nonlinearity          |
| I/O   | Input / Output                 |
| LQFP  | Low profile Quad Flat Package  |
| LSB   | Least Significant Bit          |

| Terms | Description                                 |
|-------|---|
| MSPS  | Mega Samples Per-Second                     |
| NMI   | Non-Maskable Interrupt input                |
| OTP   | One-Time Programmable (memory)              |
| POR   | Power On Reset                              |
| PWM   | Pulse Width Modulator                       |
| QFN   | Quad Flat No-Lead                           |
| RTC   | Real Time Clock                             |
| SDP   | Standard Downstream Port                    |
| SPI   | Serial Peripheral Interface                 |
| UART  | Universal Asynchronous Receiver/Transmitter |
| USB   | Universal Serial Bus                        |
| NDA   | Non-Disclosure Agreement                    |

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## Appendix C - Revision History

Document Title: FT905/6/7/8 Revision C Embedded Microcontroller Datasheet  
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Clearance No.: BRT#100  
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| Revision    | Changes         | Date       |
|-------------|-----------------|------------|
| Version 1.0 | Initial Release | 2017-11-01 |

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