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Core Facts

Provided with Core	
Documentation	Reference Design Manual Demo Instruction Manual
Design File Formats	Encrypted HDL
Instantiation Templates	VHDL
Reference Designs & Application Notes	QuartusII Project, See Reference Design Manual
Additional Items	Demo on ArriaV GX board, Arria10 GX board, and Cyclone10 GX board
Support	
Support Provided by Design Gateway Co., Ltd.	

Features

- Simple user interface by dgIF typeS
- Support four commands, i.e. IDENTIFY DEVICE, SECURITY ERASE UNIT, WRITE DMA (EXT), and READ DMA (EXT)
- SATA application layer, transaction layer and link layer by hardware logic
- No need for external memory and CPU
- Compliant with the Serial ATA specification revision 3.0
- 2 x 4Kbyte FIFO for internal buffer
- Support SATA-III Speed by using 150 MHz for SATA clock and higher frequency for User clock
- Free HDL code of SATA3 PHY and the reference design in release stuff
- Reference design by using AB12-HSMCRAID or AB09-FMCRAID adapter board from Design Gateway

Table 1: Example Implementation Statistics

Family	Example Device	Fmax (MHz)	ALMs	Registers[1]	Block Memory Bit	Transceiver[3]	Design Tools
ArriaV GX	5AGXFB3H4F35C4	285	1054	1814	33,792	1	QuartusII 16.0
Arria 10 GX	10AX115S2F45I2SG	434	1086	1772	33,792	1	QuartusII 16.0
Cyclone 10 GX	10CX220YF780E5G	434	1088	1760	33,792	1	QuartusII 18.0

Notes:

1) Actual logic resource dependent on percentage of unrelated logic

2) Transceiver is not used in the IP core, but they are used in SATA3 PHY design.

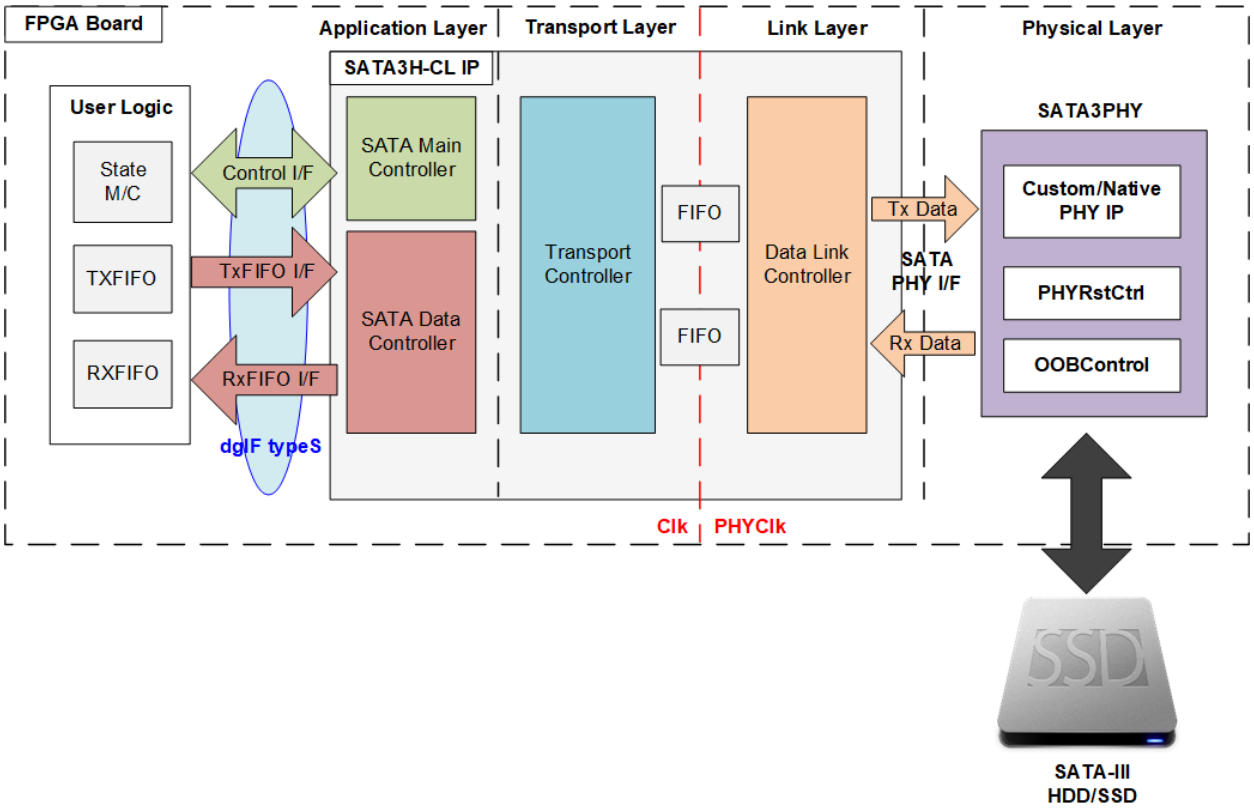

Figure 1: SATA3 Host CPUless IP Block Diagram

Applications

SATA3 Host CPUless IP Core (SATA3H-CL IP) is ideal to access SATA device without using both CPU and external memory. User interface of the IP is dgIF typeS which is easy to use. The resource utilization of the IP is less, but it can achieve very high performance. Using multiple IPs for RAID0 can increase total performance of storage system. So, it is recommended to use the IP in high-speed data recording system or big-data storage.

General Description

The SATA3 Host CPUless IP Core implements application layer, transport layer and link layer to be the host controller for SATA device access by pure hardware logic, without CPU or external memory usage. SATA Physical layer, designed by HDL code for controlling Transceiver following SATA protocol, is the interface module connected between SATA3H-CL IP and SATA device. SATA3 PHY is provided in the reference design in the release stuff for the IP customer.

The user interface of SATA3H-CL IP is dgIF typeS interface which is very easy to access. dgIF typeS has two interfaces, i.e. control interface and data interface. The control interface includes general input parameters for Write and Read command such as start address and transfer length. The data interface for Write command (Tx FIFO) and Read command (Rx FIFO) is designed by using general FIFO interface. SATA3H-CL IP supports four ATA commands, i.e.

- IDENTIFY DEVICE to check SATA device capacity.
- SECURITY ERASE UNIT to erase data in SATA device.
- WRITE DMA (EXT) to record data to SATA device.
- READ DMA (EXT) to read data back from SATA device.

Additional commands can be customized following the customer requirement.

There is one limitation about clock frequency of user logic. User logic clock frequency must be more than or equal to SATA3 PHY core clock frequency (150 MHz) to maintain the bandwidth of user interface higher than or equal to SATA3 PHY bandwidth.

The reference design on Intel FPGA development boards are available to evaluate before purchasing.

Functional Description

SATA3H-CL IP is designed to be all-in-one system, containing application layer, transport layer, and link layer in one IP, for connecting with PHY layer implemented by Transceiver without CPU and DDR usage.

The IP consists of four logic blocks. First, SATA Main Controller interfaces with the user by control interface of dgIF types and then manages the command received from user. Second, SATA Data Controller interfaces with the user by FIFO interface and handles with data packet of Transport controller. Third, Transport Controller manages the transport layer for creating and decoding SATA FIS (frame information structure) packet. Last, Data Link Controller interfaces with SATA3 PHY and manages the link layer. The interface between Data Link Controller and SATA3 PHY is 32-bit data stream with 4-bit control data.

SATA Main Controller

After system power-on, SATA Main Controller begins the initialization process of the lower layer module with SATA device. After finishing, SATA link is established and ready to transfer the packet. Next, the IP is ready to received command from user. When user sends new command request, the input parameters, (Command, Address and transfer size) are loaded to the IP for creating the command packet sent to the SATA device. After that, SATA Main Controller also decodes the status packet returned from SATA device to finish the operation. Error is asserted to the user interface when SATA Main Controller detects failure status.

SATA Data Controller

This module controls data flow between user interface (FIFO) and SATA device. In Write command, the controller reads the data from TxFIFO I/F and appends the header for creating the data packet sent to the transport controller. If the transfer data size is larger than the maximum packet size, the controller splits to be multiple packets. In Read command, the controller checks and removes the packet header. Only raw data is sent to the RxFIFO I/F. Besides, data output from Identify device command is forwarded to Iden port which is RAM interface.

Transport Controller

The Transport Controller manages the packet in transport layer, constructs frame information structure (FIS) for transmission and decomposes received frame information structures. FIS is the data format for transferring with Data Link Conroller via two FIFOs which are asynchronous FIFO type.

Data Link Controller

The Data Link Controller manages the packet in link layer. Primitive is transferred between Data Link controller and SATA3 PHY. Data Link Controller creates and receives primitives following the control signals from transport layer. Also, CRC generator and packet scramble/de-scramble module are implemented in the controller.

User Logic

This block can be designed by using simple logic. Figure 1 shows the example of user logic which consists of State machine and two FIFOs. State machine is designed to create parameters of Control I/F and monitors status of Control I/F. Two FIFOs are applied to connect with Data I/F of SATA3H-CL IP. To store data from Identify device command, 512-byte RAM with 32-bit data bus can be applied.

SATA3 PHY

SATA3 PHY design is designed by using PHY IP which is different in each FPGA model. This module is designed by HDL code and proved on many Intel evaluation boards at SATA-III speed. Supporting the additional board can be requested to our support team. The operation on user board or user design cannot be guaranteed from physical characteristic problem on the customized board.

SATA PHY consists of three parts, i.e. PHY IP which integrating Transceiver, PHY Reset Controller and OOB Control. Transceiver is the hardware inside the FPGA and the characteristic is different for each FPGA model. PHY Reset Controller is the controller for controlling reset timing of PHY IP. OOB Control includes state machine for SATA initialization from system boot to link up status.

Core I/O Signals

Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals

Signal	Dir	Description
User Interface (Synchronous to Clk)		
RstB	In	Synchronous reset signal. Active low. Deasserted to '1' after Clk signal input is stable.
Clk	In	User clock. At least 150 MHz for SATA3
Control I/F of dgIF typeS (Synchronous to Clk)		
UserCmd[1:0]	In	User Command. "00": Identify device, "01": Security erase unit, "10": Write SATA device, "11": Read SATA device. Note: 1) Security erase unit operation time depends on SATA device characteristic. It may take long time to complete the operation. So, timeout counter in IP is disabled when running Security erase unit command. 2) Security erase unit is not mandatory command, so user must confirm SATA device supports Security erase unit from specification or Identify device command.
UserAddr[47:0]	In	Start address of SATA device to write/read in sector unit (512 byte).
UserLen[47:0]	In	Total transfer size in the request in sector unit (512 byte). Valid from 1 to (LBASize-UserAddr).
UserReq	In	Request the new command. Can be asserted only when the IP is Idle (UserBusy='0'). Asserted with valid value on UserCmd/UserAddr/UserLen signals.
UserBusy	Out	IP Busy status. '1'-Busy, '0'-Idle. New request is not allowed if this signal is asserted to '1'.
LBASize[47:0]	Out	Total capacity of SATA device in sector unit (512 byte). Default value is 0. This value is updated after user sends Identify device command.
UserError	Out	Error flag. Assert when UserErrorType is not equal to 0. The flag can be cleared to '0' only by asserting RstB signal to '0'.
UserErrorType[31:0]	Out	Error status. Details of the error flag. [0] – Error from link layer such as CRC error and wrong primitive sequence. [1] – Error from Data FIS header [2] – Error from Status FIS [3] – Error from DMA active FIS. Write operation cannot complete. [4] – Error from PIO Setup FIS, failure in Identify device command. [5] – Timeout error. No FIS returned from SATA device in time. [31:6] – Reserved
Data I/F of dgIF typeS (Synchronous to Clk)		
UserFifoWrCnt[15:0]	In	Write data counter of received FIFO. Used to check full status. If total FIFO size is less than 16-bit, please fill '1' to the upper bit. UserFifoWrEn can be asserted to '1' when UserFifoWrCnt[15:3] is not equal to all 1.
UserFifoWrEn	Out	Write data valid of received FIFO.
UserFifoWrData[31:0]	Out	Write data bus of received FIFO. Synchronous to UserFifoWrEn.
UserFifoRdCnt[15:0]	In	This signal is unused for this IP.
UserFifoEmpty	In	FIFO empty flag of transmit FIFO to check data available status. '0'-Data available, '1'-Empty.
UserFifoRdEn	Out	Read valid of transmit FIFO.
UserFifoRdData[31:0]	In	Read data returned from transmit FIFO. Valid in the next clock after UserFifoRdEn is asserted to 1'.

Signal	Dir	Description
Other Interface (Synchronous to Clk)		
TestPin[31:0]	Out	Reserved to be IP test point.
TimeOutSet[31:0]	In	Timeout value to wait FIS returned from SATA device. Time unit is equal to time unit of Clk signal.
IdenWrEn	Out	Valid signal of IdenWrAddr and IdenWrData. Asserted to '1' after Identify Device command is requested.
IdenWrAddr[6:0]	Out	Index of IdenWrData in 32-bit unit. Synchronous to IdenWrEn
IdenWrData[31:0]	Out	512-byte data from Identify device command. Synchronous to IdenWrEn.
SATA3 PHY Interface (Synchronous to PHYCLK)		
PHYCLK	In	Clock output from SATA3 PHY to synchronos with TX interface of SATA3 PHY (150 MHz).
LINKUP	In	Indicate that SATA link communication is established. '1'-Link up, '0'-Not link up.
TXDATA[31:0]	Out	32-bit transmit data from the core to SATA3 PHY
TXDATAK[3:0]	Out	4-bit control data for the symbols of transmitted data, synchronous with TXDATA.
SATA3 PHY Interface (Synchronous to RECCLK)		
RECCLK	In	Clock Recovery to synchronous with Rx interface of SATA3 PHY (150 MHz)
RXDATA[31:0]	In	32-bit receive data from the SATA3 PHY to the core.
RXDATAK[3:0]	In	4-bit control data for the symbols of received data, synchronous with RXDATA and RXDATAVALID.
RXDATAVALID	In	Indicate that RXDATA and RXDATAK from SATA3 PHY is valid.

Timing Diagram

Initialization

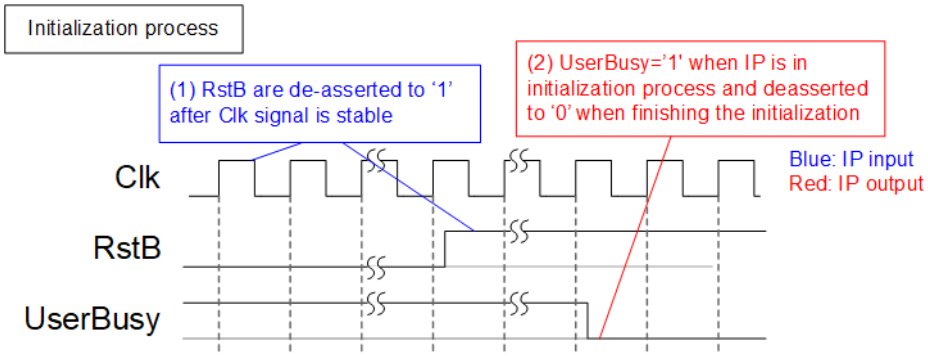

Figure 2: RstB and UserBusy during IP intialization

After Clk signal is stable, RstB can be de-asserted from '0' to '1' to start IP initailization. UserBusy flag during reset process is asserted to '1'. After finishing device initialization, UserBusy is de-asserted to '0' and the IP is ready to receive the new command, as shown in Figure 2.

Control interface of dgIF typeS

dgIF typeS signals are split into two groups. First is control interface for sending command with the parameters and monitoring the status. Second is data interface for transferring data stream in both directions.

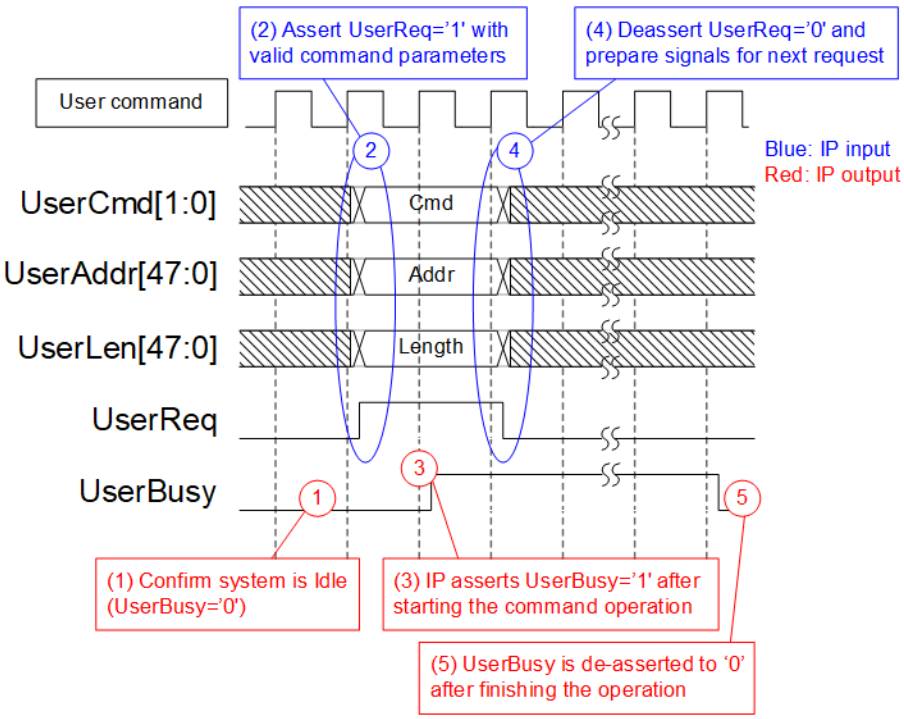

Figure 3: Control Interface of dgIF typeS Timing diagram

1) Before sending new command to the IP, UserBusy must be equal to '0' to confirm the IP is the Idle state.
2) Command and the parameters such as UserCmd, UserAddr, and UserLen must be valid and stable when UserReq is asserted to '1' for sending the new command request.
3) IP asserts UserBusy to '1' when starting the new command operation.
4) After UserBusy is asserted to '1', UserReq is de-asserted to '0' to finish the current request. New parameters for the next command could be prepared on the bus. UserReq for the new command must not be asserted to '1' until the current command operation is finished.
5) UserBusy is de-asserted to '0' after the command operation is completed. New command request could be sent by asserting UserReq to '1'.

Note: *The number of parameters using in each command is different.*

Write and Read command: Use UserCmd, UserAddr, and UserLen.
Identify device and Security Erase command: Use only UserCmd.

Data interface of dgIF typeS

Data interface of dgIF typeS is used to transfer data stream during operating Write command or Read command. The interface is compatible to general FIFO interface.

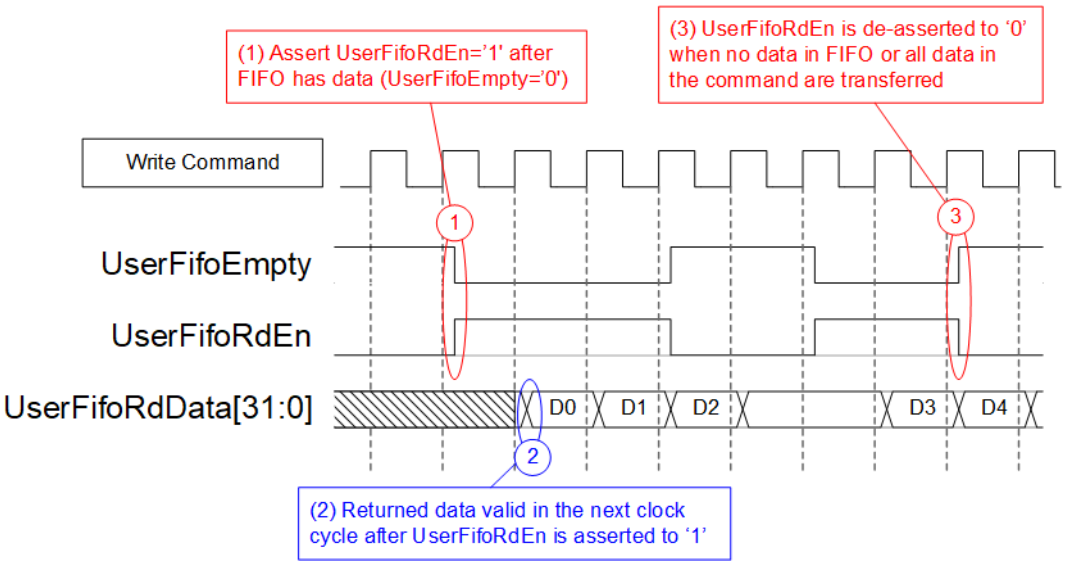

Figure 4: Transmit FIFO Interface for Write command

In Write command, data is read from Transmit FIFO until total data are completely transferred. The details are described as follows.

1) The IP waits until the data is available for reading, detected by UserFifoEmpty='0'. Next, assert UserFifoRdEn to '1' to read data input when SATA device is ready to receive data.
2) UserFifoRdData must be valid in the next clock after UserFifoRdEn is asserted to '1'.
3) When FIFO does not have the data (UserFifoEmpty='1'), UserFifoRdEn is de-asserted to '0' to pause data reading. If total data in the Write command is transferred, UserFifoRdEn is also de-asserted to '0' to finish the Write command operation.

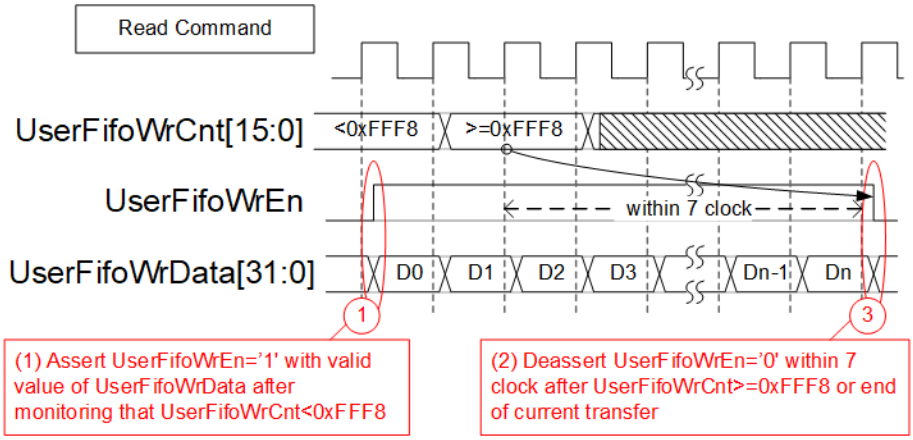

Figure 5: Received FIFO Interface for Read command

In Read command, data is sent from SATA device to Received FIFO until total data are completely transferred. The details are described as follows.

1) UserFifoWrCnt is monitored until the free space in FIFO is more than 7 (UserFifoWrCnt<65528 or 0xFFF8). After that, UserFifoWrEn is asserted to '1' at the same time as the valid data on UserFifoWrData.
2) Data transferring is paused when UserFifoWrCnt is more than 65528. UserFifoWrEn is de-asserted to '0' within 7 clock cycles after free space in FIFO is too less. Also, UserFifoWrEn is de-asserted to '0' to stop operation when Read command is finished.

Identify Device

It is recommened to send Identify device command to the IP to be the first command after system boots up. This command updates total capacity (LBASize) which must be used for calculating the input parameter limitation in Write and Read command. Note that the sum of the address (UserAddr) and transfer length (UserLen) of Write and Read command must not be more than total capacity (LBASize) of the SATA device.

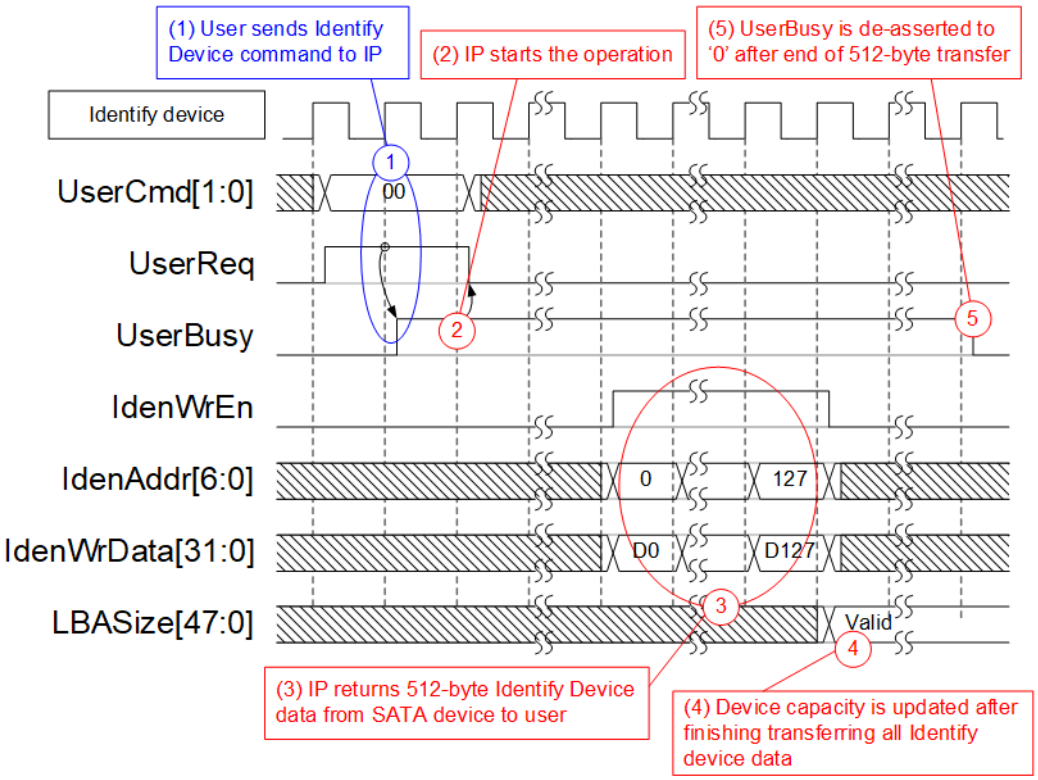

Figure 6: LBASize is updated after Identify Device command

The example steps to run Identify command are described as follows.

1) Send Identify command to the IP (UserCmd="00" and UserReq='1').
2) The IP asserts UserBusy to '1' after running Identify command.
3) 512-byte Identify device data is returned to user. IdenWrAddr is equal to 0-127 with asserting IdenWrEn. Also, IdenWrData is valid at the same clock as IdenWrEn='1'.
4) LBASize of the SATA device is updated.
5) UserBusy is de-asserted to '0' after finishing the Identify device command.

Security Erase

Securtiy Erase is the command to delete the data in the SSD. Similar to Identify device command, UserAddr and UserLen are ignored in this command. User needs to confirm that the device can support this command from the SATA device specficiation or Identify device data. Erase time of each device is different and may be very long. The estimation erase time can be checked from Identify device data.

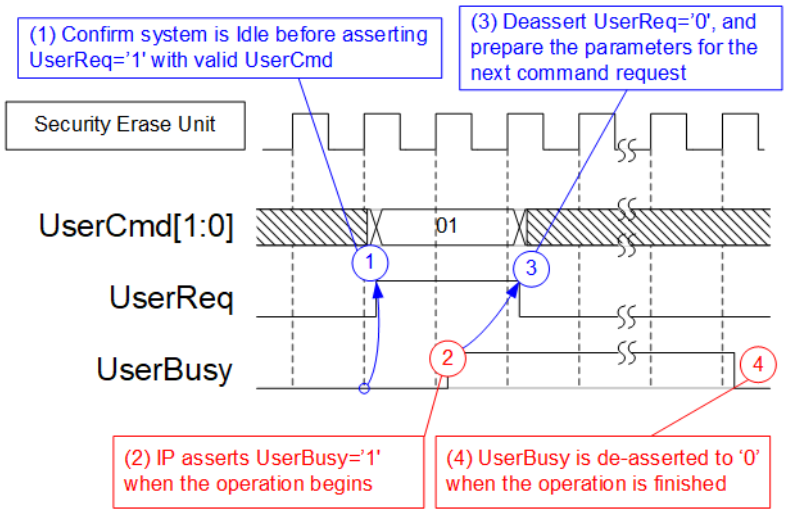

Figure 7: User interface for Security Erase Unit command

The example to run Security Erase command is described as follows.

1) Before sending the command request, the IP must be in the Idle state (UserBusy='0'). To send Security Erase command, user asserts UserReq to '1' with UserCmd="01".
2) UserBusy is asserted to '1' after the IP begins the operation.
3) UserReq is de-asserted to '0' to clear the current request when UserBusy is asserted to '1'.
4) UserBusy is de-asserted to '0' when the command operation is completed.

Error

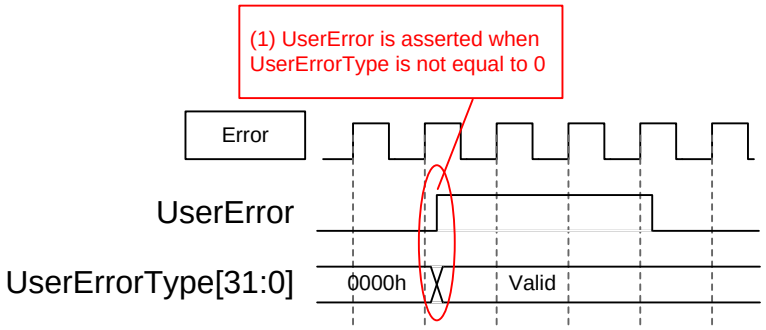

Figure 8: Error condition Timing diagram

When the error is found during running initialization process or operating some commands, UserError flag is asserted to '1'. UserErrorType is read to check the error type.

UserError flag can be cleared by RstB signal only. After the failure is solved, RstB is asserted to '0' to clear the error flag and reset the system.

Verification Methods

The SATA3 Host CPUless IP Core functionality was verified by simulation and also proved on real board design by using ArriaV GX, Arria10 GX and Cyclone10 GX development board.

Recommended Design Experience

Experience design engineers with a knowledge of QuartusII Tools should easily integrate this IP into their design.

Ordering Information

This product is available directly from Design Gateway Co., Ltd. For additional information about this product, please use the contact information on the front page of this datasheet.

Example: SATA3H-CPUless-IP-xxx

IP Core
SATA3 Host CPUless IP Core

Intel FPGA device family
A10SX=Arria 10 SX, A10GX=Arria 10 GX, C10GX=Cyclone 10 GX
S5GX=Stratix V GX, A5GX=Arria 5 GX, A5ST=Arria 5 ST

Licensing condition

1) IP Core licensing is based on single project netlist license.
2) A “Project” is defined to be a single board that is programmed using multiple bitstreams containing the core, or multiple boards that are programmed by a single bitstream containg the core.
3) The license is allowed to use the core on unlimited number of board.
4) Technical support for this license is free of charge for 90 days after delivery date by email and phone call, based on proven Intel development board.
5) License file for Quartus software is provided with a license key valid for 1 year, License file shall be renewed free of charge upon request for Licensed Project.
6) Continued technical support and warranty (annual maintenance) fee is 20% of IP Core Cost for the Licensed Project.

Please contact Design Gateway Co., Ltd directly for license agreement contract and license file.

Revision History

Revision	Date	Description
1.0	Apr-10-2020	New release

Mouser Electronics

Authorized Distributor

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Design Gateway:

SATA3H-CPUless-IP-A10SX SATA3H-CPUless-IP-C10GX SATA3H-CPUless-IP-S5GX SATA3H-CPUless-IP-A5GX SATA3H-CPUless-IP-A5ST