

USB3.0-IP FMC demo board Manual [Ver2.0E]

AB07-USB3FMC (2.5V I/O) or AB07-USB3FMC-1.8VIF (1.8V I/O)

Introduction

Thank you for choosing USB3.0-IP FMC demo board [Part Number: AB07-USB3FMC] (“demo board” in this manual).

The demo board will connect with FPGA Evaluation board that furnishes FMC extension connector, so that user can evaluate USB3.0-IP from DesignGateway. The demo board can be applicable to both USB3.0 Device-IP (Product number: USB3D-IPxxx) evaluation and Host-IP (Product number: USB3H-IPxxx) evaluation. **Take enough care that FMC interface voltage of the demo board is fixed, so that user shall never use any FPGA board that cannot adjust to proper FMC I/O voltage. Otherwise, FPGA board or the demo board will be damaged!**

User can try USB3.0 SuperSpeed real board operation by using FPGA board with this demo board and bit-file for evaluation provided from DesignGateway.

The demo board mainly mounts following parts.

- TUSB1310A (USB3.0 PHY device from T.I) and related power supply circuit.
- A-type USB3.0 connector
- FMC-LPC connector

The 1meter-length USB3.0 AtoA cable is attached with the demo board product. USB3.0 Device-IP core (Product Name: USB3D-IPxxx) evaluation needs to use this USB3.0 cable. Note that USB3.0 AtoB cable is not attached with the product, so that user needs to arrange USB3.0 AtoB cable to evaluate USB3.0 Host-IP core (Product Name: USB3H-IPxxx).

Note that the demo board only supports SuperSpeed (5Gbps) communication and does not support any legacy USB speed. (There is no DM/DP signal connection resource for USB2.0 or earlier standard) because the demo board is dedicated to USB3.0-IP from DesignGateway only.

Package List

The demo board includes following items in its product.

- USB3FMC board: 1pcs
- USB3.0 AtoA cable: 1pcs. (AtoA cable is for Device-IP core evaluation)

Board Outline

The demo board size is 69mm width and 58.65mm length. Following figure-1 shows board outline.

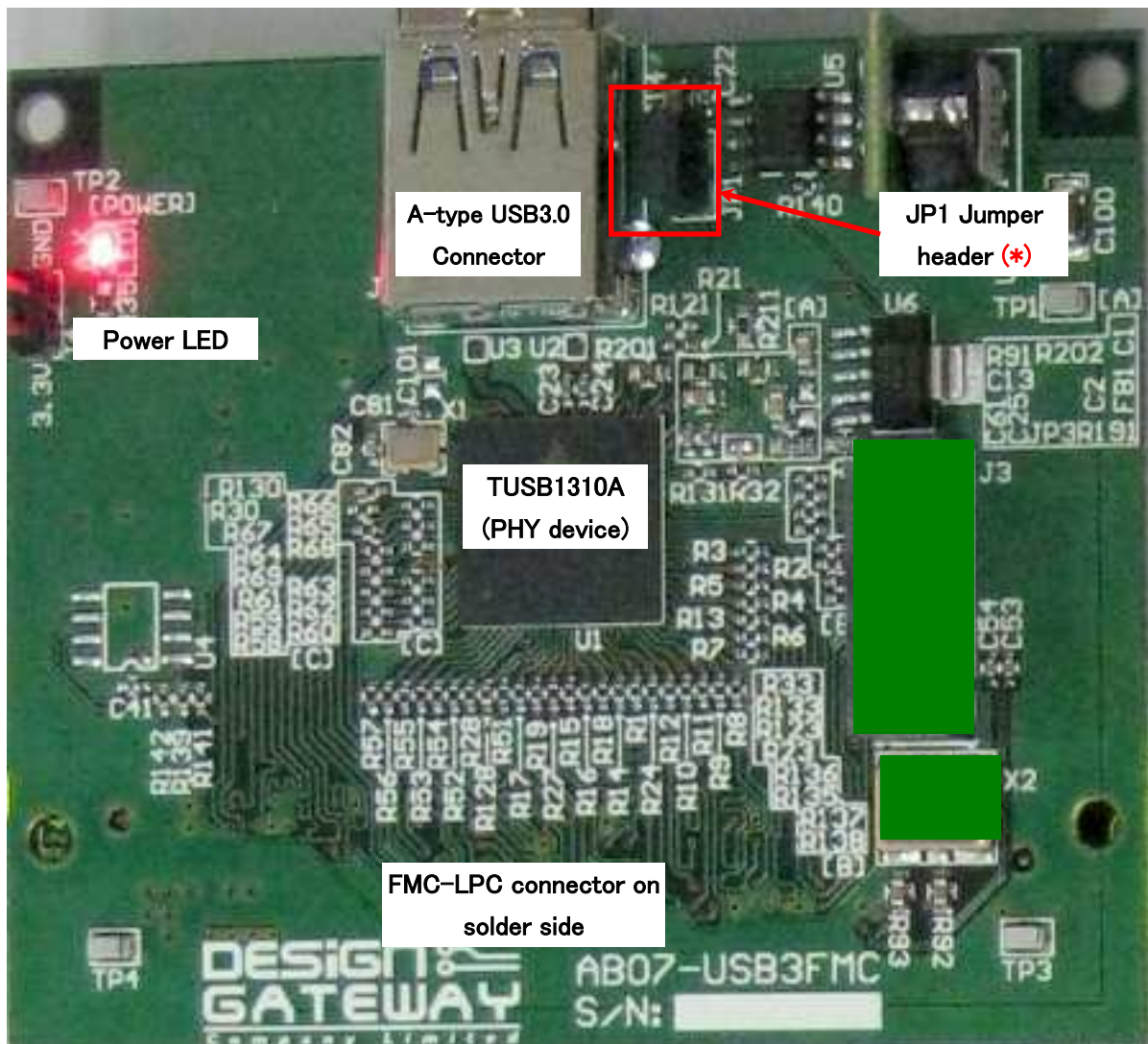


Figure-1: AB07-USB3FMC board outline

Note(*): JP1 Jumper header is to set short or open between 5V power supply from USB (VUSB) and on-board 5V power supply output.

When evaluate Device-IP, do not set Jumper Socket on JP1.

When evaluate Host-IP, set Jumper Socket on JP1.

Pin Assignment

Pin assignment between FPGA I/O pin and TUSB1310 is listed following table-1. For AB07-USB3FMC-1.8VIF, this board only supports 1.8V I/O so that it cannot connect with SP605 or ML605, however, signal connection information between FMC pin and TUSB1310A is same as AB07-USB3FMC.

| Demo Bd.FMC-LPC | | TUSB1310A on Demo Bd | | XC6SLX45 on SP-605 | | XC6VLX240 on ML-605 | | Remark |
|-----------------|----------------|----------------------|-----------------------|--------------------|---------------------------|---------------------|--------------------------|----------|
| FMC Pin# | FMC definition | Chip Pin# | TUSB1310A signal name | FPGA PIN# | Spartan-6 pin attribution | FPGA PIN# | Virtex-6 pin attribution | |
| C10 | LA06_P | P2 | TX_DATA4 | D4 | L2P_0 | K33 | L16P_16 | |
| C11 | LA06_N | | USB_PWEN | D5 | L2N_0 | J34 | L16N_16 | Not used |
| C14 | LA10_P | M1 | TX_DATA8 | H10 | L33P_0 | F30 | L3P_16 | |
| C15 | LA10_N | F3 | RX_ELECIDLE | H11 | L33N_0 | G30 | L3N_16 | |
| C18 | LA14_P | G2 | TX_DATA15 | C17 | L50P_0 | C33 | L6P_16 | |
| C19 | LA14_N | | | A17 | L50N_0 | B34 | L6N_16 | |
| C22 | LA18_P_CC | C2 | RX_DATA4 | T12 | L29P_GC_2 | L29 | L11P_SC_15 | |
| C23 | LA18_N_CC | D3 | RX_TERM | U12 | L29N_GC_2 | L30 | L11N_SC_15 | |
| C26 | LA27_P | B4 | RX_DATA10 | AA10 | L41P_2 | R31 | L14P_15 | |
| C27 | LA27_N | | | AB10 | L41N_2 | R32 | L14N_15 | |
| D8 | LA01_P_CC | P3 | TX_DATA2 | F14 | L36P_GC_0 | F31 | L11P_SC_16 | |
| D9 | LA01_N_CC | L11 | TX_DEEMPH0 | F15 | L36N_GC_0 | E31 | L11N_SC_16 | |
| D11 | LA05_P | N2 | TX_DATA5 | C4 | L6P_0 | H34 | L14P_16 | |
| D12 | LA05_N | K11 | TX_DEEMPH1 | A4 | L6N_0 | H33 | L14N_16 | |
| D14 | LA09_P | M2 | TX_DATA9 | F7 | L7P_0 | L25 | L18P_16 | |
| D15 | LA09_N | K3 | TX_ELECIDLE | F8 | L7N_0 | L26 | L18N_16 | |
| D17 | LA13_P | H1 | TX_DATA13 | G16 | L51P_0 | D34 | L8P_SC_16 | |
| D18 | LA13_N | | | F17 | L51N_0 | C34 | L8N_SC_16 | |
| D20 | LA17_P_CC | A6 | PCLK | Y11 | L32P_GC_2 | N28 | L9P_MC_15 | |
| D21 | LA17_N_CC | | (GND) | AB11 | L32N_GC_2 | N29 | L9N_MC_15 | |
| D23 | LA23_P | B1 | RX_DATA5 | U9 | L50P_2 | R28 | L18P_15 | |
| D24 | LA23_N | C7 | RX_STATUS2 | V9 | L50N_2 | R27 | L18N_15 | |
| D26 | LA26_P | A3 | RX_DATA7 | U14 | L16P_2 | L33 | L6P_15 | |
| D27 | LA26_N | | | U13 | L16N_2 | M32 | L6N_15 | |

Table-1: Pin connection list

| Demo Bd.FMC-LPC | | TUSB1310A on Demo Bd | | XC6SLX45 on SP-605 | | XC6VLX240 on ML-605 | | Remark |
|-----------------|----------------|----------------------|-----------------------|--------------------|---------------------------|---------------------|--------------------------|----------|
| FMC Pin# | FMC definition | Chip Pin# | TUSB1310A signal name | FPGA PIN# | Spartan-6 pin attribution | FPGA PIN# | Virtex-6 pin attribution | |
| G2 | CLK1_M2C_P | | | E16 | L37P_GC_0 | F33 | L10P_MC_16 | |
| G3 | CLK1_M2C_N | | | F16 | L37N_GC_0 | G33 | L10N_MC_16 | |
| G6 | LA00_P_CC | P5 | TX_DATA0 | G9 | L34P_GC_0 | K26 | L9P_MC_16 | |
| G7 | LA00_N_CC | M6 | TXDET_RXLPBK | F10 | L34N_GC_0 | K27 | L9N_MC_16 | |
| G9 | LA03_P | N3 | TX_DATA3 | B18 | L63P_0 | J31 | L19P_16 | |
| G10 | LA03_N | M9 | TX_MARGIN0 | A18 | L63N_0 | J32 | L19N_16 | |
| G12 | LA08_P | P1 | TX_DATA6 | B20 | L65P_0 | J30 | L13P_16 | |
| G13 | LA08_N | J3 | PHY_RESETN | A20 | L65N_0 | K29 | L13N_16 | |
| G15 | LA12_P | L2 | TX_DATA10 | H13 | L38P_0 | E32 | L2P_16 | |
| G16 | LA12_N | G3 | POWER_DOWNN1 | G13 | L38N_0 | E33 | L2N_16 | |
| G18 | LA16_P | J2 | TX_DATA12 | C5 | L8P_0 | A33 | L4P_16 | |
| G19 | LA16_N | J1 | TX_DATAK0 | A5 | L8N_0 | B33 | L4N_16 | |
| G21 | LA20_P | D1 | RX_DATA2 | R9 | L59P_2 | P29 | L19P_15 | |
| G22 | LA20_N | F1 | RX_VALID | R8 | L59N_2 | R29 | L19N_15 | |
| G24 | LA22_P | D2 | RX_DATA1 | V7 | L58P_2 | N27 | L5P_15 | |
| G25 | LA22_N | C5 | RX_STATUS0 | W8 | L58N_2 | P27 | L5N_15 | |
| G27 | LA25_P | A2 | RX_DATA6 | W14 | L20P_2 | P31 | L4P_15 | |
| G28 | LA25_N | C6 | RX_STATUS1 | Y14 | L20N_2 | P30 | L4N_15 | |
| G30 | LA29_P | A4 | RX_DATA9 | T15 | L23P_2 | N34 | L18P_15 | |
| G31 | LA29_N | B7 | RX_DATAK1 | U15 | L23N_2 | P34 | L18N_15 | |
| G33 | LA31_P | B8 | RX_DATA12 | U16 | L4P_2 | M31 | L90P_15 | |
| G34 | LA31_N | H11 | PWRPRESENT | V15 | L4N_2 | L31 | L90N_15 | |
| G36 | LA33_P | B9 | RX_DATA15 | Y17 | L15P_2 | K32 | L2P_15 | |
| G37 | LA33_N | | IPL_DD0 | AB17 | L15N_2 | K31 | L2N_15 | Not used |
| H2 | PRSNT | | (GND) | Y16 | IO_L17P_2 | AD9 | L14P_34 | |
| H4 | CLK0_M2C_P | | | H12 | L35P_GC_0 | A10 | L1P_GC_34 | |
| H5 | CLK0_M2C_N | | | G11 | L35N_GC_0 | B10 | L1N_GC_34 | |
| H7 | LA02_P | N4 | TX_DATA1 | G8 | L32P_0 | G31 | L5P_16 | |
| H8 | LA02_N | J11 | RESETN | F9 | L32N_0 | H30 | L5N_16 | |
| H10 | LA04_P | L3 | TX_DATA11 | C19 | L64P_0 | K28 | L7P_16 | |
| H11 | LA04_N | L10 | OUT_ENABLE | A19 | L64N_0 | J29 | L7N_16 | |
| H13 | LA07_P | N1 | TX_DATA7 | B2 | L3P_0 | G32 | L17P_16 | |
| H14 | LA07_N | H3 | POWER_DOWNN0 | A2 | L3N_0 | H32 | L17N_16 | |
| H16 | LA11_P | K1 | TX_CLK | H14 | L49P_0 | D31 | L15P_16 | |
| H17 | LA11_N | | (GND) | G15 | L49N_0 | D32 | L15N_16 | |
| H19 | LA15_P | H2 | TX_DATA14 | D18 | L62P_0 | C32 | L0P_16 | |
| H20 | LA15_N | G1 | TX_DATAK1 | D19 | L62N_0 | B32 | L0N_16 | |
| H22 | LA19_P | E2 | RX_DATA0 | R11 | L22P_2 | M30 | L17P_15 | |
| H23 | LA19_N | E3 | PHY_STATUS | T11 | L22N_2 | N30 | L17N_15 | |
| H25 | LA21_P | C1 | RX_DATA3 | V11 | L42P_2 | R26 | L15P_15 | |
| H26 | LA21_N | E3 | PHY_STATUS | W11 | L42N_2 | T26 | L15N_15 | |
| H28 | LA24_P | B3 | RX_DATA8 | AA14 | L6P_2 | N32 | L8P_SC_15 | |
| H29 | LA24_N | C8 | RX_POLARITY | AB14 | L6N_2 | P32 | L8N_SC_15 | |
| H31 | LA28_P | B5 | RX_DATA11 | AA16 | L19P_2 | N33 | L10P_MC_15 | |
| H32 | LA28_N | A7 | RX_DATAK0 | AB16 | L19N_2 | M33 | L10N_MC_15 | |
| H34 | LA30_P | A8 | RX_DATA13 | Y15 | L21P_2 | M26 | L3P_15 | |
| H35 | LA30_N | | USB_OVCR | AB15 | L21N_2 | M27 | L3N_15 | Not used |
| H37 | LA32_P | A9 | RX_DATA14 | W17 | L5P_2 | N25 | L1P_15 | |
| H38 | LA32_N | | IPL_DC0 | Y18 | L5N_2 | M25 | L1N_15 | Not used |

Table-1: Pin connection list (cont'd)

Disclaimer

The manufacturer of the product limits liability in following situation or use.

- Any damage to the connected Host-PC via USB interface.
- Any damage to the FPGA evaluation board or the demo board **when user mistakenly connect AB07-USB3FMC with non-2.5V FMC I/F or AB07-USB3FMC-1.8VIF with non-1.8V FMC I/F.**
- Any misoperation in Device-IP evaluation when attached USB3.0 AtoA cable is not used.
- Any misoperation in Host-IP evaluation when USB3.0 cable is not USB3.0 standard compliant.
- DesignGateway does not guarantee transfer speed performance.
- DesignGateway is exempted from any misoperation under user's original environment.

[Inquiry]

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Revision History

| Revision | Date | Description |
|----------|-------------|--|
| 1.1E | 11-Jul-2012 | Initial English manual |
| 1.2E | 23-Mar-2015 | Remove SATA description |
| 2.0E | 08-May-2017 | Added AB07-USB3FMC-1.8VIF for 1.8V FMC environment |

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